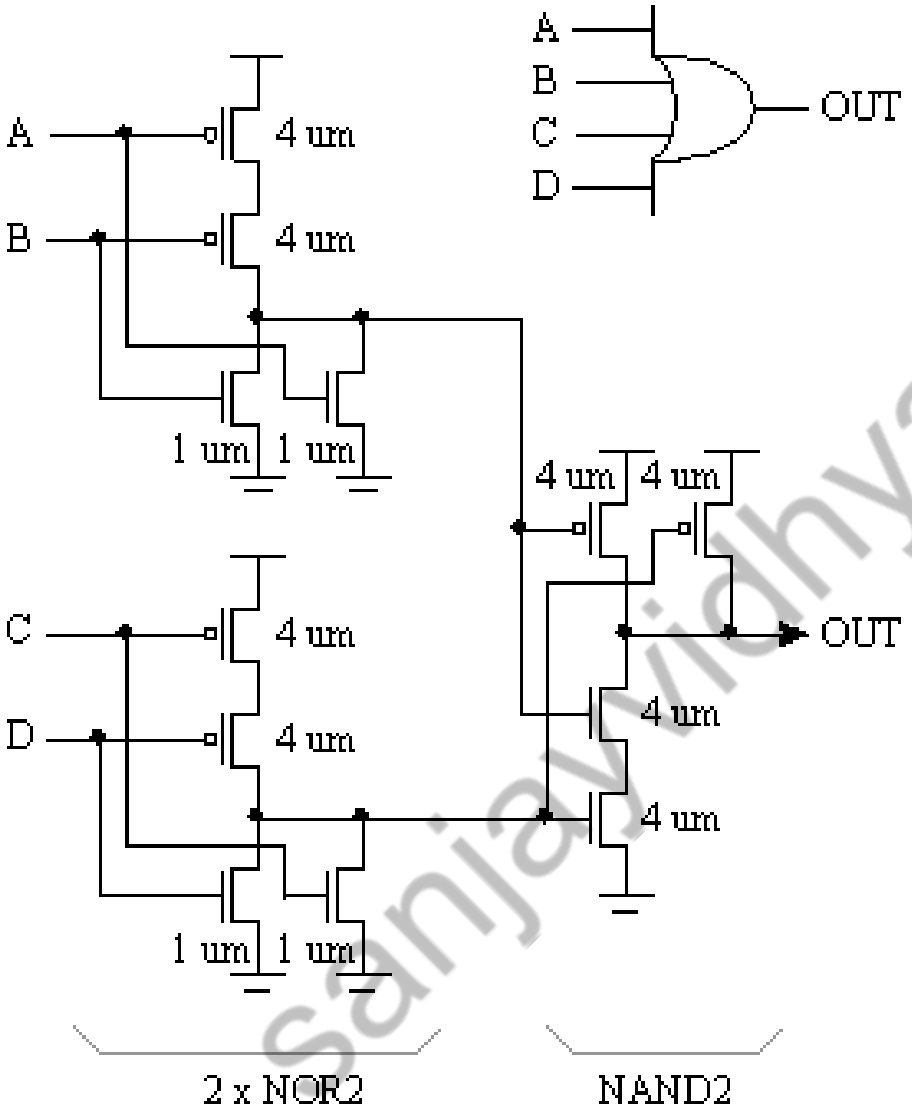
VLSI Design
Lecture 8
Dynamic Logic

By Prof. Sanjay Vidhyadharan

Static CMOS Logic



F=A+B+C+D

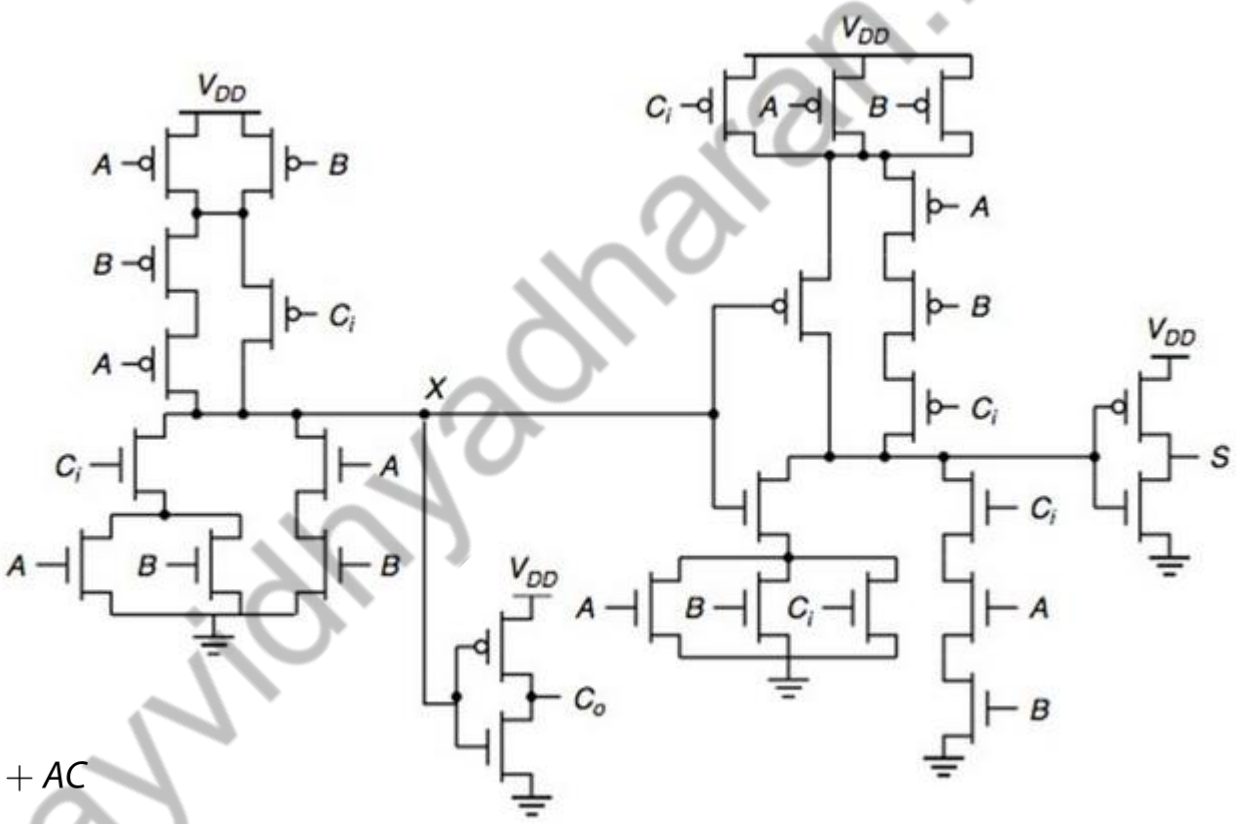
F= {[(A+B)+(C+D)]'}'

F= {(A+B)'.(C+D)'}'

- Area Large
- Static Dissipation
- Dynamic Dissipation
  - Short Circuit
  - Switching Loss

Static Full Adder

A	B	Carry In	Sum	Carry out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

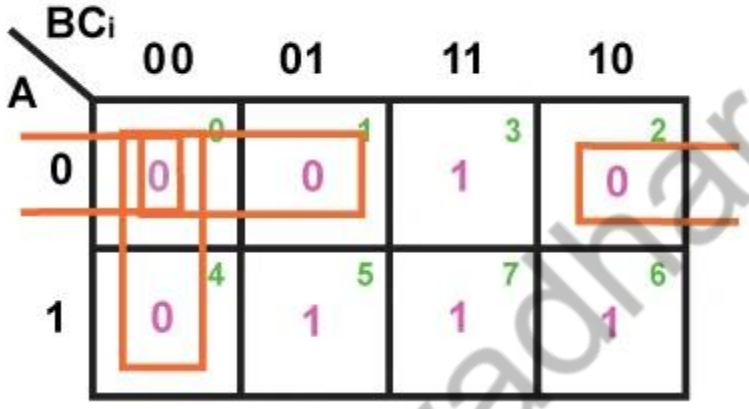


$$Carry(CY) = AB + BC + AC$$

$$Sum(S) = \bar{A}\bar{B}C + A\bar{B}\bar{C} + \bar{A}B\bar{C} + ABC$$

$$\left.\begin{aligned} CY &= AB + C(A+B) \\ S &= \overline{CY}(A+B+C) + ABC \end{aligned}\right\} \text{ Simplified Expressions}$$

CMOS 28T Mirror Adder

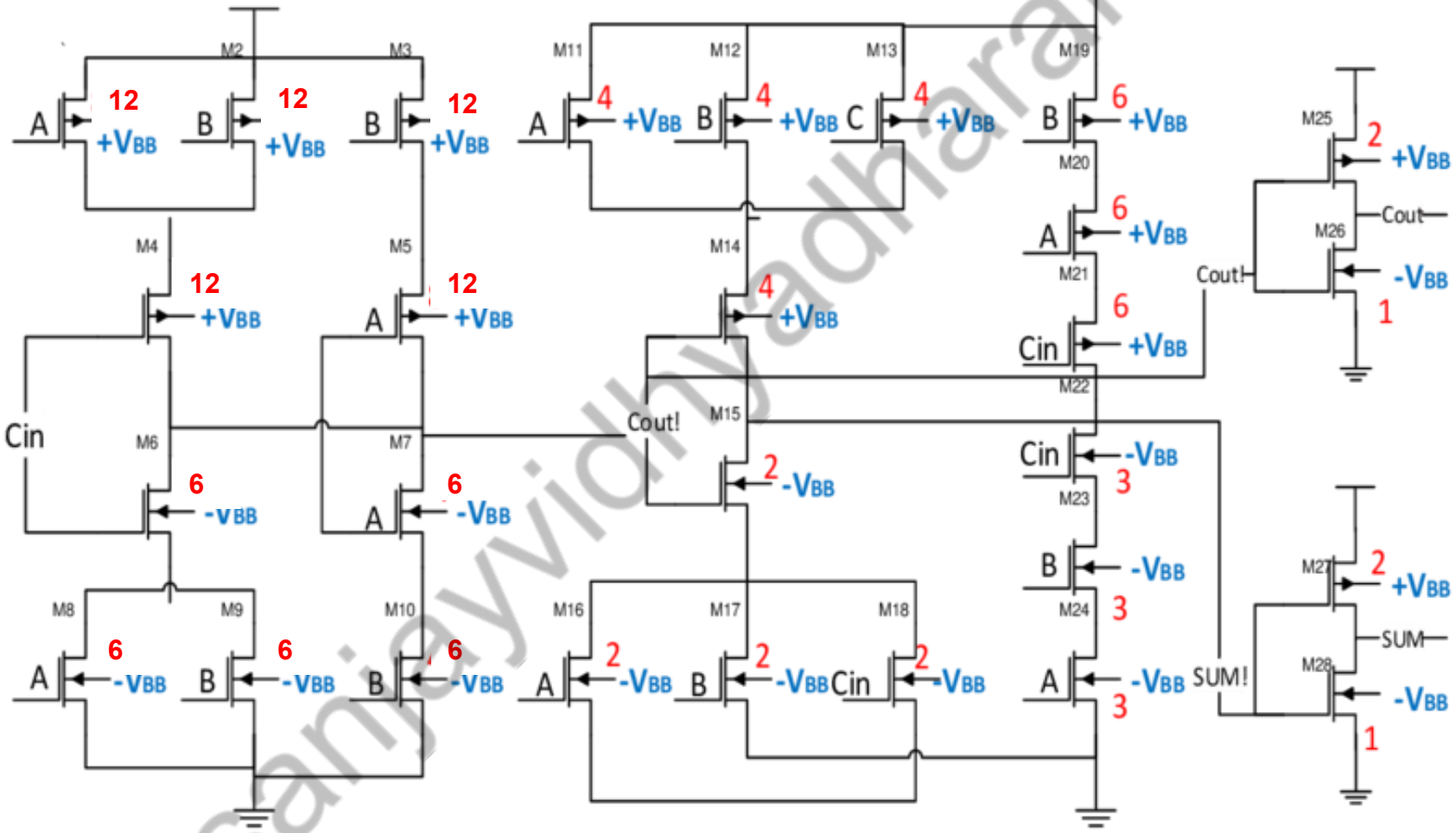


$$Carry = AB + BC + CA = AB \; + \; C(A + B)$$

$$Pull - Down\ Network\ for\ Carry\ Bar = AB \; + \; C(A + B)$$

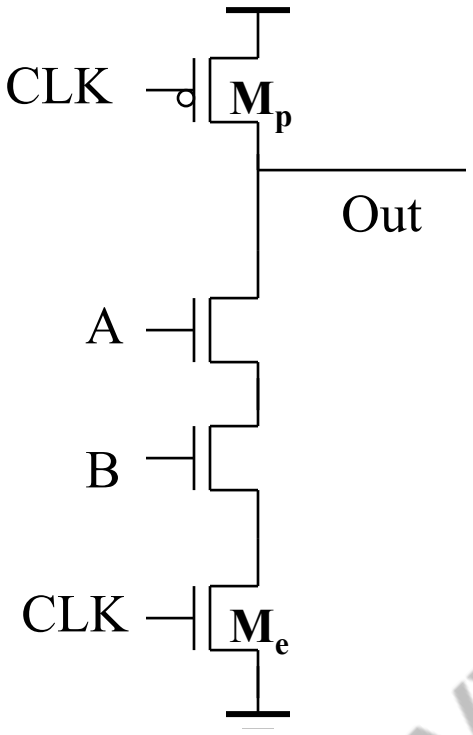
$$Pull - UP\ Network\ for\ Carry\ Bar = A'B' + B'C' + C'A'$$
$$= A'B' + \; C'(A' + B')$$

CMOS 28T Mirror Adder

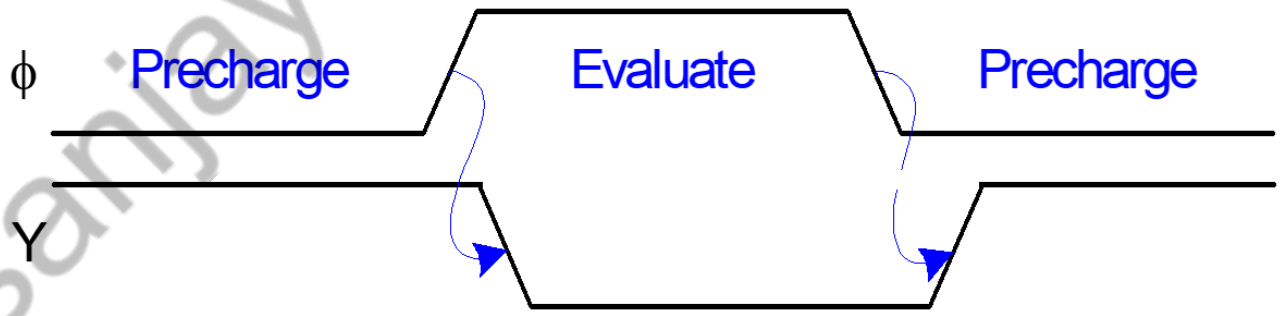


Carry Delay = 2 Gate Delay and Sum = 3 Gate Delays

Dynamic Logic



- Area Less
- Lesser Static Dissipation
- Lesser Dynamic Dissipation
  - Short Circuit
  - Switching Loss



Static vs. Dynamic

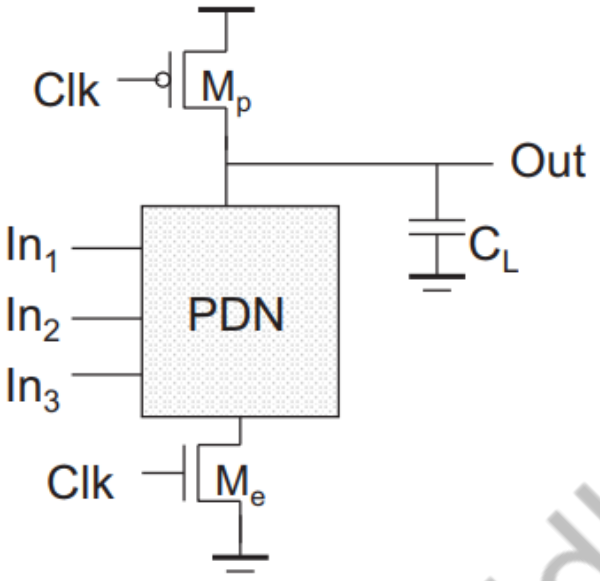
In static circuits at every point in time (except when switching) the output is connected to either GND or VDD via a low resistance path.

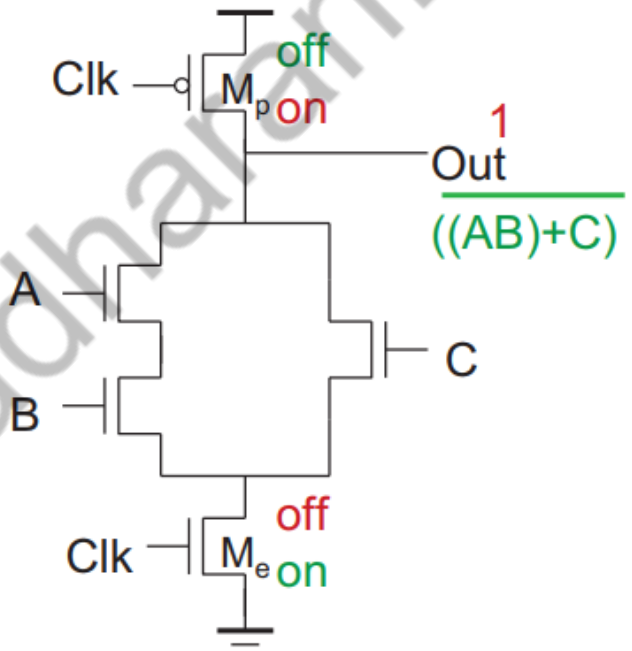
fan-in of *n* requires 2*n* (*n* N-type + *n* P-type) devices

Dynamic circuits rely on the temporary storage of signal values on the capacitance of high impedance nodes.

requires on *n* + 2 (*n*+1 N-type + 1 P-type) transistors

Dynamic Gate





Two phase operation

Precharge (Clk = 0)

Evaluate (Clk = 1)

$$OUT = \overline{CLK} + \overline{(A \cdot B + C)} \cdot CLK$$

DG needs periodic sequence of pre-charges and evaluations

Properties of Dynamic Gate

- Once the output of a dynamic gate is discharged, it cannot be charged again until the next pre-charge operation.
- Inputs to the gate can make at most one transition during evaluation.
- Output can be in the high impedance state during and after evaluation (PDN off), state is stored on CL

Properties of Dynamic Gate

- **Logic function is implemented by the PDN only**
  number of transistors is N + 2 (versus 2N for static complementary CMOS)

- **Full swing outputs (V_{OL} = GND and V_{OH} = V_{DD})**

- **Non-ratioed - sizing of the devices does not affect the logic levels**
- **Faster switching speeds**
  - Reduced load capacitance due to lower input capacitance
  - Reduced load capacitance due to smaller output loading
  - Reduced logical effort

No I_{sc} so all the current provided by PDN goes into discharging C_L

Properties of Dynamic Gate

- **Overall power dissipation usually higher than static CMOS (for low input switching activity)**
  No static current path ever exists between V_{DD} and GND (including Psc)
  Higher transition probabilities
  Extra load on Clk

- **PDN starts to work as soon as the input signals exceed V_{Tn}, so V_M, V_{IH} and V_{IL} equal to V_{Tn}**
  Low noise margin (N_{ML})
  Needs a pre-charge / evaluate clock

Speed of Dynamic Logic

Main advantages are increased speed and reduced implementation area

For low input signal no additional switching occurs $t_{pLH} = 0$!

Pre-charge time should coincide with other system function "Dead Zone"

- **For Microprocessor instruction decode**

Transition Activity

- Switching activity, $P_{0\rightarrow1}$, has two components
  - A static component – function of the logic topology
  - A dynamic component – function of the timing behavior (glitching)

2-input NOR Gate

A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

Static transition probability

$$P_{0\rightarrow1} = P_{out=0} \times P_{out=1}$$
$$= P_0 \times (1-P_0)$$

With input signal probabilities

$P_{A=1} = 1/2$

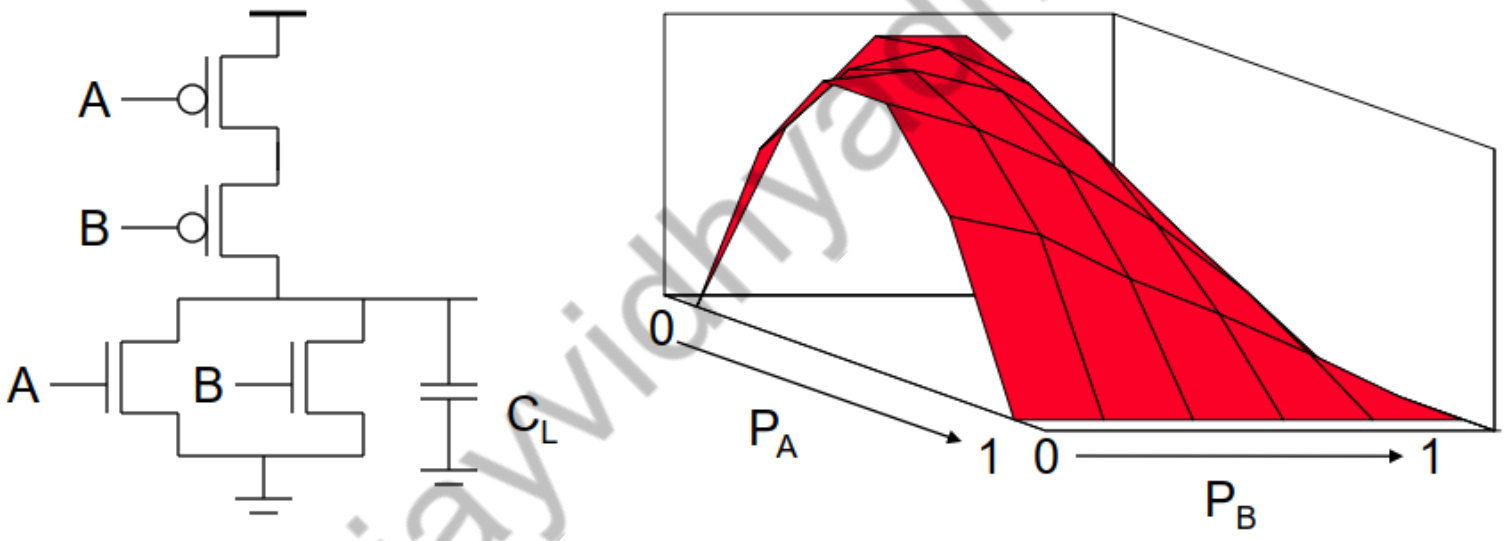
$P_{B=1} = 1/2$

NOR static transition probability

$= 3/4 \times 1/4 = 3/16$

Transition Activity

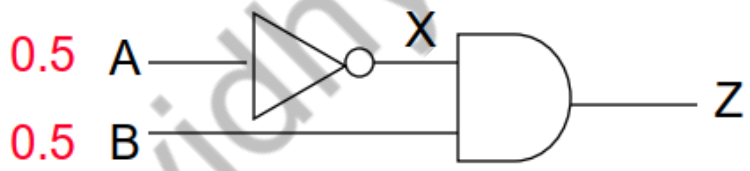
- Switching activity is a strong function of the input signal statistics
  - P_A and P_B are the probabilities that inputs A and B are one



$$P_{0\rightarrow1} = P_0 \times P_1 = (1-(1-P_A)(1-P_B))\,(1-P_A)(1-P_B)$$

Transition Activity

	$P_{0\rightarrow1} = P_{out=0} \times P_{out=1}$
NOR	$(1 - (1 - P_A)(1 - P_B)) \times (1 - P_A)(1 - P_B)$
OR	$(1 - P_A)(1 - P_B) \times (1 - (1 - P_A)(1 - P_B))$
NAND	$P_A P_B \times (1 - P_A P_B)$
AND	$(1 - P_A P_B) \times P_A P_B$
XOR	$(1 - (P_A + P_B - 2P_A P_B)) \times (P_A + P_B - 2P_A P_B)$



For X: $P_{0\rightarrow1} = P_0 \times P_1 = (1-P_A)\,P_A$

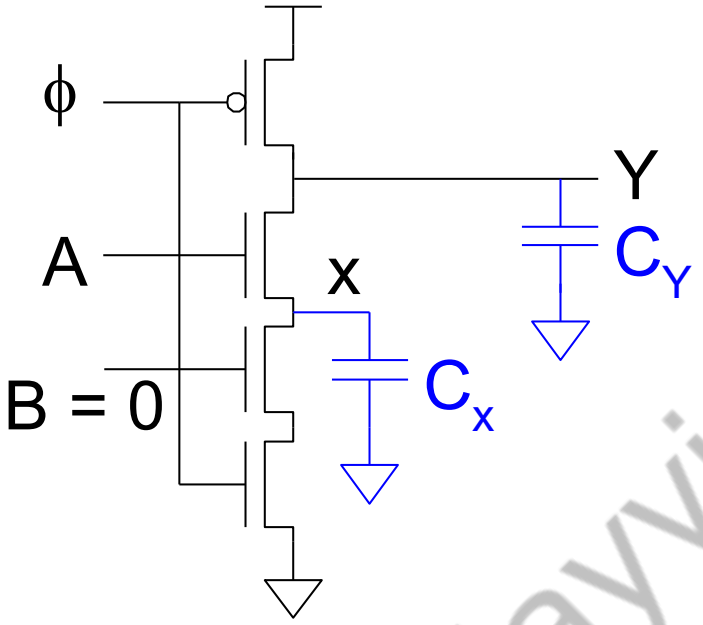
$= 0.5 \times 0.5 = 0.25$

For Z: $P_{0\rightarrow1} = P_0 \times P_1 = (1-P_X P_B)\,P_X P_B$

$= (1 - (0.5 \times 0.5)) \times (0.5 \times 0.5) = 3/16$

Dynamic Logic

- **Dynamic Logic Suffers from Charge Sharing Phenomenon**



Case1. $\Delta V_{out} > -V_{Tn}$

$|\Delta V_{out}| < V_{Tn}$

$$V_{DD} \cdot C_Y = V_Y C_Y + (V_{DD} - V_{Tn}) C_X$$

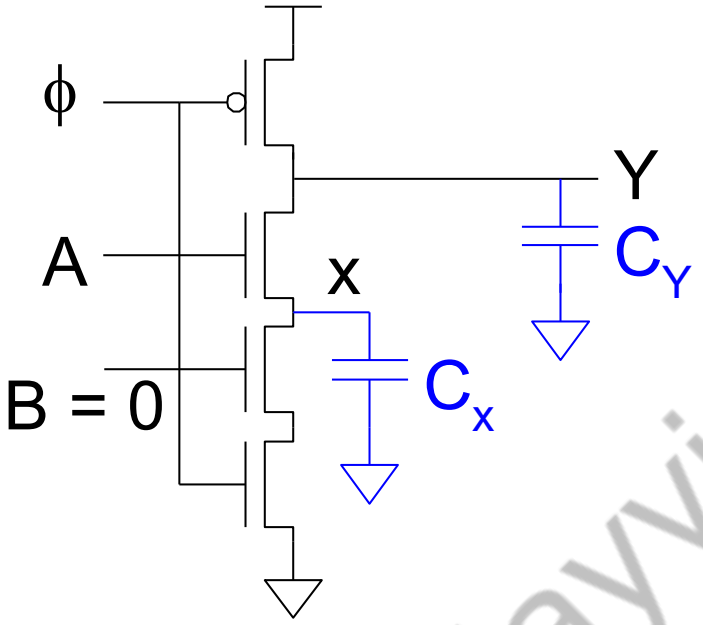
$$\Delta V_{out} = - \frac{(V_{DD} - V_{Tn}) C_X}{C_Y}$$

$$C_X << C_Y$$

$$V = Q/C$$

Dynamic Logic

- **Dynamic Logic Suffers from Charge Sharing Phenomenon**



Case2. $\Delta V_{out} < -V_{Tn}$

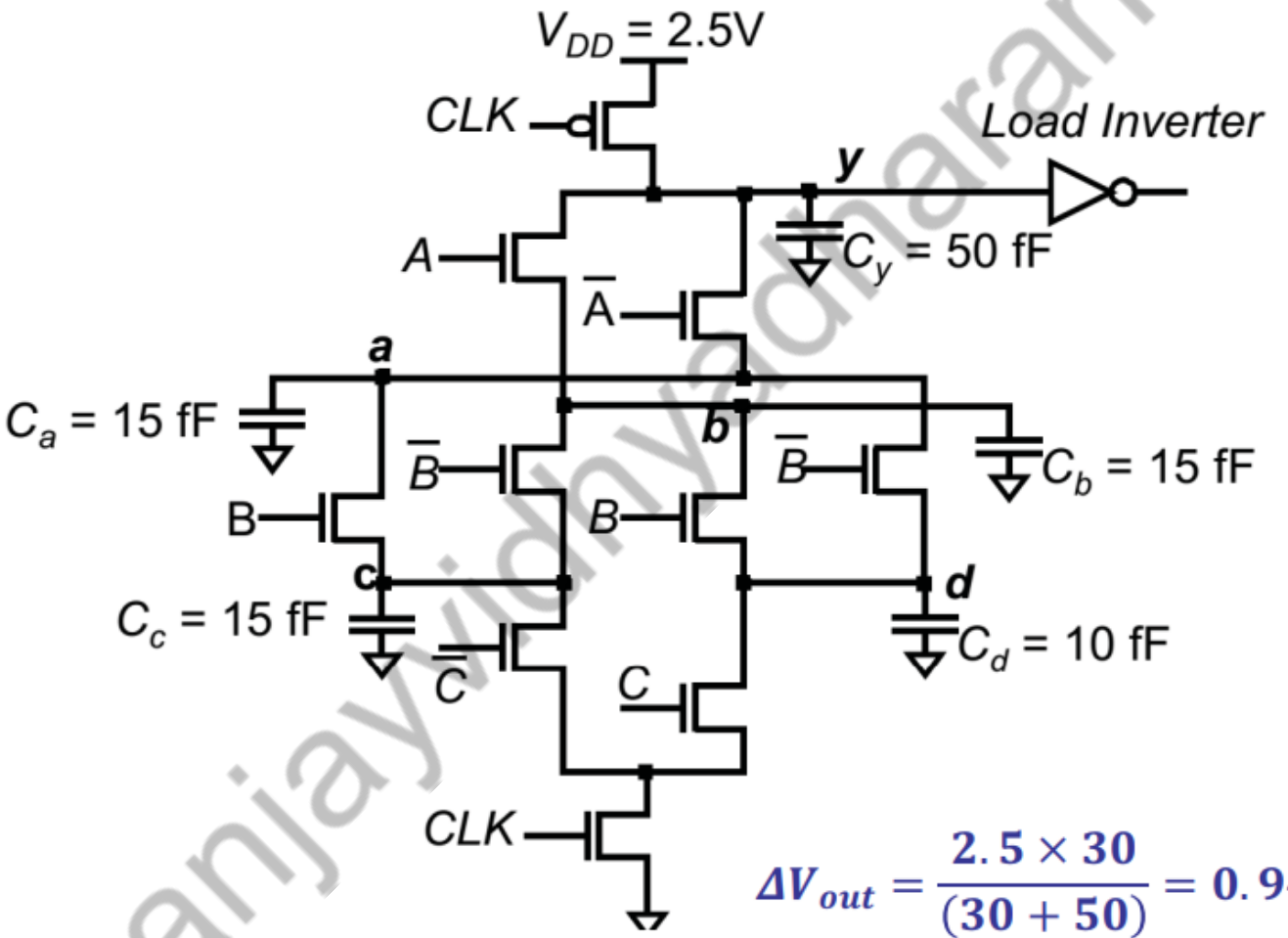
$$V_{DD}.C_Y = V_Y C_Y + V_X C_X$$

$$V_{DD}.C_Y = V_Y C_Y + V_Y C_X$$

$$V_{DD}.C_Y = (V_{DD} + \Delta V_{out})(C_Y + C_X)$$

$$\Delta V_{out} = -\frac{V_{DD} C_X}{C_{Y+} C_X}$$

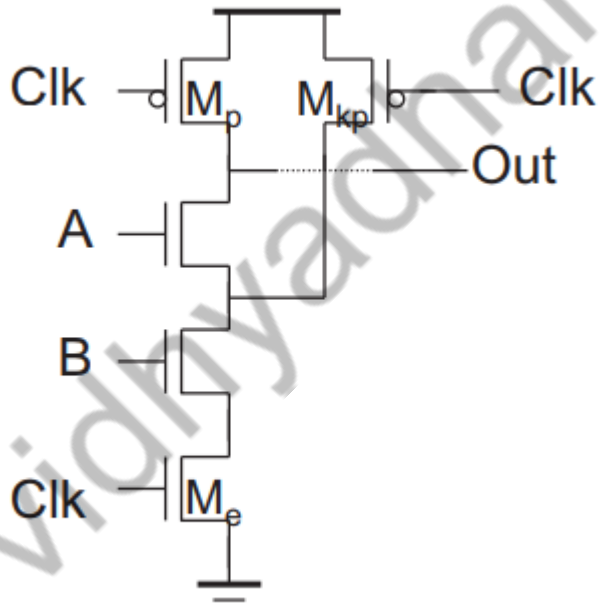
Dynamic Logic



$$\Delta V_{out} = \frac{2.5 \times 30}{(30 + 50)} = 0.94V$$

Dynamic Logic

Solution to Charge Redistribution



Pre-charge internal nodes using a clock-driven transistor (at the cost of increased area and power)

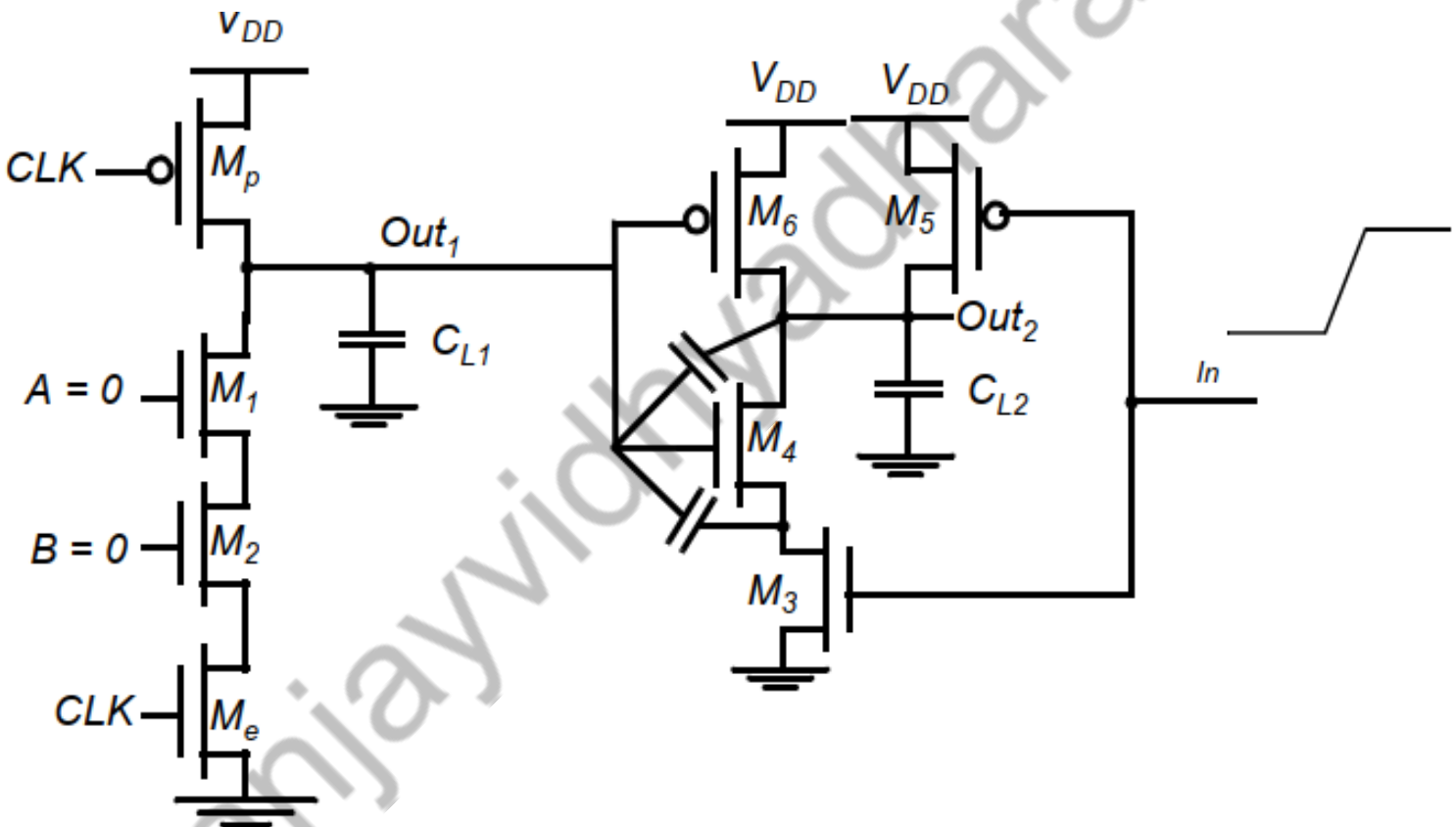
Dynamic Logic

Capacitive Coupling

The high impedance of the output node makes the circuit very sensitive to crosstalk effects. A wire routed over a dynamic node may couple capacitively and destroy the state of the floating node.

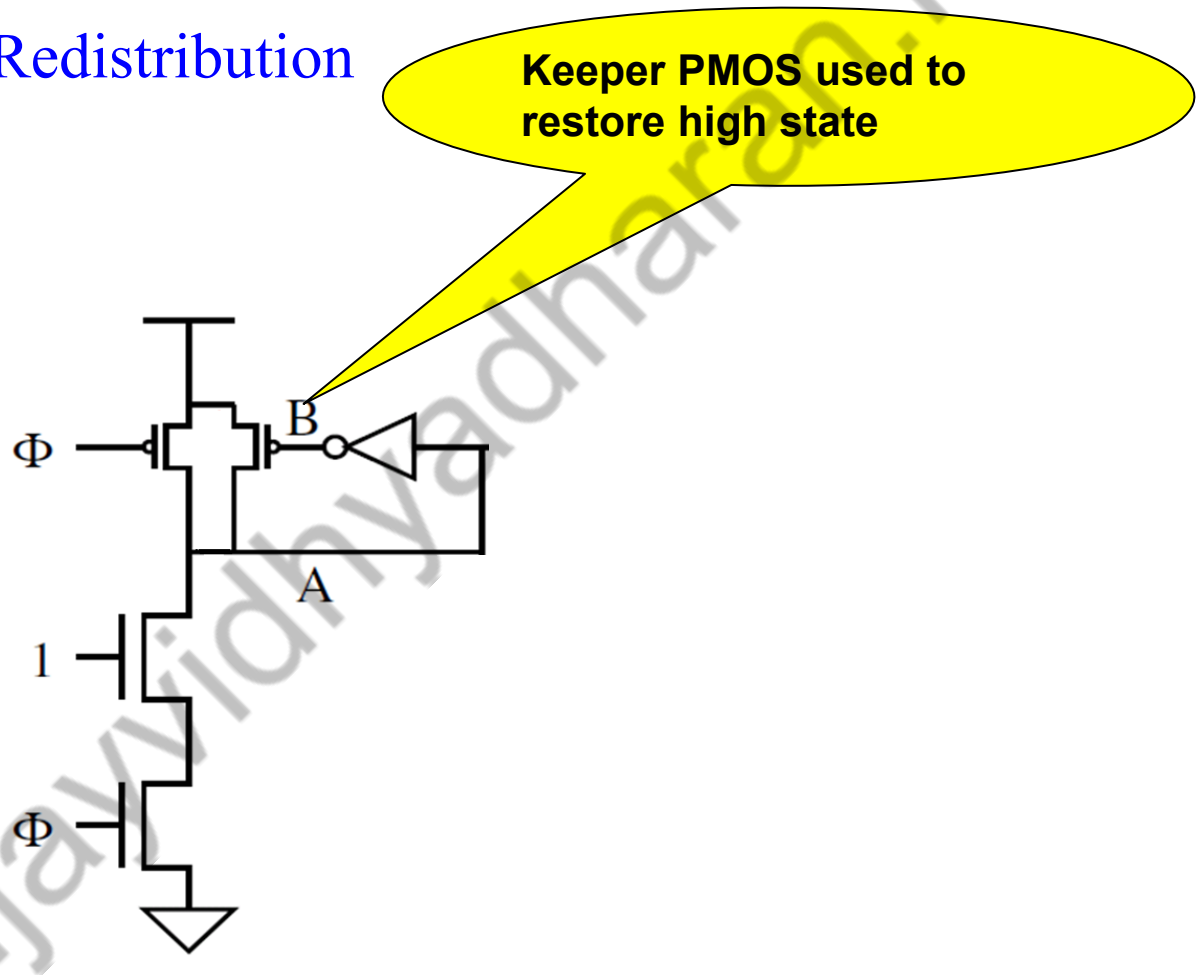
Dynamic Logic

Backgate (or output-to-input) coupling



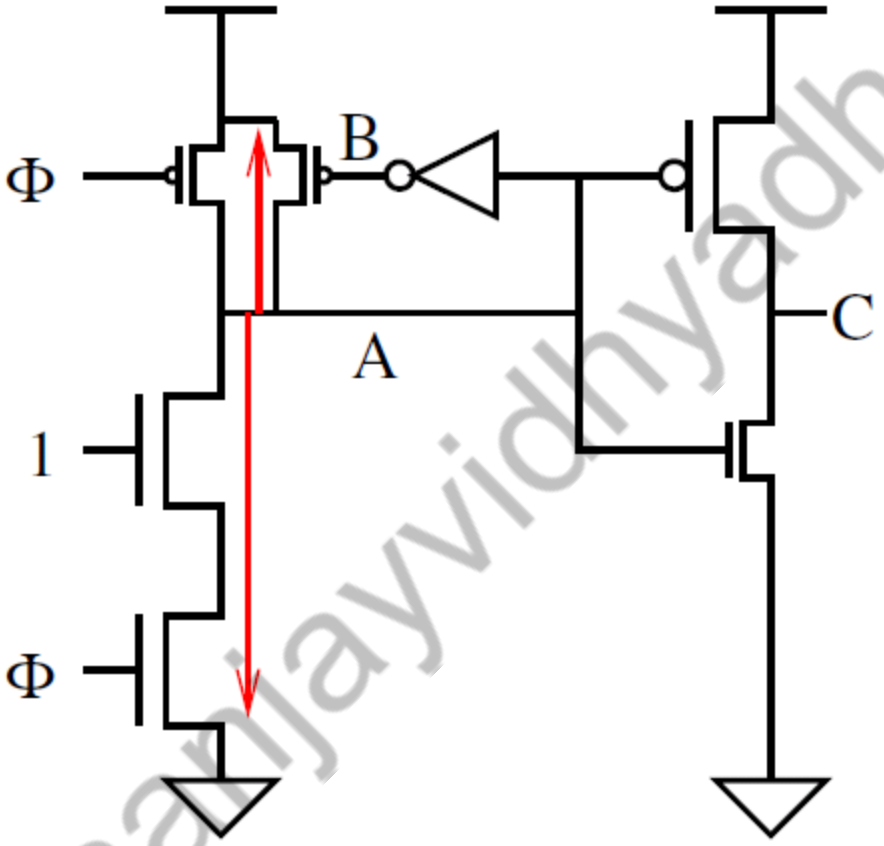
Dynamic Logic

Solution to Charge Redistribution

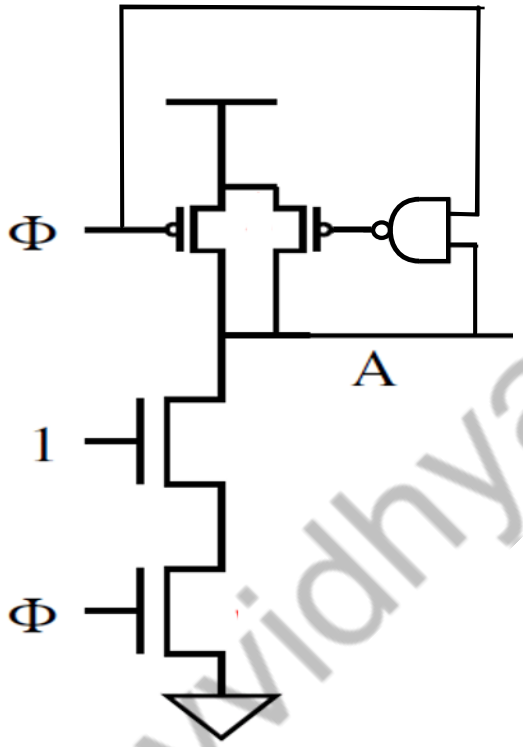


Dynamic Logic

Contention



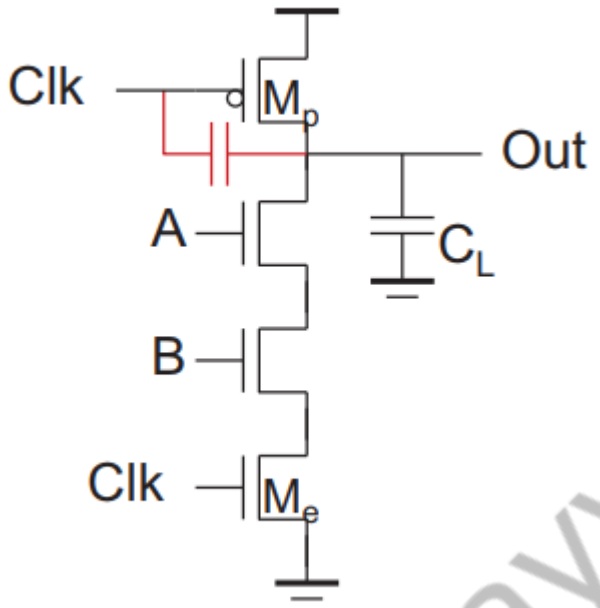
Dynamic Logic

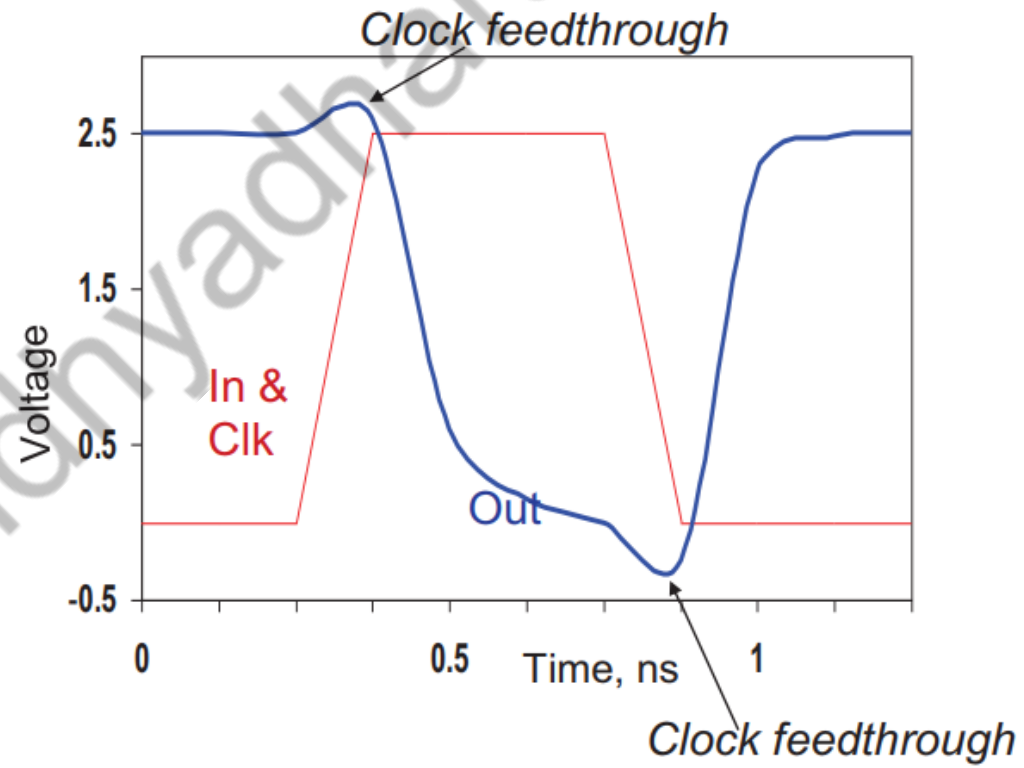


[7] M.E.S Elraba, M.H Anis, M.I Elmasry, "A contention-free domino logic for scaled down CMOS technologies with ultra low threshold voltages," *Proc. of IEEE International Symposium on Circuits and Systems* pp. 748 - 751, May 2000.

Dynamic Logic

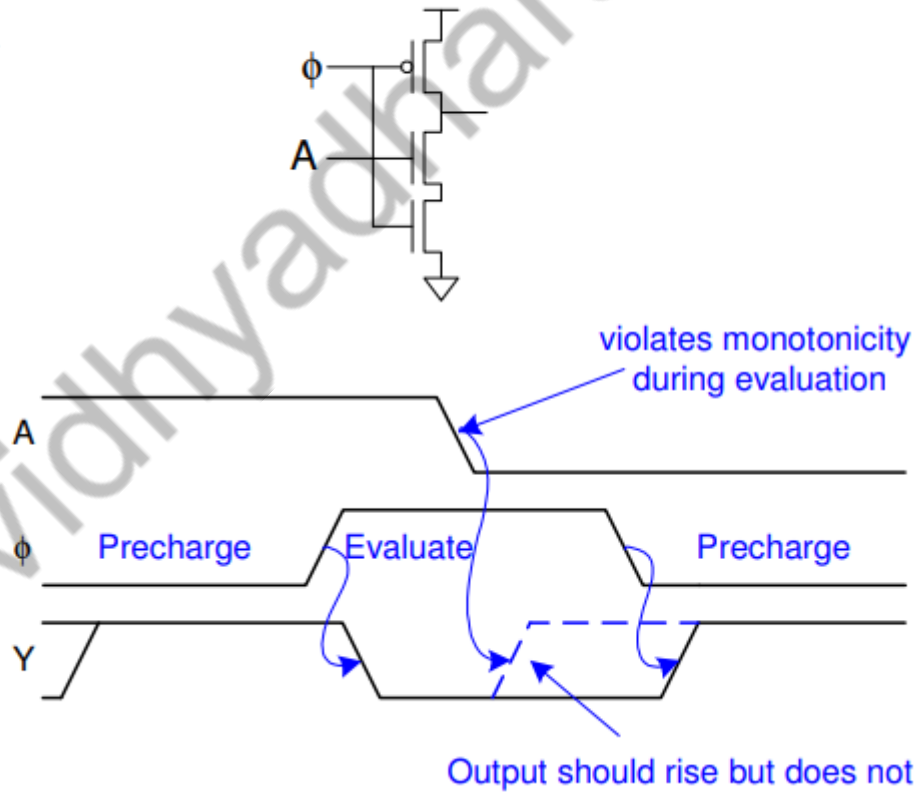
Clock-Feedthrough





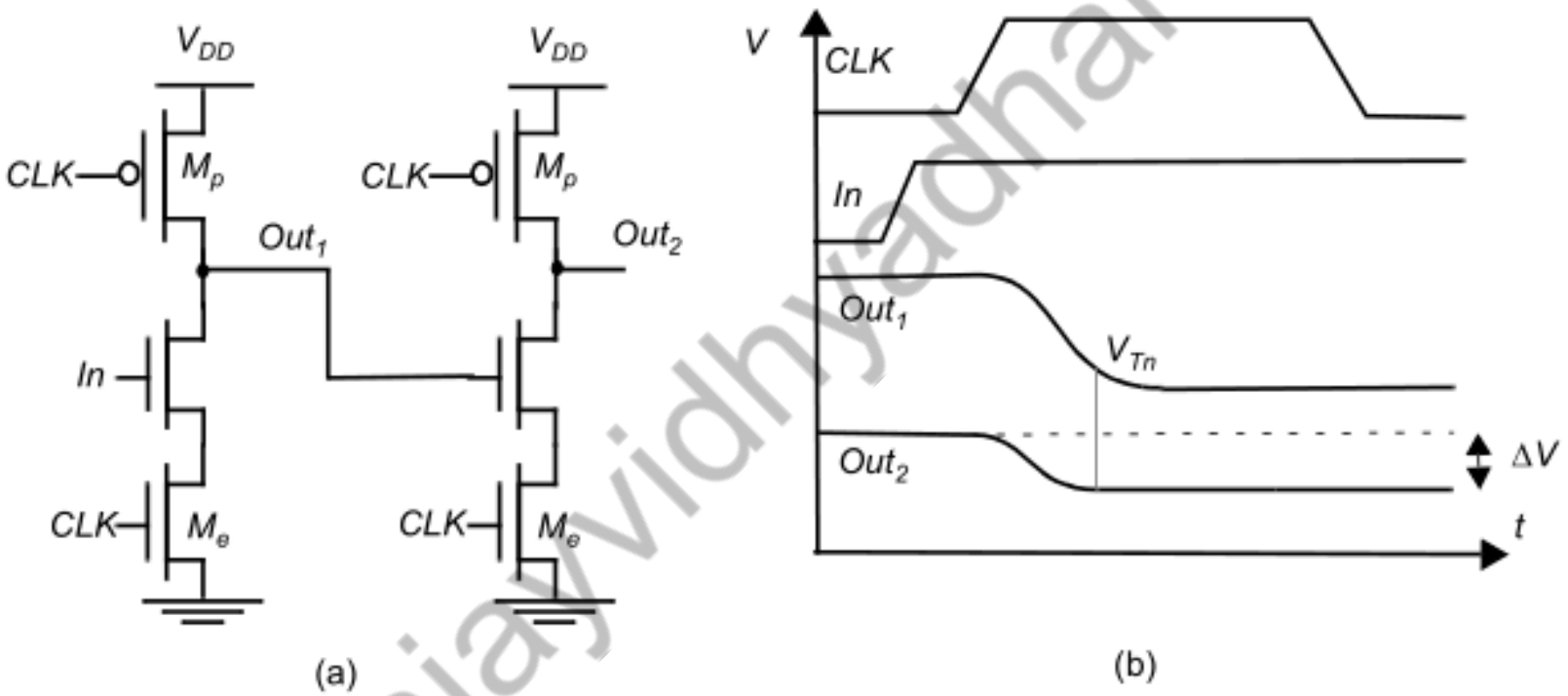
Dynamic Logic

- Dynamic gates require *monotonically rising* inputs during evaluation
  - 0 -> 0
  - 0 -> 1
  - 1 -> 1
  - But not 1 -> 0



Dynamic Logic

- **Cascading Dynamic Gates**



Thank you