# Testability of VLSI

# Lecture 13
# Analog and Mixed-Signal Testing

**By Dr. Sanjay Vidhyadharan**

# Analog Testing Difficulties

**1. Modeling Problems.** The major difference between analog *structural* test and analog *functional* test is the fault derivation and modeling procedure.

Functional test often assumes that the components are faulty and generates the fault list using component deviations and catastrophic faults. The circuit parameter values vary widely, even in good circuits. Deterministic models are inefficient for analog circuits. Therefore, signals are specified by a nominal value, along with an acceptable *range* of values around the nominal value.

Example: Minimum overall gain, Minimum BW

Structural test uses manufacturing defect statistics, and the fault list may be either catastrophic or parametric.

Example: Shorted resistance, Error in resistance value, unintended bridge resistance

Defects cannot be directly mapped to faults.

# Analog Testing Difficulties

2. **Simulation Error**. Expected analog circuit signal values (in fault free circuit) are computed by simulation, whose accuracy is limited by the numerical accuracy of the simulation algorithm, the simulation assumptions, and by the accuracy of the models of the parasitic analog devices. Also, process variations cause even good circuits to exhibit a range of different behaviors.

3. **Tester Measurement Error**. Measurement errors at the analog circuit tester come from analog offsets, the effect of the load of the measurement probe on the analog circuit behavior, and the impedance of the analog probe. Also, random noise is a problem, so analog testers are limited in bandwidth and measurement accuracy

4. **For mixed-signal chips**, transporting internal analog signals to output pins may alter the signal and the circuit functionality. Capacitive coupling between high-frequency digital signals and analog signals causes additional analog circuit noise. Analog tests must create a difference in an analog output between the good and bad machines that lies outside the measurement error of the test fixture and the ATE. Otherwise, the fault effect is masked by measurement error.

# Analog Testing Difficulties

5. **Test Accessibility Problems.** Circuit complexity and the inaccessibility of internal components restrict the use of conventional analog ATE.

6. **Information Flow**. It is difficult to test circuits by individually testing subcircuits. Consider the case of two cascaded single-input, single-output analog circuits, C1 and C2 with analog voltage transfer functions *H*1 and *H*2. and may behave unacceptably when tested individually, due to manufacturing imperfections that distort their transfer functions. However, when cascaded, it could happen that the distortion in *H*1 is cancelled by the distortion in *H*2, which might be, in some sense, the inverse of the distortion in *H*1. Therefore, the cascaded combination of C1 and C2 may actually be acceptable. Conversely, individually acceptable analog circuits, when cascaded, may produce an unacceptable circuit.

# Analog Fault Models

## 1. Catastrophic or Hard faults:

An analog component becomes open or shorted
Stuck at $V_{DD}$
Stuck at $V_{SS}$

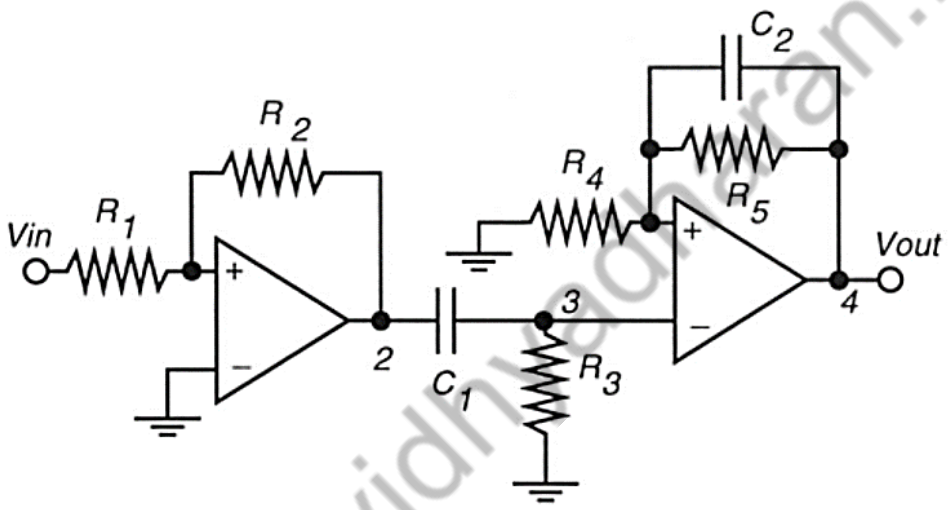
## 2. Parametric or soft faults

An analog *R*, *L*, *C*, or transistor trans-conductance value changes sufficiently that it moves outside its tolerance box and causes unacceptable performance degradation of the analog circuit.

*Single parametric* faults are interesting in multi-chip module interconnects, as they will be termination resistances or important components such as precision off-chip inductors used in RF circuits.

# Analog Fault Models

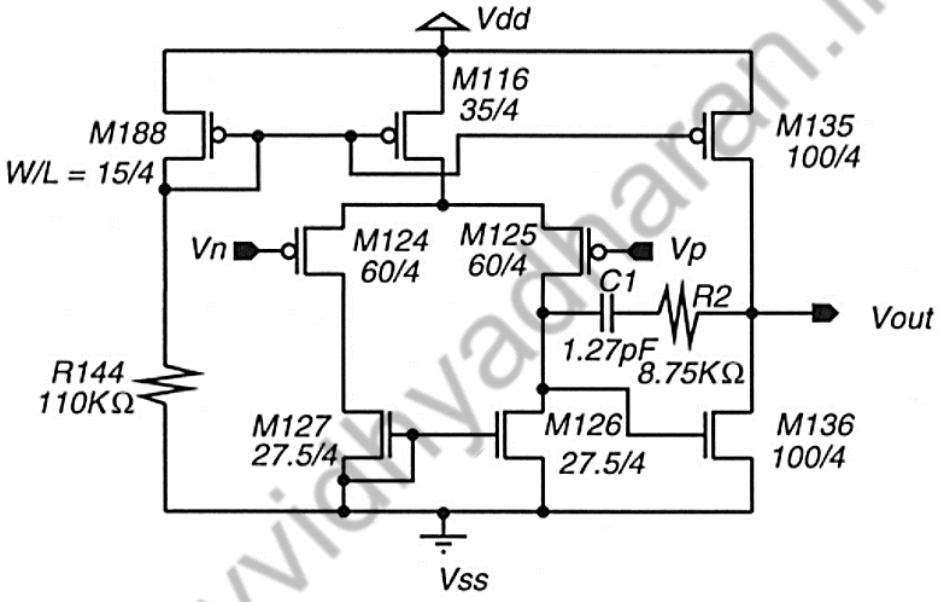
Linear analog ICs are designed so that the analog performance depends on ratios of components, so *multiple parametric* faults are most interesting in such chips. Checking




| Functional parameter | Determining components |
|---|---|
| Amplification circuit | |
| First stage gain | $R_2$ / $R_1$ |
| High-pass filter gain | $R_3$ and $C_1$ |
| High-pass filter cutoff frequency | $C_1$ |
| AC voltage gain of the low-pass filter | $R_4$, $R_5$, and $C_2$ |
| DC voltage gain of the low-pass filter | $R_4$ and $R_5$ |
| Low-pass filter cutoff frequency | $C_2$ |

# Analog Fault Models

Linear analog ICs are designed so that the analog performance depends on ratios of components, so *multiple parametric* faults are most interesting in such chips.




| OPAMP circuit | |
|---|---|
| Biasing current | $R_{144}$, $K_{M188}$, $K_{M116}$ |
| Differential linearity | $K_{M124}$, $K_{M125}$, $K_{M127}$, $K_{M126}$ |
| Output stage voltage gain | $K_{M135}$, $K_{M136}$, $K_{M188}$ |
| Compensation | $C_1$, $R_2$ |

# Levels of Abstraction

For analog testing, the *transistor level* of abstraction provides detailed models and structural interconnections for analog devices. At this level, the SPICE netlist, complete with transistor models, provides a *structural view.* The system of non-linear partial differential equations describing the netlist provides a *behavioral view.*

However, analog circuit testing can be done at a higher level of abstraction, the *functional level,* in which we model resistors, capacitors, inductors, and *ideal OPAMPs*, which have infinite gain and are considered to be fault-free. The benefits of this higher level of abstraction are modeling convenience and computational efficiency, and the liability is that OPAMPs may have faults, which should be tested for

# Types of Analog Testing

**1. Specifications based Testing.**

Each class of analog circuits has its own separate set of specifications. (Op amp, ADC, DAC, Filters,)
There already exist accepted and specific functional tests for each class of analog circuits.
There is no universal set of performance specifications.
Also, there are no general design techniques for all analog circuits.

Analog circuit tests can be classified into these three categories:

- *Design characterization,* to determine whether the design meets specifications.
- *Diagnostics,* which determine the cause of a device failure when it fails a test.
- *Production tests* used for large volumes of linear or mixed-signal circuits.

*Specification-based* tests are generated directly from the circuit specifications, without reference to an analog fault model. This approach is easily adapted to wide varieties of circuits. However, with large numbers of specifications, test application has become most expensive, and its cost must be reduced. The test set can be reduced by locating dependencies between specifications and eliminating unnecessary testing.

# Types of Analog Testing

**2. Structural fault-model based Testing**

Structural fault-model based Testing will target a specific set of modeled faults. This allows quantification of a set of analog tests in terms of their *fault coverage*, so test sets can be *graded*. The models also reduce the test set size, since test waveforms that detect faults already covered by other waveforms can be deleted. However, advocates of structural tests have been unable to establish a link between the fault coverage and satisfaction of the design specifications. This makes designers reluctant to accept structural analog testing.

# Analog Fault Simulation

At present, no viable analog circuit synthesis tools exist, so analog design is accomplished manually by experienced analog designers, who design circuits using rules of thumb. For these designers, analog fault simulation is extremely useful for *what-if* analysis, where the designer asks the question, "What would happen if the resistance of resistor were out of specification by 3.5%?" Answering this question requires analog fault simulation, which is far more computationally intensive than ordinary analog circuit simulation. It is important to take advantage of the structure of the circuit equations to concurrently simulate many analog faults.

- *DC fault simulation of non-linear circuits*
- *AC fault simulation of linear circuits*
- *Transient* or *time-domain fault simulation.*

We first apply DC tests to analog circuits, and only if the circuit passes these do we apply AC tests, which are more difficult to generate and more costly to apply. Finally, only if the circuit passes AC testing do we apply *transient* or time-domain tests.

# DC Fault Simulation

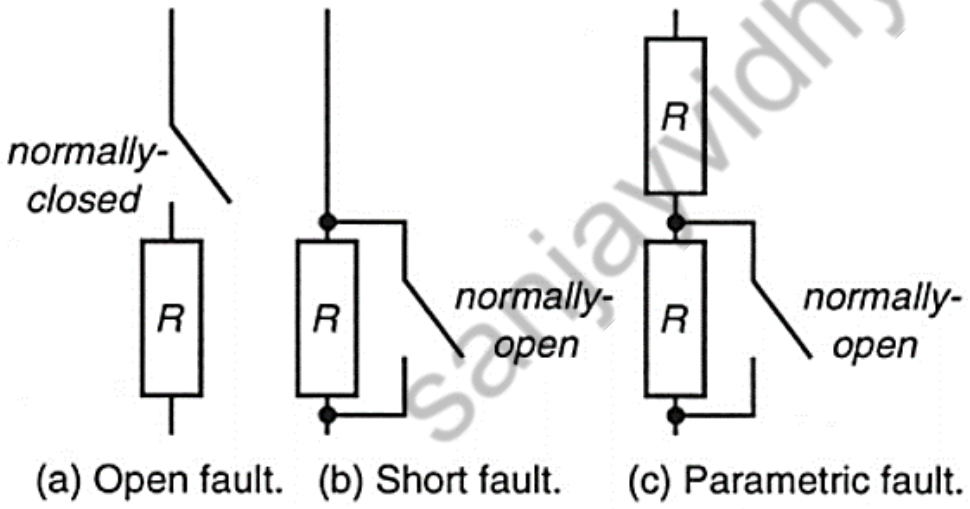
DC testing of analog circuits is attractive, because it requires less expensive testers and less testing time. DC fault simulation is useful to analyze how well a DC test can detect a given fault list. It is done by solving a set of non-linear equations using PSPICE or similar analog simulators, which converge only after many iterations. Simulation of catastrophic faults often fails to converge or causes the system matrix to be singular. Several techniques reduce fault simulation CPU time while improving convergence.

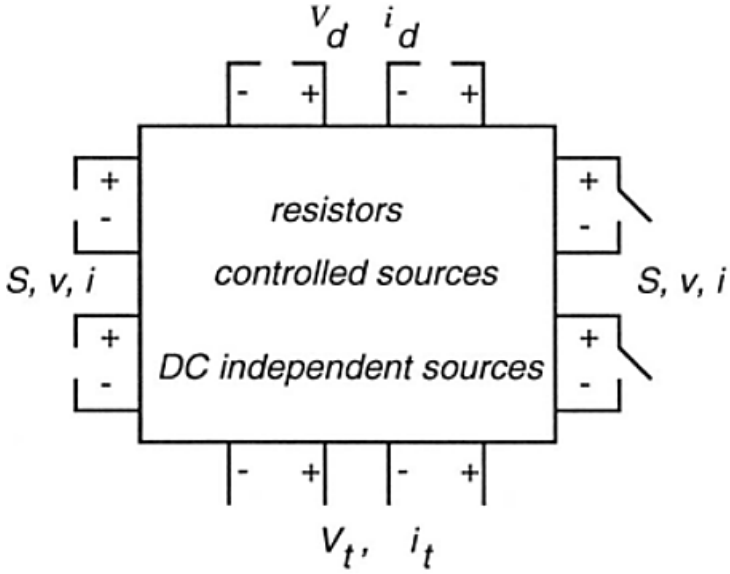
# DC Fault Simulation

## Complementary Pivot Method

1. They model the circuit linearity by ideal diodes. B *piecewise linear* (PWL) $I - V$ curve, usually a 2 or 3-segment approximation to the diode $I - V$ curve.

2. The transistor faults are modeled using switches, and these models are solved by an operations research method call *complementarity pivoting*. This method does not have the problem of Newton-Raphson iteration, which suffers from the extreme non-linearity coming from analog circuit and fault modeling.



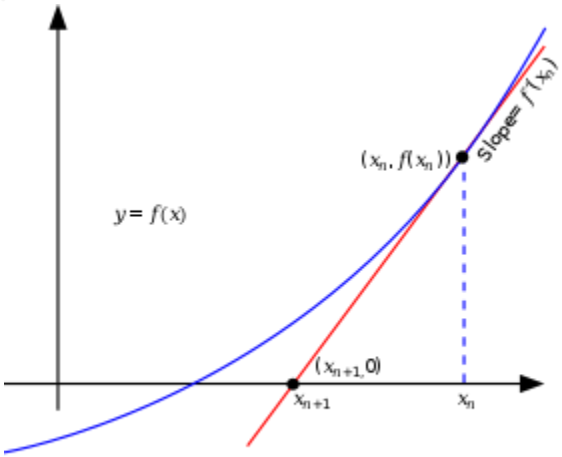

Four Kind of simulations per device including fault free

# DC Fault Simulation

Newton-Raphson iteration solves equations iteratively, starting from an initial point and iterating until the difference between and converges

For Solving f(x) =0 Start assuming initial solution as X0.
Iterate till error value within limits

$$x_1 = x_0 - \frac{f(x_0)}{f'(x_0)}$$



# DC Fault Simulation

## ONE-STEP RELAXATION VIA HOUSEHOLDER'S FORMULA

In *one-step relaxation,* the Newton-Raphson algorithm is operated for only one step using the good circuit solution as the starting point.

- Guess: $\mathbf{x}^{(0)}$
- Solve: $\mathbf{J}(\mathbf{x}^{(i)})(\mathbf{x}^{(k+1)} - \mathbf{x}^{(k)}) = -\mathbf{f}(\mathbf{x}^{(k)})$ for $k = 0, 1, 2, \ldots,$ until it converges, $\mathbf{J}(\mathbf{x}^{(k)})$ is the *Jacobian* matrix of $\mathbf{f}(\mathbf{x}^{(k)})$ and is calculated as:

$$\mathbf{J}(\mathbf{x}^{(k)}) = \frac{\partial \mathbf{f}(\mathbf{x}^{(k)})}{\partial \mathbf{x}^{(k)}} \qquad (11.2)$$

# Fault Simulation

cadence

Legato Reliability Solution for Analog Defects



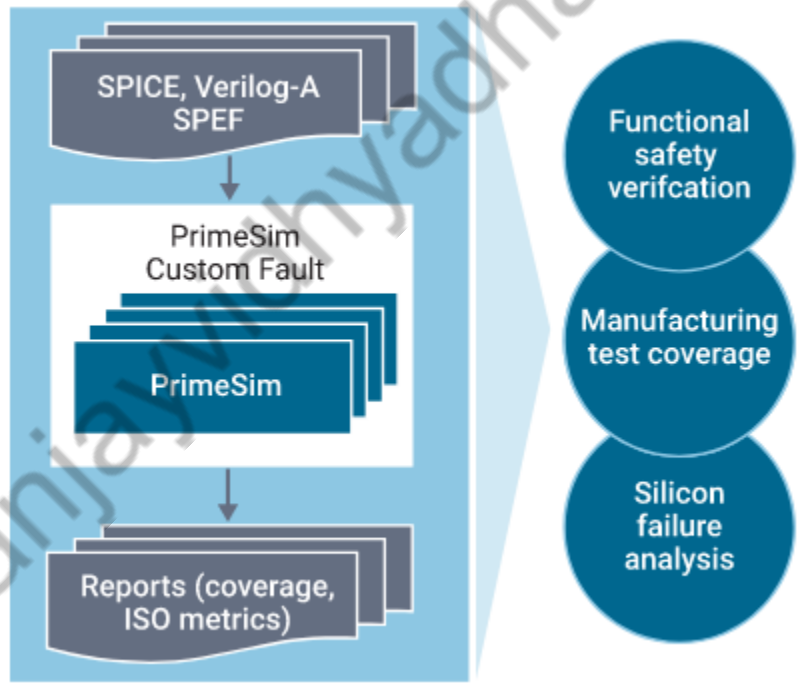
- Quickly identify potential sources of device manufacturing defects
- Multiple fault injection methods to optimize the simulation resolution and performance
- Calculate the test program's defect coverage based on simulation
- Choose the minimum set of tests to provide maximum fault coverage
- Supports different defect models (open, short, or bridge)
- Select defects based on criteria such as device type, parameter value, terminals, etc.
- Correct-by-construction fault identification
- Defect detection based on the production test limits (range, >, etc.)
- Customizable measurement test based on preprocessing, calibration, etc.

# Fault Simulation

SYNOPSYS®

**PrimeSim Custom Fault**

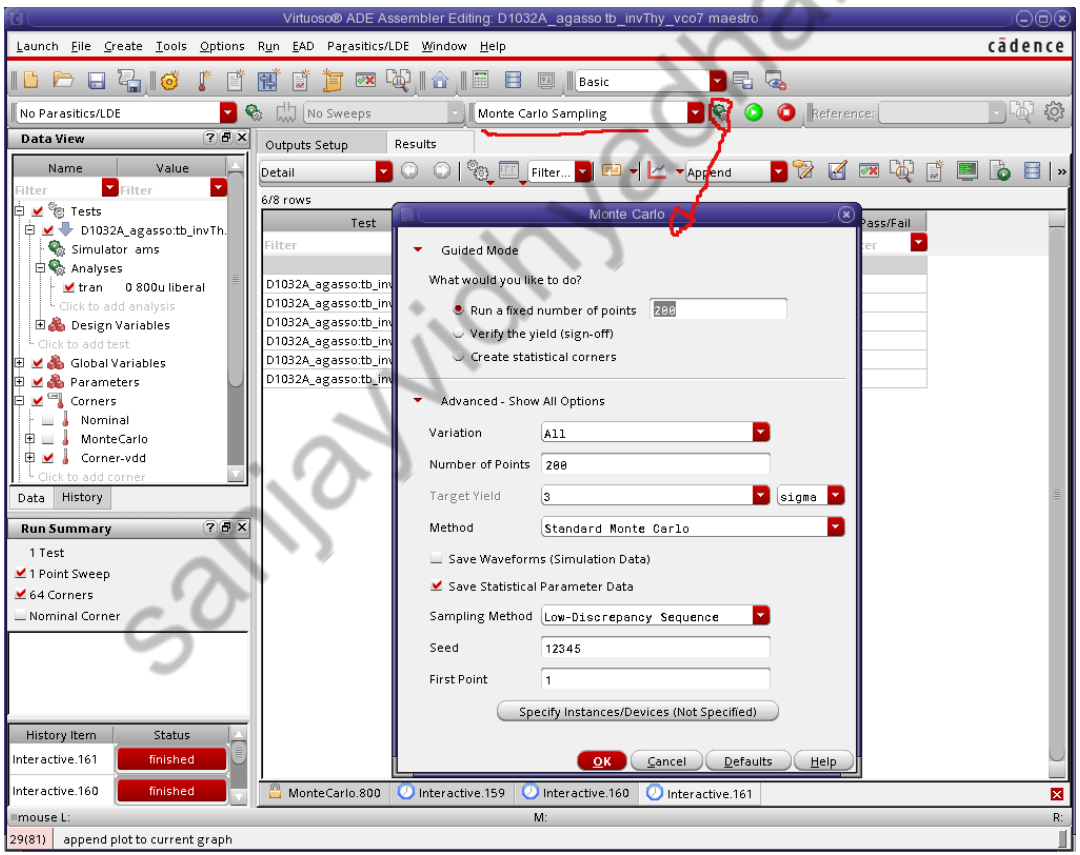
**Redefining Analog Fault Simulation for Functional Safety and Test Coverage Analysis**



# Fault Simulation

## Monte-Carlo Simulation

*Monte-Carlo* simulation has been extensively used in analog circuit and fault simulation. We perform the simulation for randomly-generated small variations in circuit component values. This is done because the actual IC manufacturing process will cause good circuits to deviate by such values. However, Monte-Carlo simulation is computationally expensive, unless the circuit is small with few statistical parameters.



# TPG Using Sensitivities

First-order *sensitivity* represents the relation between circuit *elements* and output *parameters*

We deduce component deviations by measuring various *output parameters*, and through sensitivity analysis and tolerance computation. They identify tests for catastrophic and soft (parametric) faults, for both single and multiple fault models. This ATPG method is intended for production testing applications.

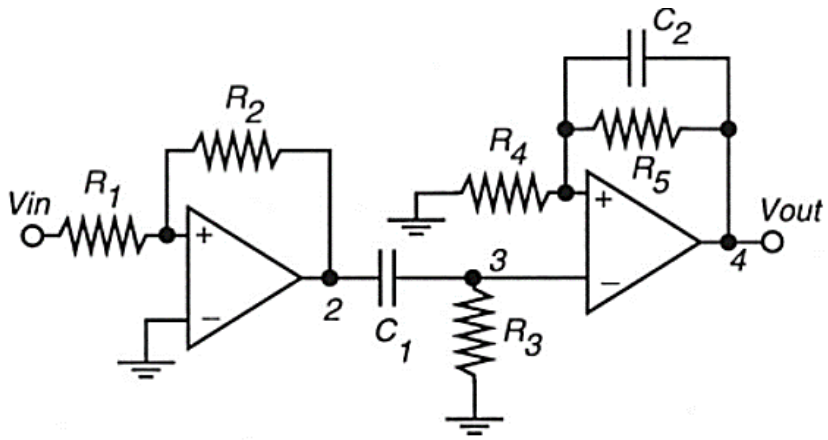
*Differential sensitivity* shows the effect of small variations in elements, and is defined as:

$$S_{x_i}^{T_j} = \frac{x_i}{T_j}\frac{\partial T_j}{\partial x_i} = \left.\frac{\Delta T_j/T_j}{\Delta x_i/x_i}\right|_{\Delta x_i \to 0}$$

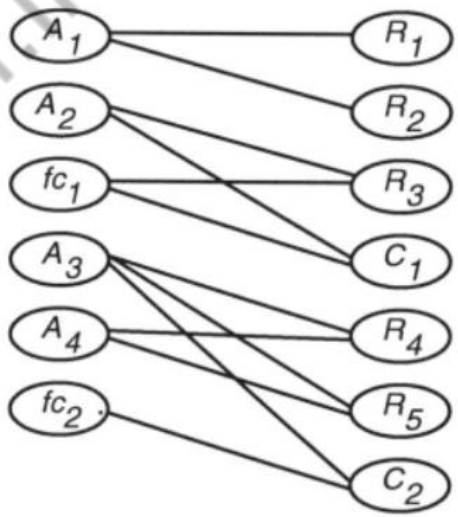
*Incremental sensitivity* shows the effect of large element variations, and is defined as:

$$\rho_{x_i}^{T_j} = \frac{x_i}{T_j} \times \frac{\Delta T_j}{\Delta x_j}$$

# TPG Using Sensitivities




*Bipartite graph of this incremental sensitivity matrix*




*Incremental sensitivity matrix*

$$\begin{bmatrix} -0.91 & 1 & 0 & 0 & 0 & 0 & 0 & A_1 \\ 0 & 0 & 0.58 & 0.38 & 0 & 0 & 0 & A_2 \\ 0 & 0 & -0.91 & -0.89 & 0 & 0 & 0 & fc_1 \\ 0 & 0 & 0 & 0 & -0.96 & 0.48 & -0.48 & A_3 \\ 0 & 0 & 0 & 0 & -0.97 & -0.97 & 0 & A_4 \\ 0 & 0 & 0 & 0 & 0 & -0.88 & -0.91 & fc_2 \\ R_1 & R_2 & C_1 & R_3 & R_4 & R_5 & C_2 & \backslash \end{bmatrix}$$

$A_1$: *First stage gain.*
$A_3$: *AC voltage gain of third part.*
$A_4$: *DC voltage gain of third part.*

$A_2$: *High-pass filter gain at known frequency.*
$fc_1$: *High-pass filter cutoff frequency.*
$fc_2$: *Low-pass filter cutoff frequency.*

# TPG Using Sensitivities

**Test Method**

1. Perform sensitivity analysis.

2. Build the circuit bipartite graph.

3. Compute tolerances (relative deviations) of every circuit element. The relative deviation of fault-free elements comes from circuit data sheets. The tolerance of a faulty element is computed as a (*min*, *max*) pair.

4. Construct the bipartite optimization graph.

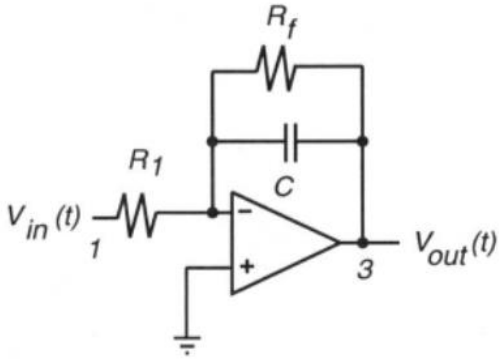
5. Select parameters (or performances) to be measured during testing using the *simplex* optimization method.

6. Perform testability analysis of the circuit by computing the analog fault coverage. For given tolerance values, analog *fault coverage* is the ratio of detected faults over all possible faults.

7. Improve the circuit testability with *design for testability* (DFT) hardware. They add new POs to increase observability of untestable elements.

# TPG Using Signal Flow Graphs

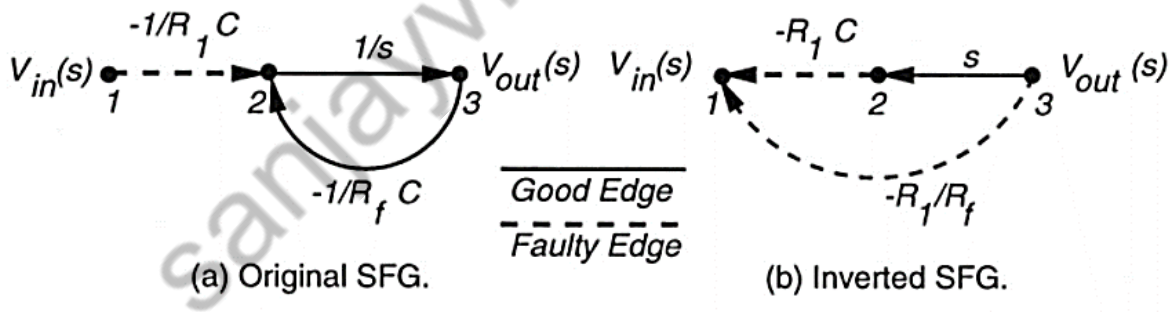
Ramadoss and Bushnell proposed *structural* analog circuit testing, where they generate test waveforms that verify which component values or ratios of component values are within specifications. This method shortens tester time per circuit, by reducing the number of measurements.




$$Z_f = \frac{R_f \frac{1}{sC}}{R_f + \frac{1}{sC}} = \frac{R_f}{sR_fC + 1}$$

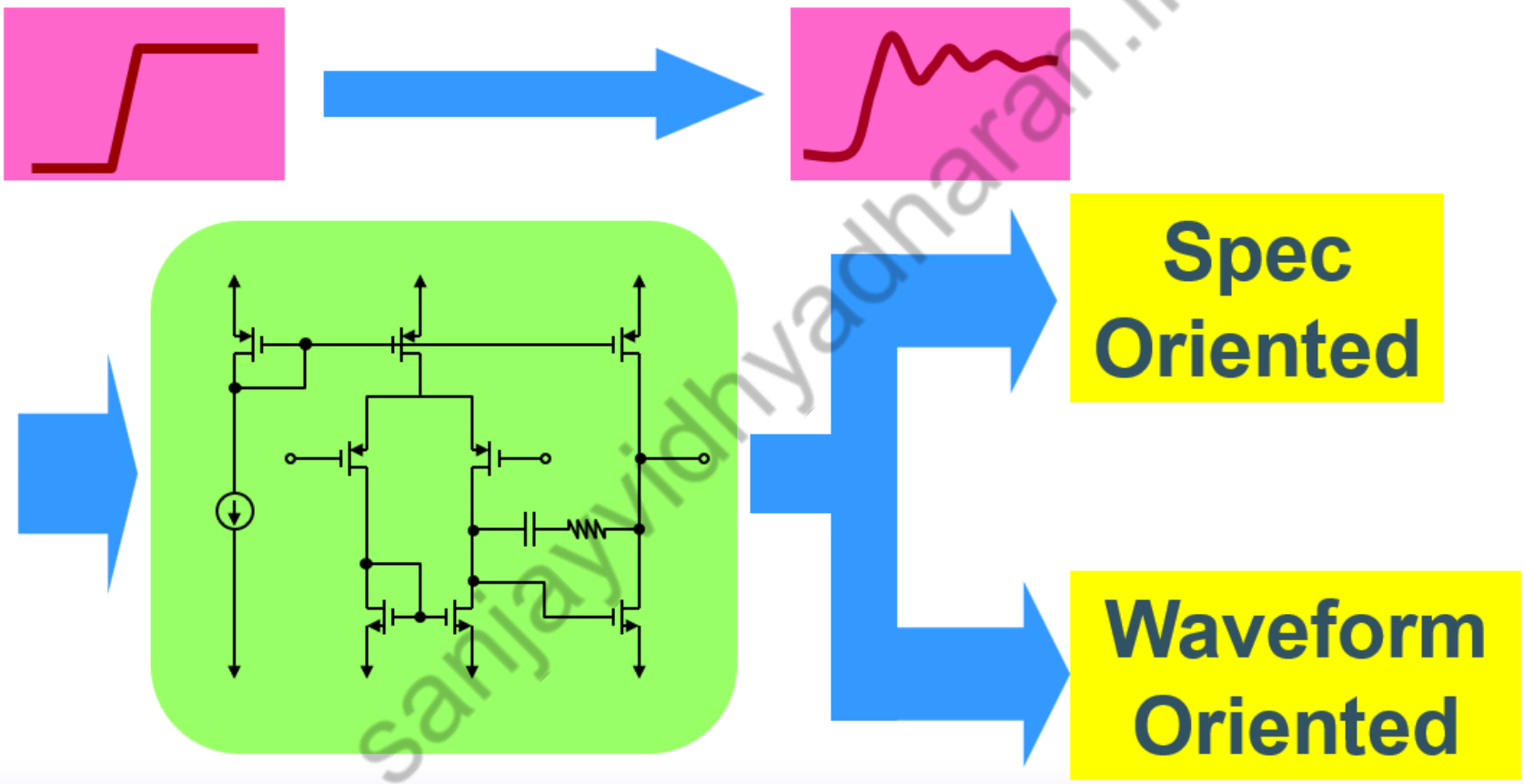
$$\frac{V_{in}(s)}{R_1} = \frac{-V_{out}(s)}{Z_f}$$

$$V_{out}(s) = -V_{in}(s)\frac{Z_f}{R_1} = -V_{in}(s)\frac{1}{sR_1C + \frac{R_1}{R_f}}$$




SFG inversion can calculate the parameter tolerances that the circuit components must meet (during manufacturing), in order to ensure that the analog output waveforms remain within specifications. This new method avoids specifying analog components to tighter parametric tolerances than is necessary, and this reduces cost.

# Analog Testing



# Analog Testing

## Specification Oriented Test

### OP777/OP727/OP747–SPECIFICATIONS

**ELECTRICAL CHARACTERISTICS** (@ $V_S$ = 5.0 V, $V_{CM}$ = 2.5 V, $T_A$ = 25°C unless otherwise noted.)

Analog Devices, Inc.™

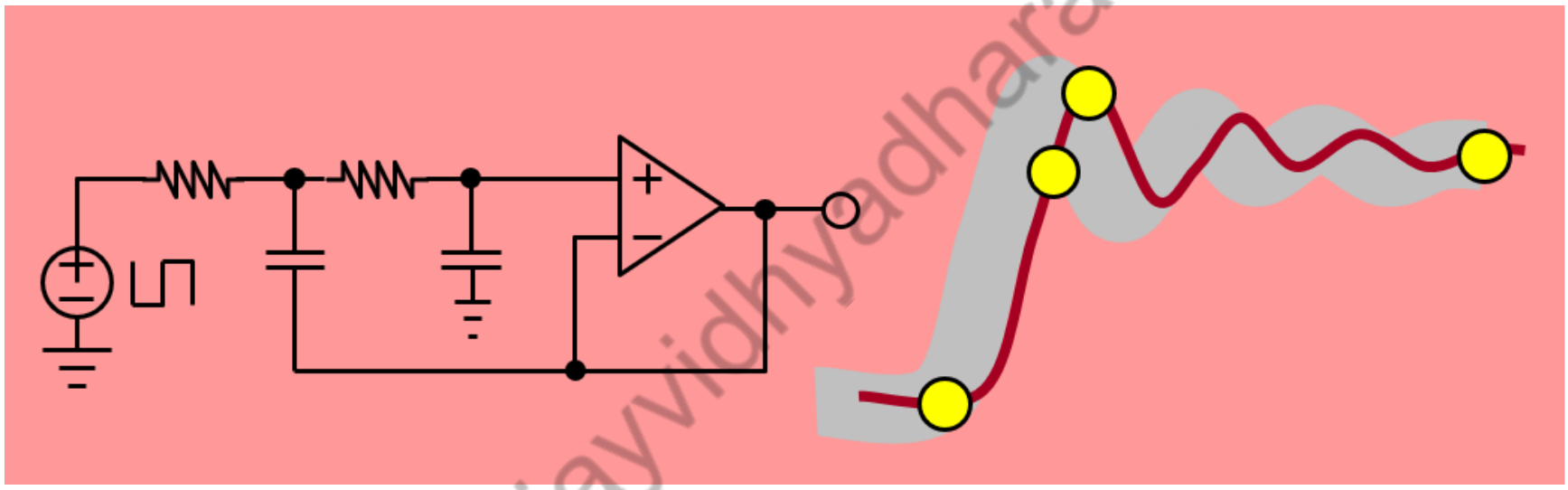
| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| INPUT CHARACTERISTICS | | | | | | |
| Offset Voltage OP777 | $V_{OS}$ | +25°C < $T_A$ < +85°C | | 20 | 100 | µV |
| | | –40°C < $T_A$ < +85°C | | 50 | 200 | µV |
| Offset Voltage OP727/OP747 | | +25°C < $T_A$ < +85°C | | 30 | 160 | µV |
| | | –40°C < $T_A$ < +85°C | | 60 | 300 | µV |
| Input Bias Current | $I_B$ | –40°C < $T_A$ < +85°C | | 5.5 | 11 | nA |
| Input Offset Current | $I_{OS}$ | –40°C < $T_A$ < +85°C | | 0.1 | 2 | nA |
| Input Voltage Range | | | 0 | | 4 | V |
| Common-Mode Rejection Ratio | CMRR | $V_{CM}$ = 0 V to 4 V | 104 | 110 | | dB |
| Large Signal Voltage Gain | $A_{VO}$ | $R_L$ = 10 kΩ, $V_O$ = 0.5 V to 4.5 V | 300 | 500 | | V/mV |
| Offset Voltage Drift OP777 | $\Delta V_{OS}/\Delta T$ | –40°C < $T_A$ < +85°C | | 0.3 | 1.3 | µV/°C |
| Offset Voltage Drift OP727/OP747 | $\Delta V_{OS}/\Delta T$ | –40°C < $T_A$ < +85°C | | 0.4 | 1.5 | µV/°C |
| OUTPUT CHARACTERISTICS | | | | | | |
| Output Voltage High | $V_{OH}$ | $I_L$ = 1 mA, –40 °C to +85 °C | 4.88 | 4.91 | | V |
| Output Voltage Low | $V_{OL}$ | $I_L$ = 1 mA, –40 °C to +85 °C | | 126 | 140 | mV |
| Output Circuit | $I_{OUT}$ | $V_{DROPOUT}$ < 1 V | | ±10 | | mA |
| POWER SUPPLY | | | | | | |
| Power Supply Rejection Ratio | PSRR | $V_S$ = 3 V to 30 V | 120 | 130 | | dB |
| Supply Current/Amplifier OP777 | $I_{SY}$ | $V_O$ = 0 V | | 220 | 270 | µA |
| | | –40°C < $T_A$ < +85°C | | 270 | 320 | µA |
| Supply Current/Amplifier OP727/OP747 | | $V_O$ = 0 V | | 235 | 290 | µA |
| | | –40°C < $T_A$ < +85°C | | 290 | 350 | µA |
| DYNAMIC PERFORMANCE | | | | | | |
| Slew Rate | SR | $R_L$ = 2 kΩ | | 0.2 | | V/µs |
| Gain Bandwidth Product | GBP | | | 0.7 | | MHz |
| NOISE PERFORMANCE | | | | | | |
| Voltage Noise | $e_{np}$-p | 0.1 Hz to 10 Hz | | 0.4 | | µV p-p |
| Voltage Noise Density | $e_n$ | f = 1 kHz | | 15 | | nV/√Hz |
| Current Noise Density | $i_n$ | f = 1 kHz | | 0.13 | | pA/√Hz |

NOTES
Typical specifications: >50% of units perform equal to or better than the "typical" value.
Specifications subject to change without notice.

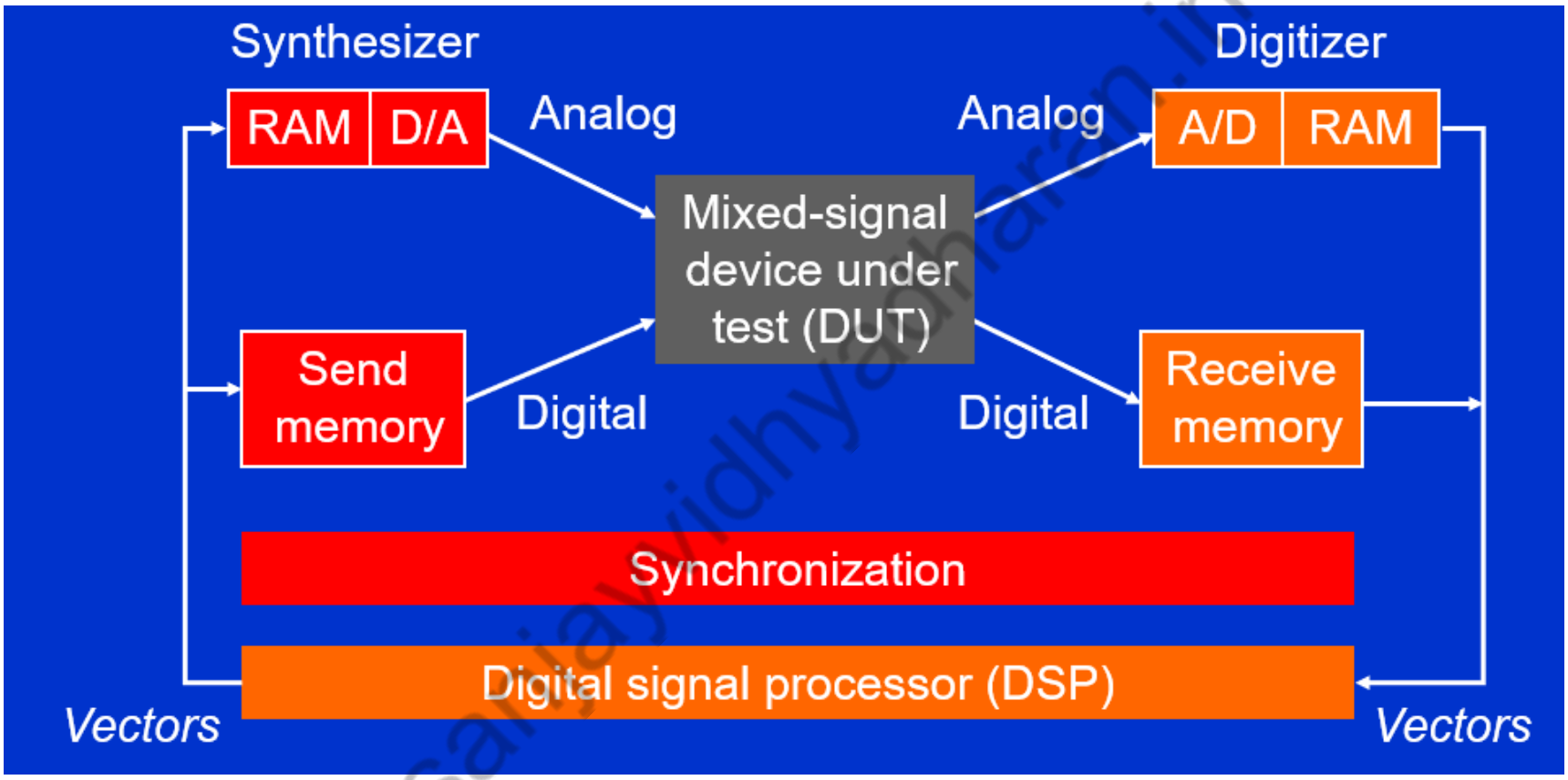
# Analog Testing

## Waveform Oriented Test

Compare waveform to the simulated ones



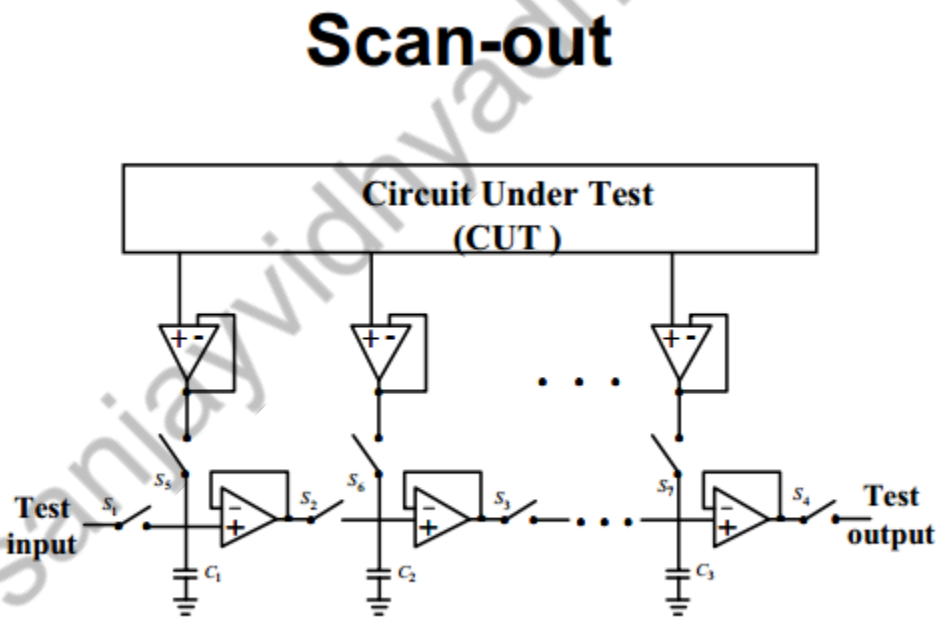
# DSP-Based Mixed-Signal Test



# Scan-in/Scan-out

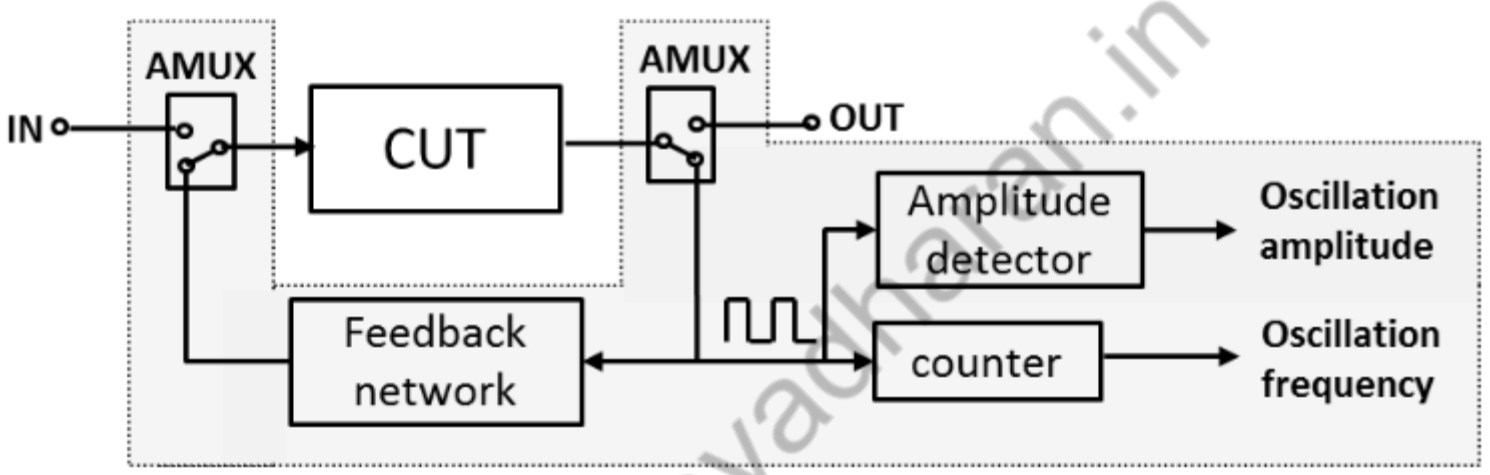
A chain of capacitors and voltage-follower buffers form an analog shift register.

• The test input signal can be scanned in from input pins to the internal nodes and the test results can be scanned out from the internal nodes to output pins



# BIST for Analog Circuits

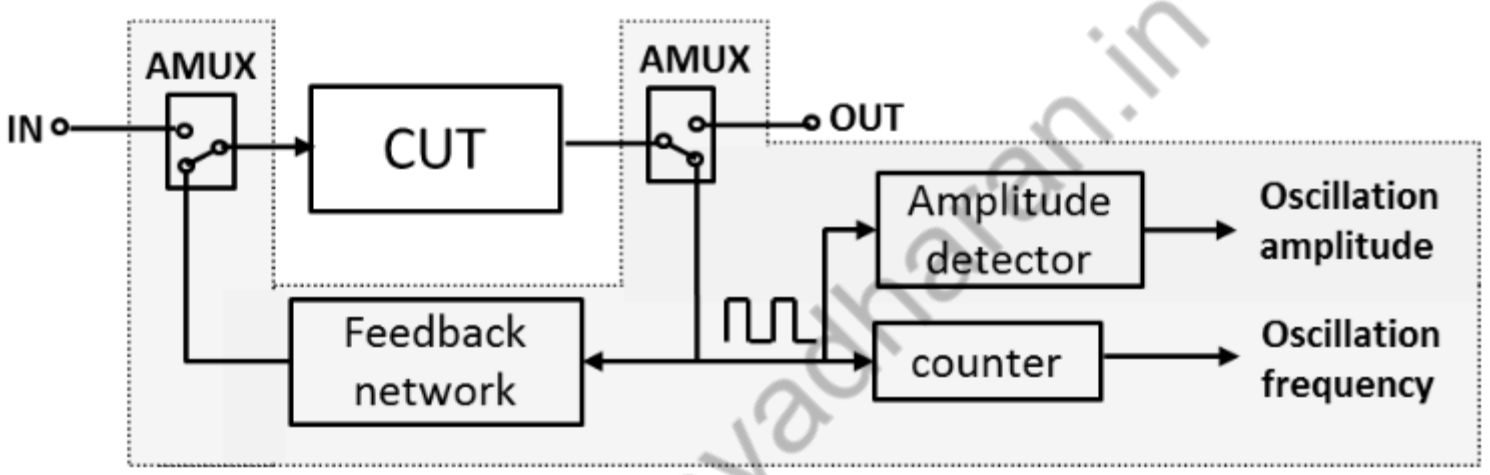
Oscillation-based test architecture.




A first well-known example is the generic oscillation test where the CUT is reconfigured to oscillate by connecting it into a positive feedback loop, as shown in Fig. The oscillation frequency and magnitude are information-rich signatures that can be used to gain insight about the functionality of the CUT and to detect abnormal behavior

# BIST for Analog Circuits

Oscillation-based test architecture.

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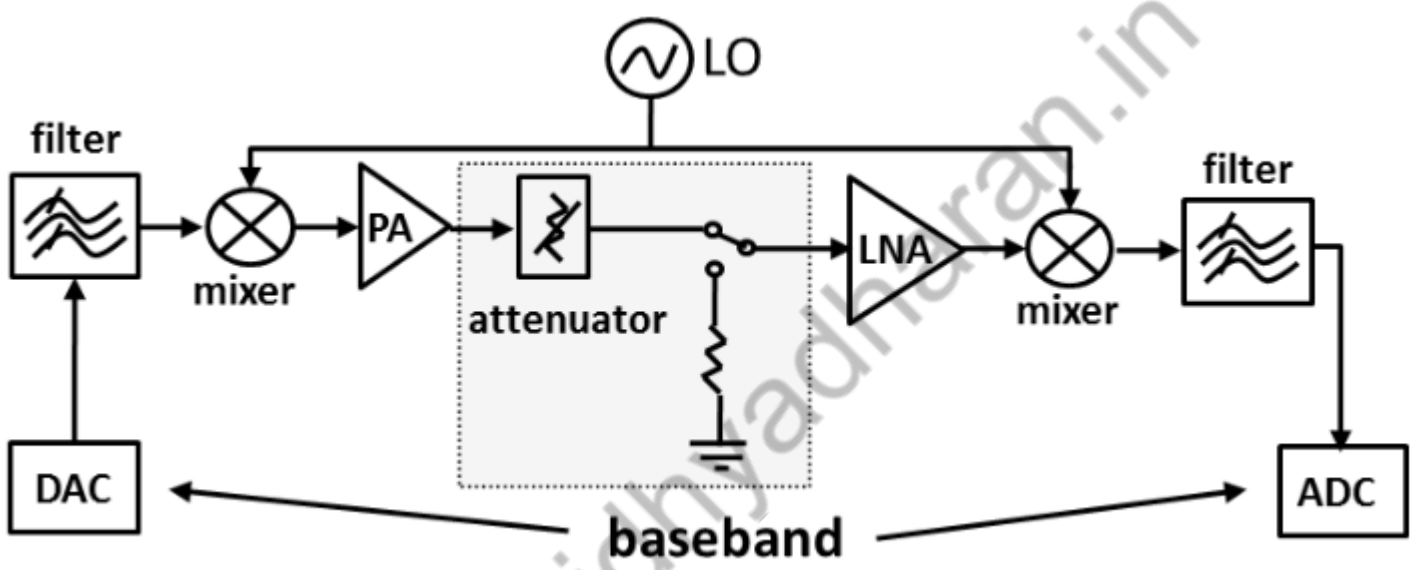
# BIST for Analog Circuits

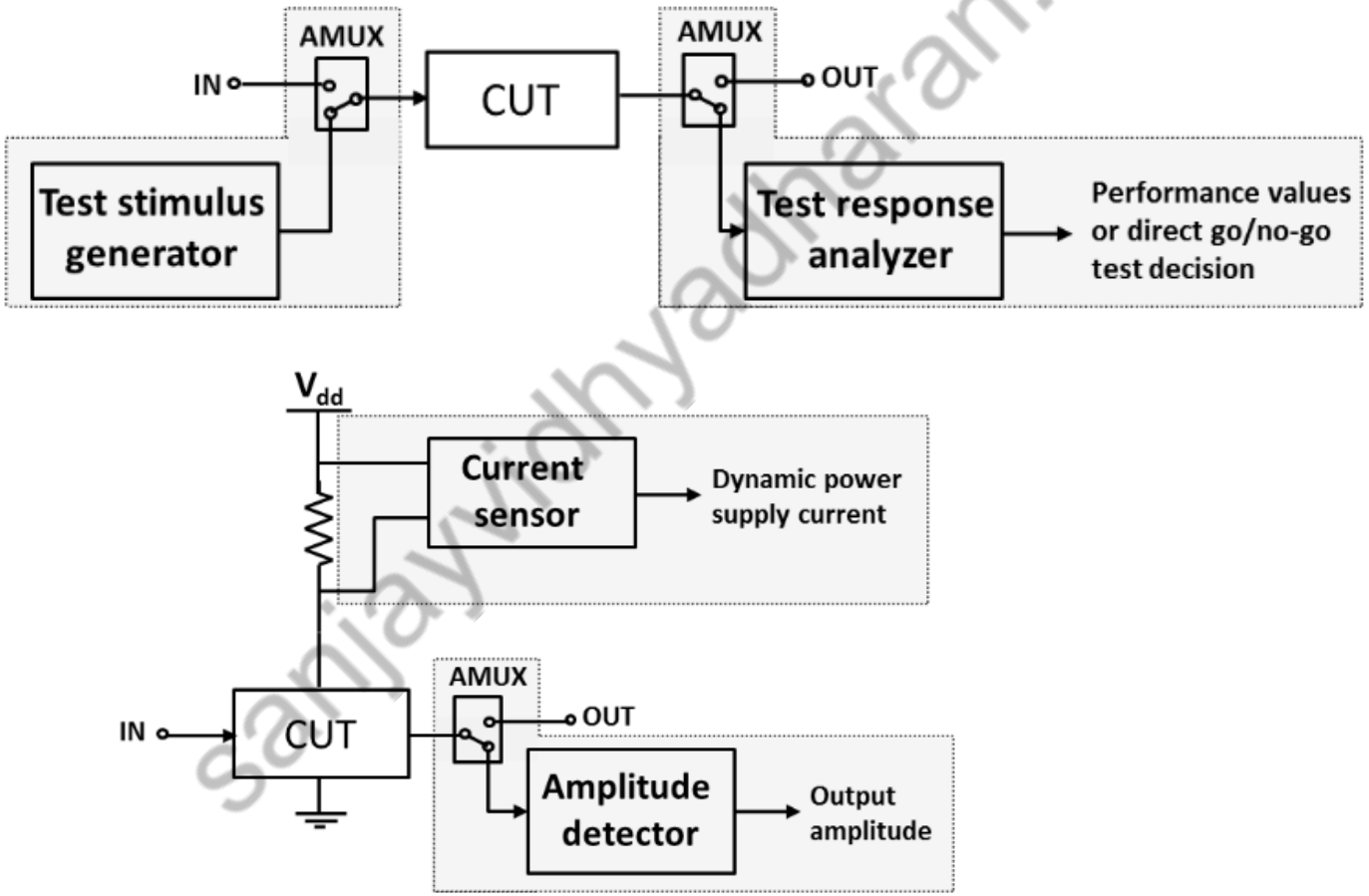
Loop-back test for RF transceivers.




A second example is the loop-back test for RF transceivers where the test signals are generated in the baseband and the transmitter's output is switched to the receiver's input through an attenuator to analyze the test response also in the baseband

# BIST for Analog Circuits

BIST employing an on-chip test stimulus generator and an on-chip test response analyzer



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1. “Essentials of Electronic Testing, for Digital, Memory and Mixed-Signal VLSI Circuits”, Michael L. Bushnell and Vishwani D. Agrawal,–Kluwer Academic Publishers (2000).

2. Video lectures by Professor James Chien-Mo Li
Lab. of Dependable Systems Graduate Institute of Electronics Engineering
National Taiwan University
https://www.youtube.com/watch?v=yfcoKOUV5DM&list=PLvd8d-SyI7hjk_Ci0zpTqImAtpEjdK5JF&index=1

3. NPTEL Lectures
https://www.youtube.com/watch?v=M8VEEaYwlQ&list=PLbMVogVj5nJTClnafWQ9FK2nt3cGG8kCF&index=31

# Thankyou