Testability of VLSI

Lecture 11:
Design for Testability

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Design for Testability

Observability & Controllability

- *Observability*: ease of observing a node by watching external output pins of the chip
- *Controllability*: ease of forcing a node to 0 or 1 by driving input pins of the chip
- Combinational logic is usually easy to observe and control
- Finite state machines can be very difficult, requiring many cycles to enter desired state
  – Especially if state transition diagram is not known to the test engineer

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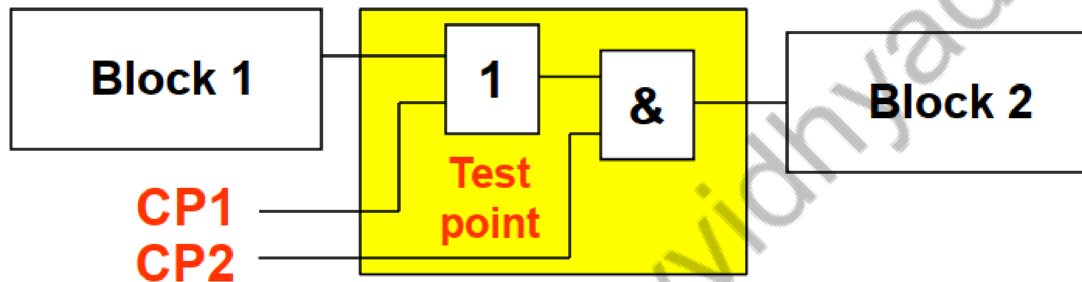
Ad Hoc Design for Testability

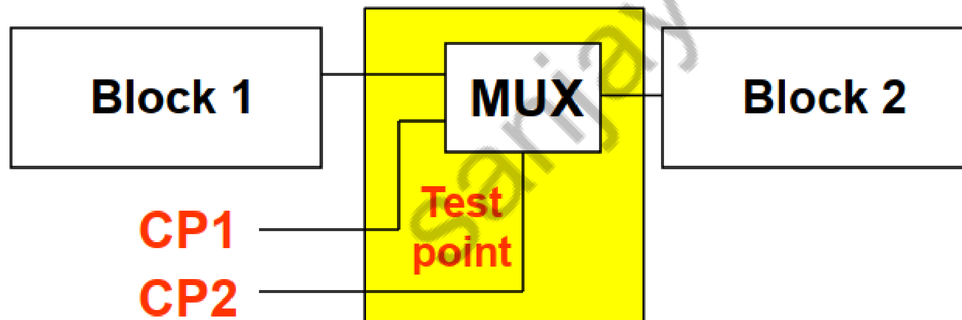
Method of Test Points:

Block 1 is not observable,
Block 2 is not controllable

Improving controllability:



Normal working mode:
CP1 = 0, CP2 = 1
Controlling Block 2 with 1:
CP1 = 1, CP2 = 1
Controlling Block 2 with 0:
CP2 = 0



Normal working mode:
CP2 = 0
Controlling Block 2 with 1:
CP1 = 1, CP2 = 1
Controlling Block 2 with 0:
CP1 = 0, CP2 = 1

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Ad Hoc Design for Testability

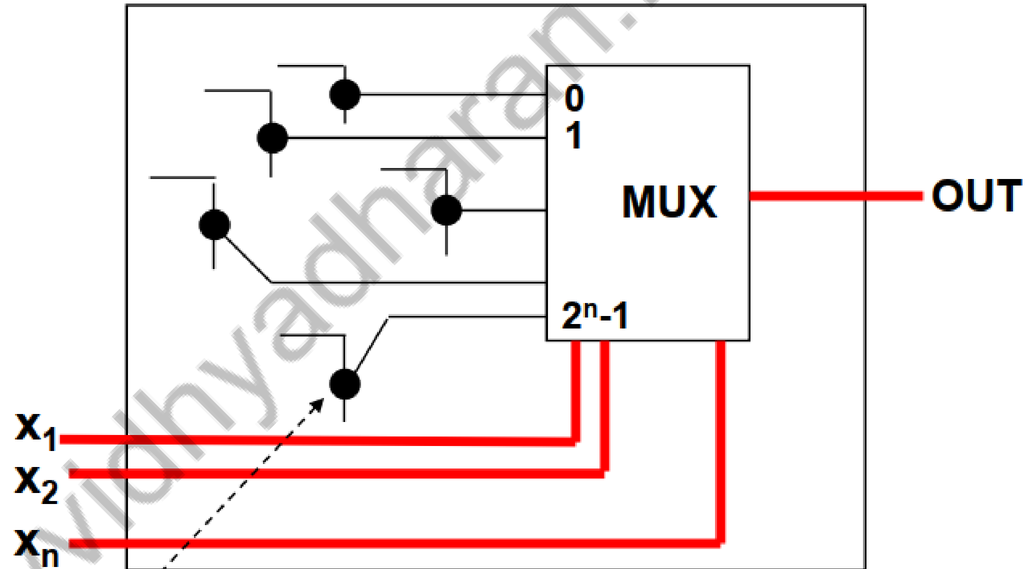
Multiplexing monitor points:

To reduce the number of output pins for observing monitor points, multiplexer can be used:

2^n observation points are replaced by a single output and n inputs to address a selected observation point

Disadvantage:

Only one observation point can be observed at a time



MUX

Number of additional pins: $(n + 1)$
Number of observable points: $[2^n]$

Advantage: $(n + 1) << 2^n$

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Ad Hoc Design for Testability

Multiplexing monitor points:

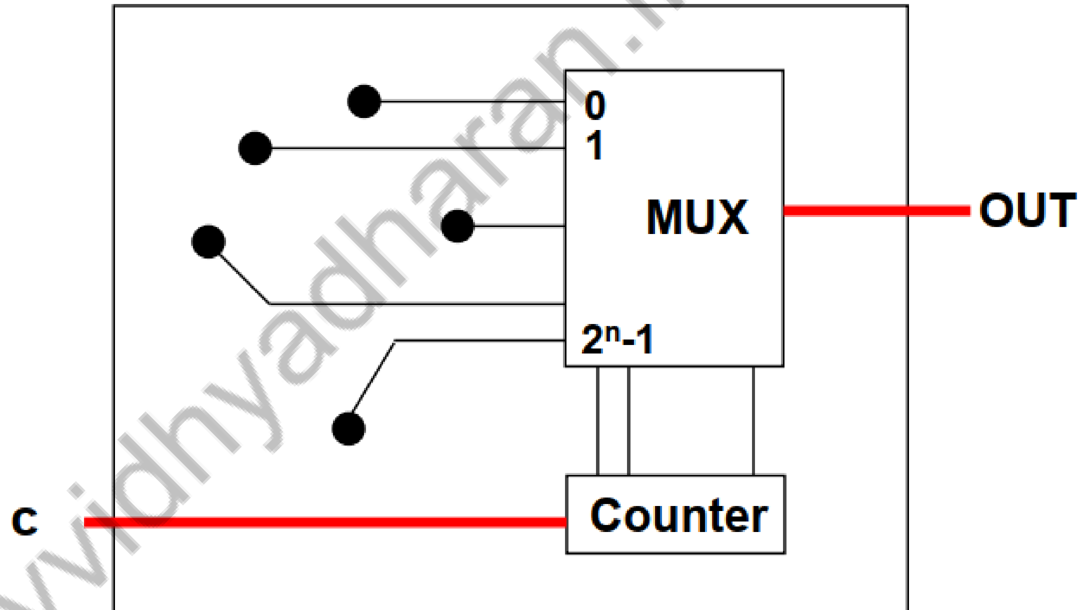
To reduce the number of output pins for observing monitor points, multiplexer can be used:

To reduce the number of inputs, a counter (or a shift register) can be used to drive the address lines of the multiplexer

Disadvantage:

Only one observation point can be observed at a time

Reset for counter?



Number of additional pins: 2

Nmber of observable points: $[2^n]$

Advantage: $2 < n << 2^n$

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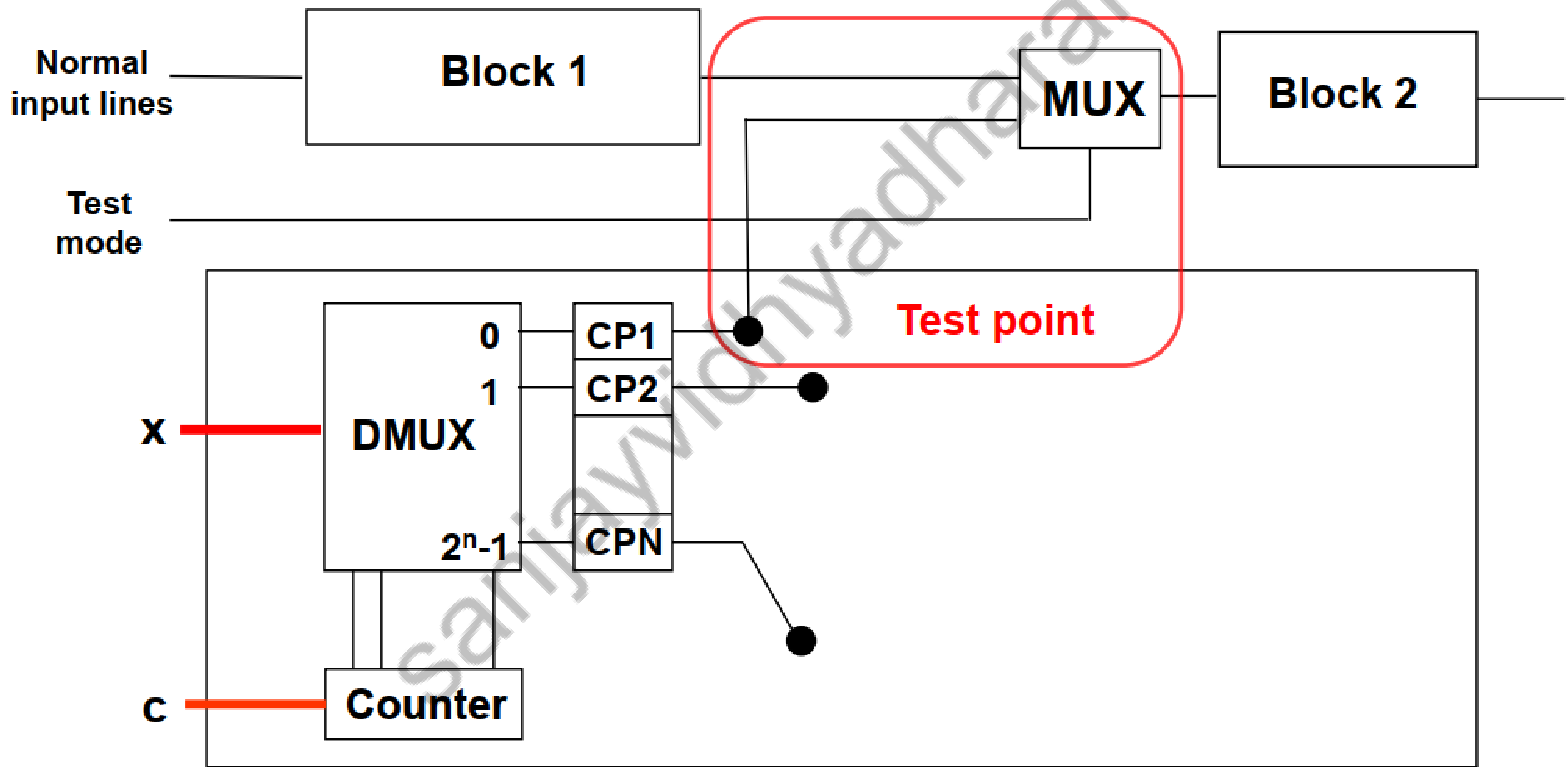
Ad Hoc Design for Testability

Demultiplexer for implementing control points:



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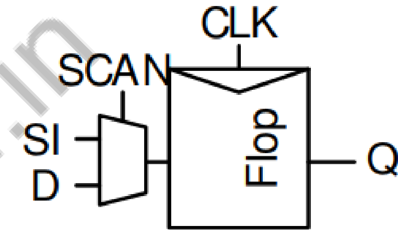
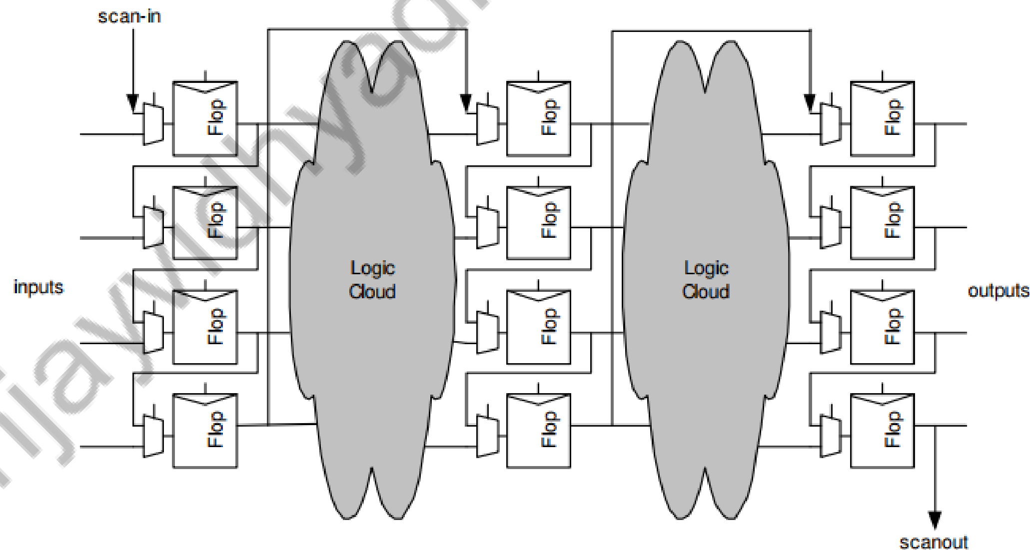
Scan Design

- Convert each flip-flop to a scan register
  - Only costs one extra multiplexer
- Normal mode: flip-flops behave as usual
- Scan mode: flip-flops behave as shift register



- Contents of flops can be scanned out and new values scanned in



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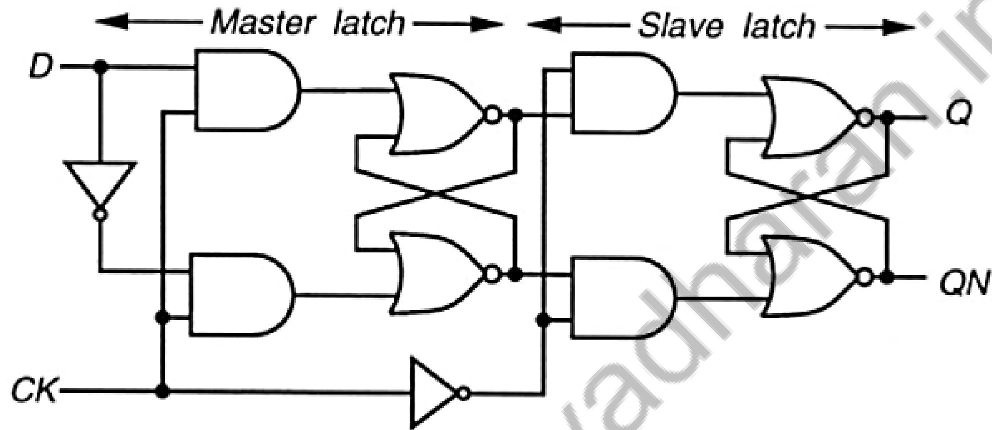
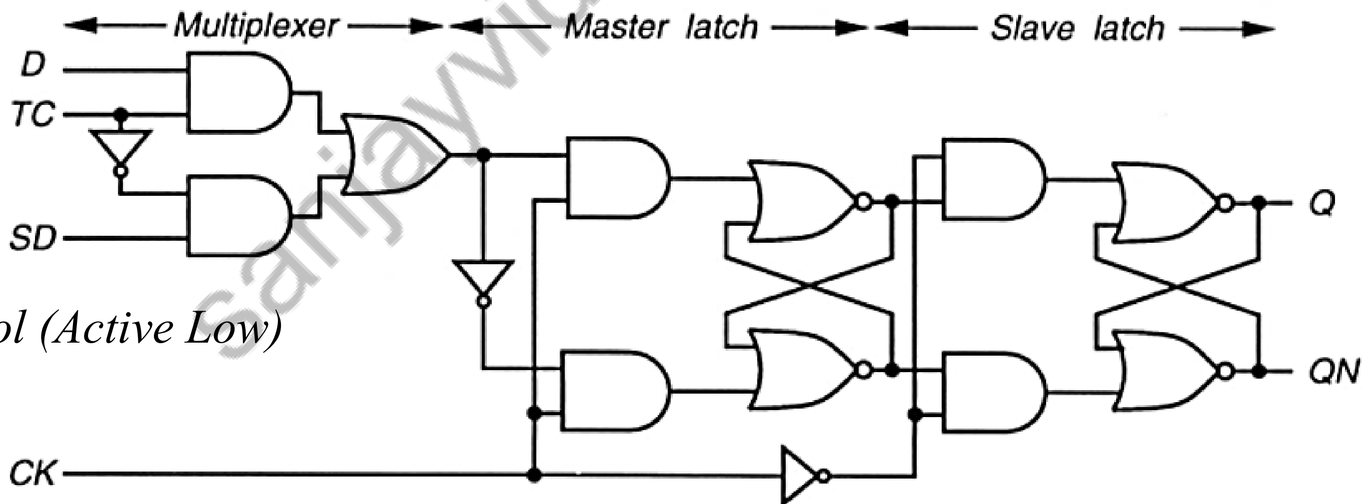
Scan Design

D flip-flop



A single-clock scan flip-flop



TC Test control (Active Low)
SD Scan data

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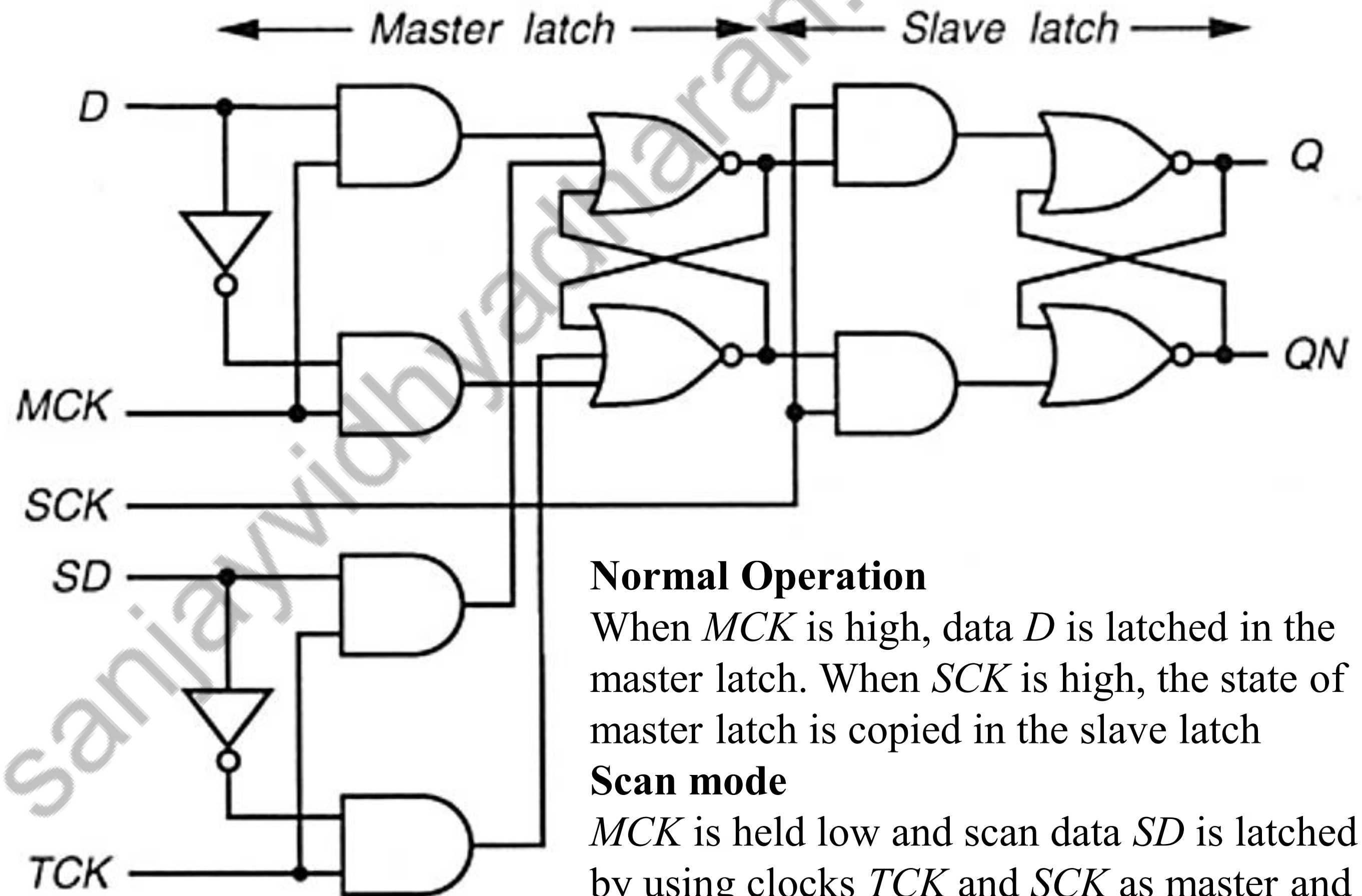
Scan Design

A two-clock scan flip-flop

Level-sensitive scan design (LSSD), uses two non-overlapping clock signals.



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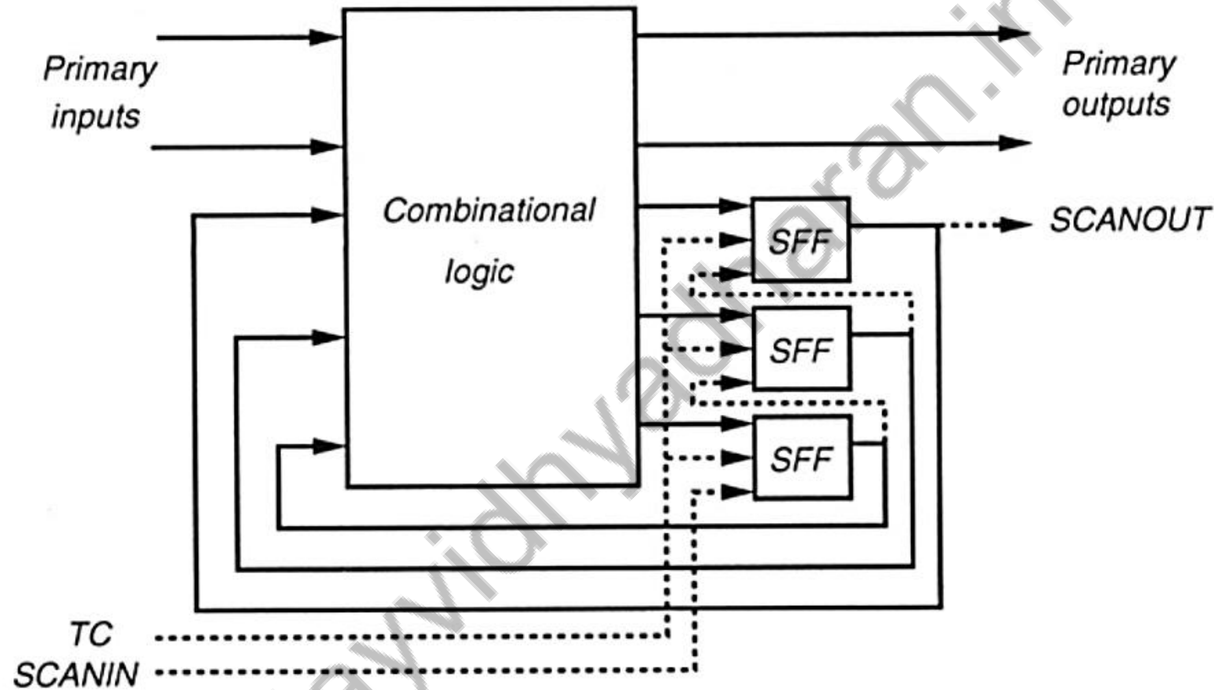
Normal Operation

When *MCK* is high, data *D* is latched in the master latch. When *SCK* is high, the state of master latch is copied in the slave latch

Scan mode

MCK is held low and scan data *SD* is latched in by using clocks *TCK* and *SCK* as master and slave clocks

Scan Design



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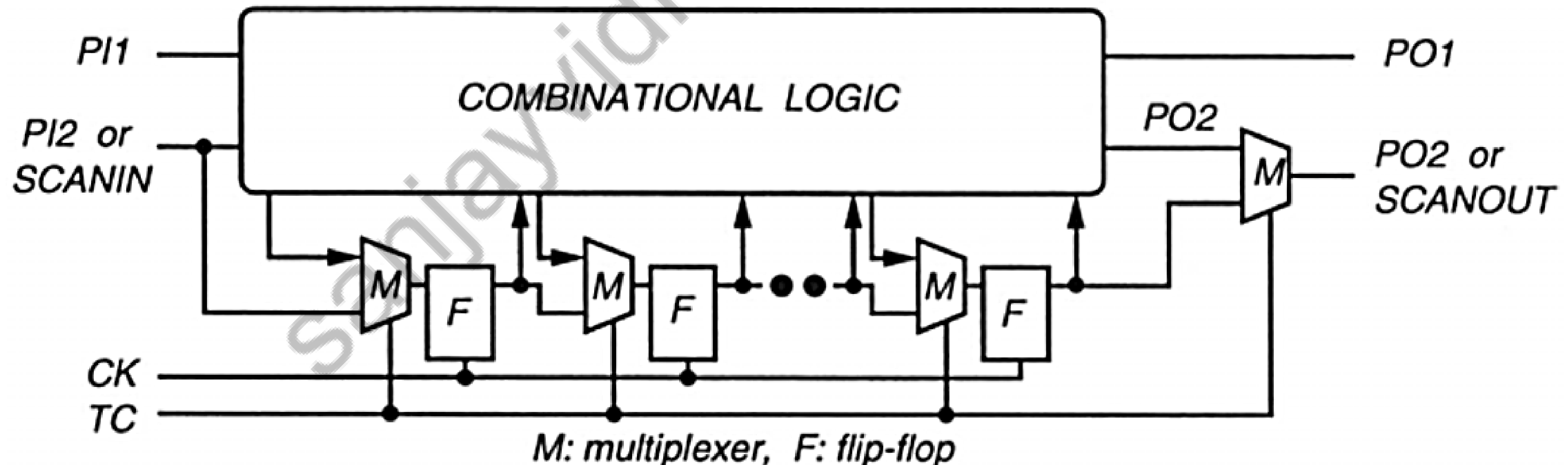
The *SD* input of one SFF is supplied by another new primary input *SCANIN.* All SFFs are chained by connecting the *Q* output of one SFF to the *SD* input of the next SFF. The *Q* output of the last SFF in the chain is a new primary output *SCANOUT.* This design has the advantage of reducing the effort of test generation. The wiring added for scan design shown in broken lines. Especially for the case of *full-scan*, where all flip-flops are scanned,

Scan Design Rules

R-1: *Only D-type master-slave flip-flops should be used.* This rule prohibits the use of other types of flip-flops (JK, toggle, etc.) or other forms of asynchronous logic (unclocked RS latches, combinational feedback elements.)

R-2: *At least one primary input pin must be available for test.* In general, flip-flops can be connected as multiple scan registers, each of which will require a scan-in and a scan-out terminal. If extra pins are not available, then any normal primary input can be used as scan-in and any primary output pin can be multiplexed as scan-out.



Scan design with a single extra pin for *test control* (*TC*)

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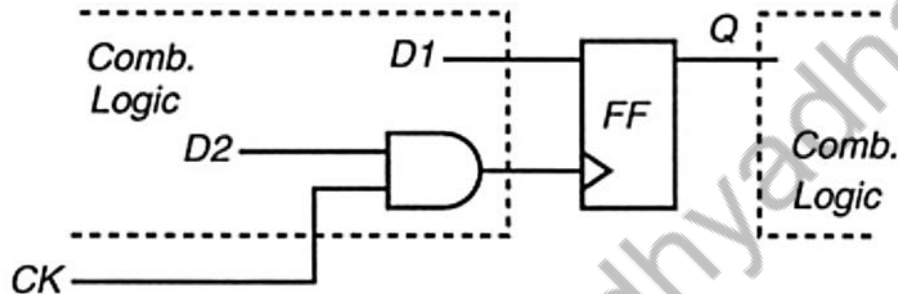
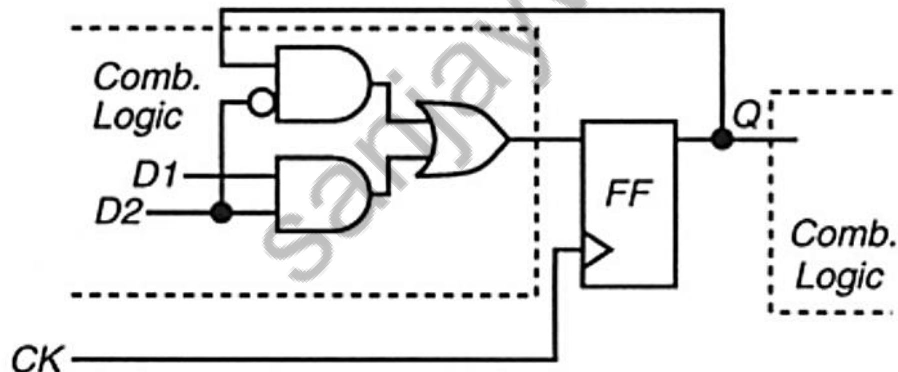
Scan Design Rules

R-3: *All flip-flop clocks must be controllable from primary inputs. This rule is necessary for flip-flops to function as a scan register. Some violations of this rule, if they exist, can be removed by a simple work-around.*



(a) Gated-clock: Violation of Rule R-3.



(b) A modification to eliminate gating of clock.

The two circuits are functionally identical, and the modified circuit satisfies the rule R-3. It can be converted into scan design as described in the previous section.

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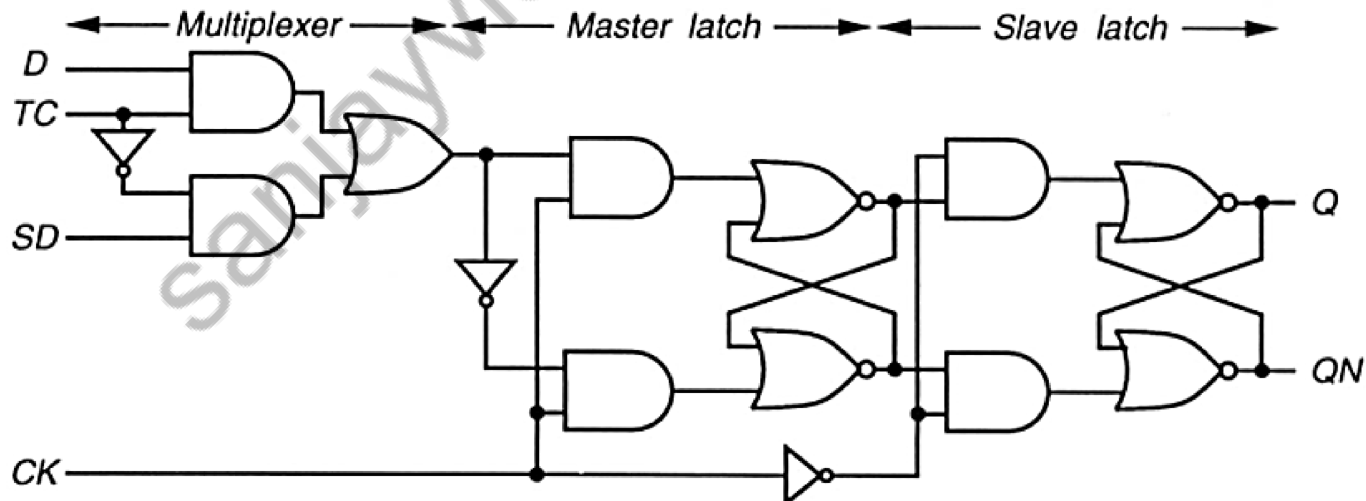
Tests for Scan Circuits

Testing of scan circuits is done in two phases.

1.The first phase tests the scan register by a *shift test.* The circuit is set in scan mode by setting *TC* = 0. All flip-flops now form a shift register between *SCANIN* and *SCANOUT.* A *toggle sequence,* 00110011 . . ., of length $n_{sf} + 4$ where n_{sf} is the total number of flip-flops, is applied at *SCANIN.* The toggle sequence is clocked through the shift register using the normal clock signal. This sequence produces all four transitions, and in each flip-flop and shifts the outputs to the observable output *SCANOUT.* It covers most, if not all, single stuck-at faults in the flip-flops, and verifies the correctness of the shift operation of the scan register.



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Tests for Scan Circuits

In the second phase of testing, single stuck-at faults in the combinational logic are targeted. A combinational ATPG program is used to generate test vectors assuming that all flip-flop outputs are completely controllable and all flip-flop inputs are observable.

$$\text{Scan test length} = n_{sff} + 4 + (n_{sff} + 1)n_{comb} + n_{sff}$$
$$= (n_{comb} + 2)n_{sff} + n_{comb} + 4 \quad \text{clock periods}$$

where n_{comb} is the number of combinational test vectors and n_{sff} is the number of flip-flops in the scan register ($n_{sff} > 0$). We assume that all flip-flops form a single scan register. Such a design can lead to a long test time. For example, in a circuit with 2,000 flip-flops if all faults of the combinational logic are tested by $n_{comb} = 500$ vectors, then the complete scan test will run for 1,004,504 clock periods.

Several Pipelined Combinational circuits will be tested parallelly

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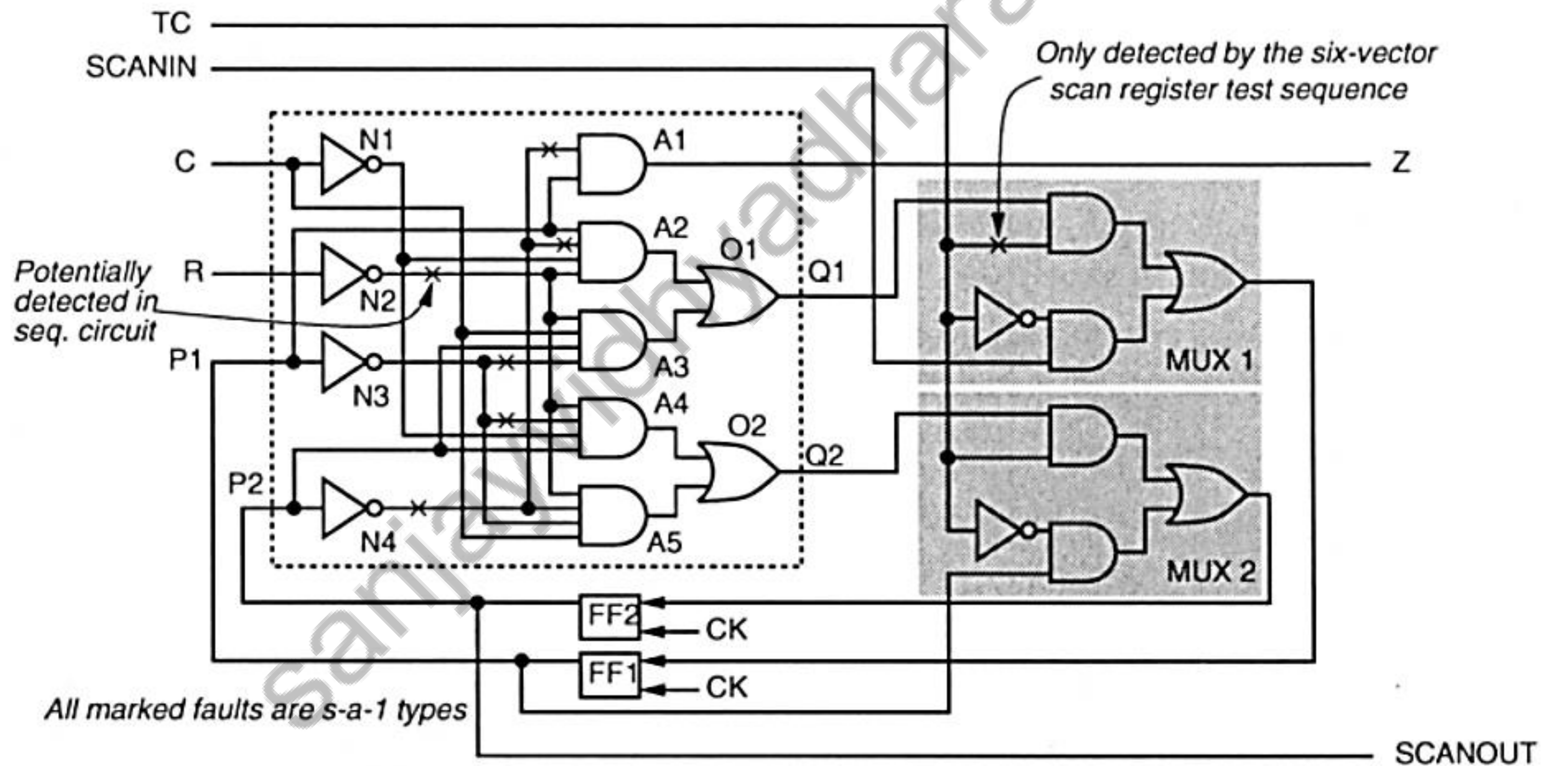
Tests for Scan Circuits

Example: A modulo-3 counter

When R = 1, *the counter is set to its initial state 00. For R* = 0 *and C* = 1, *the state advances as with each clock. The output Z becomes* 1 *only for the state* 10 *and remains* 0 *for all other states. When R* = *C* = 0, *the counter retains its state.*



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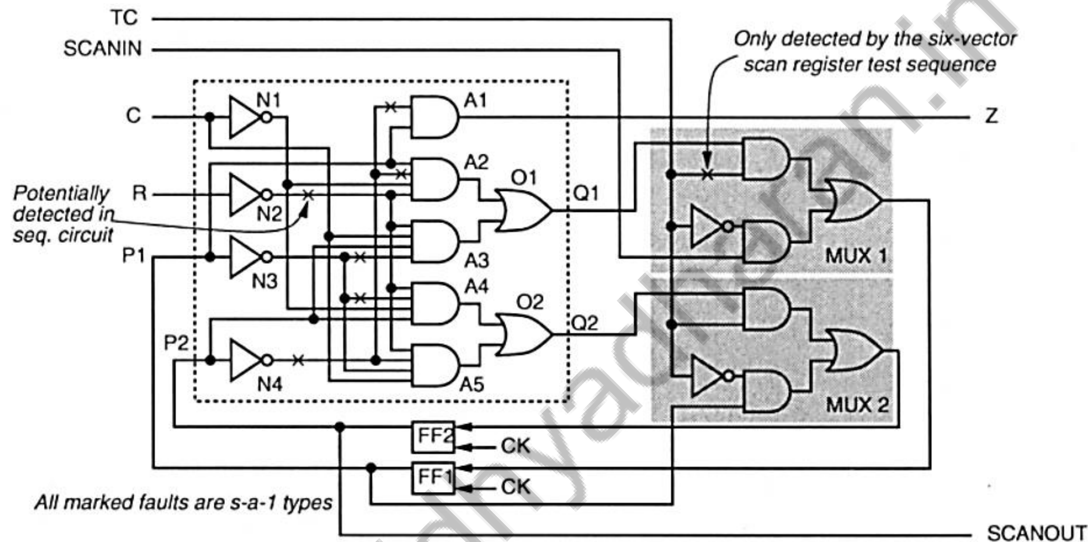
Tests for Scan Circuits

Example: A modulo-3 counter



A sequential ATPG program generated 35 vectors to cover 36 of 42 faults in the non-scan circuit. Few faults are not detectable due to cyclic feedback.
The ATPG program produced 12 vectors for the combinational circuit in the dotted-line box, having four inputs, C, R, P1, and P2, and three outputs, Z, Q1, and Q2
Converted to scan sequences including a six-vector shift register test, these gave a scan test sequence of 44 vectors.

$$\text{Scan test length} = n_{sff} + 4 + (n_{sff}+1)n_{comb} + n_{sff}$$
$$= (n_{comb}+2)n_{sff} + n_{comb} + 4 \ \text{clock periods}$$

(12+2)2+12+4=44

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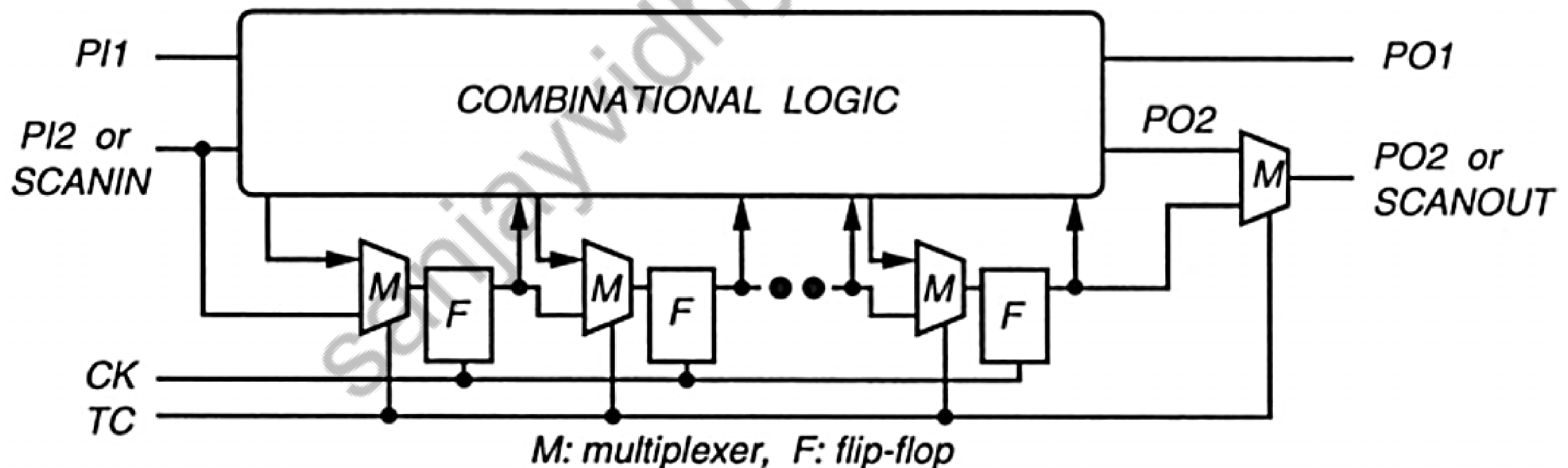
Multiple Scan Registers

To reduce the time of scan test, sometimes flip-flops are arranged in multiple scan registers. Each scan register requires separate *SCANIN* and *SCANOUT* pins. If extra pins are not available, added fanouts from normal primary input pins can provide *SCANIN* signals to scan chains. This is possible because the normal primary inputs and *SCANIN* are never simultaneously used Similarly, the *SCANOUT* signals can be multiplexed with the normal primary output pins under the control of the test control (*TC*) signal. In general, multiple scan registers can have varying lengths. The length of scanin and scanout sequences depends on the longest register.



M: multiplexer, F: flip-flop

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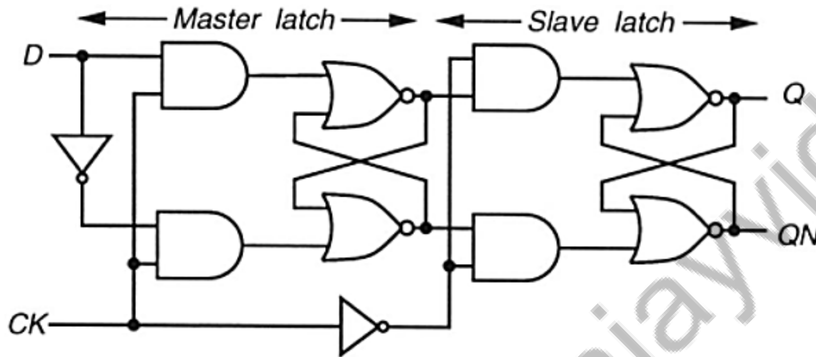
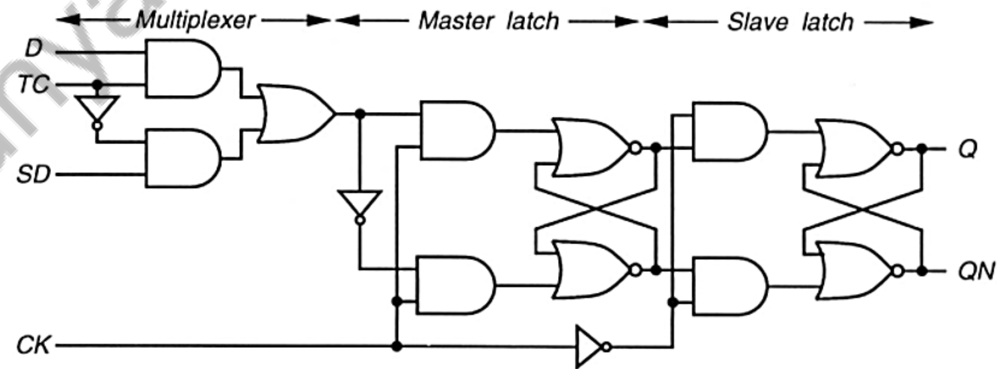
Overheads of Scan Design

The use of scan design has two types of penalties. The scan hardware increases

1. the chip size (area overhead) and
2. slows the signals down (performance overhead.)

1. Gate overhead. Suppose a circuit has gates and flip-flops (each FF consisting of 10 gates). Assume that original flip-flops are replaced single-clock scan flip-flop. Then each flip-flop adds an overhead of four gates (used in the multiplexer.) The total gate overhead is computed as:





$$\text{Gate overhead of scan} = \frac{4 \times n_{sff}}{n_g + 10n_{ff}} \times 100\%$$

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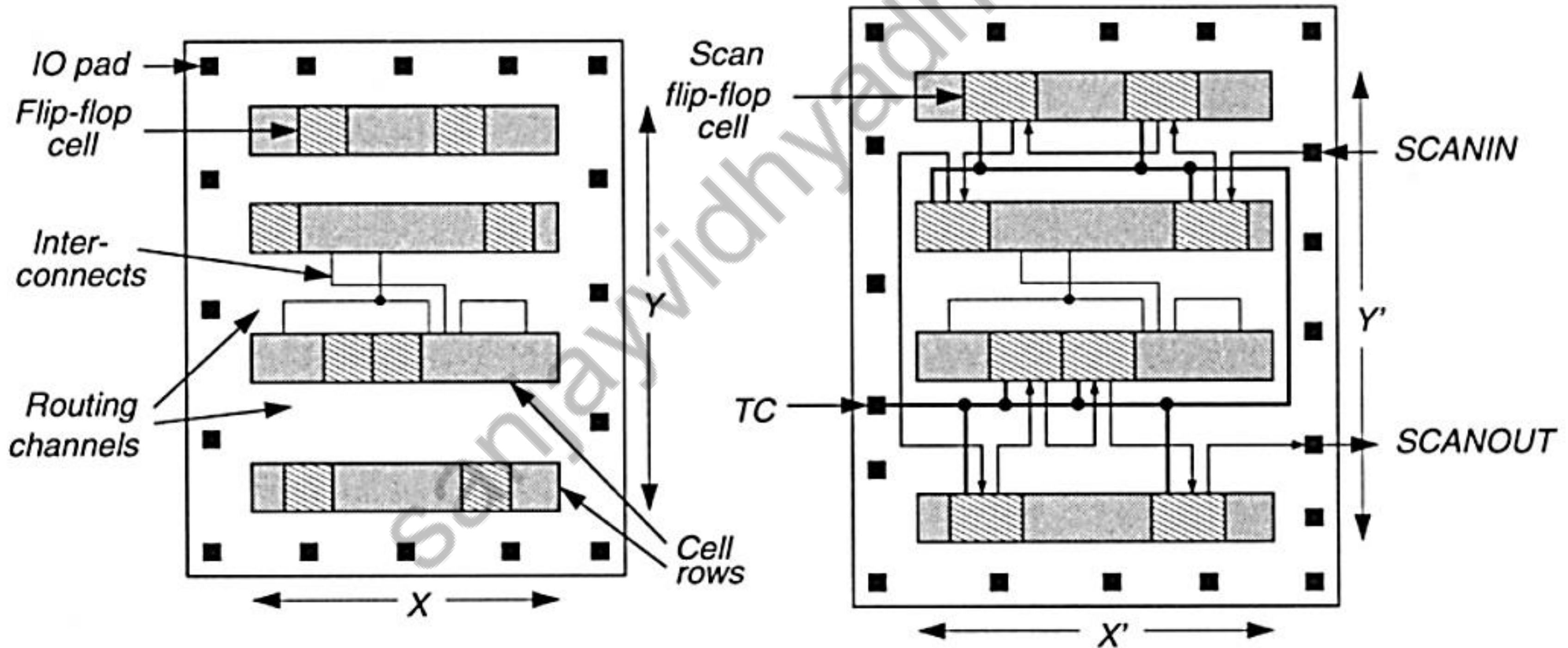
Overheads of Scan Design

2. Area overhead. Scan design requires a significant amount of routing that can impact the chip area. The test control signal (TC) is routed to all flip-flops and the output of each flip-flop is routed to the scan data (SD) input of the next flip-flop in the scan register chain. The impact of scan routing on the chip area increase can be reduced by: (a) flip-flop placement on the layout for optimum routing and (b) selecting the flip-flop order in the scan chain



(a) Standard-cell layout.

(b) Optimized scan layout.

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Overheads of Scan Design

y: Track width in length units.

C: Combined width of combinational cells.

S: Combined width of sequential (flip-flop) cells in the non-scan circuit.

s: Fraction of cell area under flip-flops, $s = S/(C + S)$.

α: Fractional width increase of a scan flip-flop over a non-scan cell.

r: Number of cell rows or routing channels (assumed to be equal.)

β: Fraction of active area occupied by routing channels (routing fraction.)

T: Cell height in number of tracks.

$$X = \frac{C+S}{r} \quad \text{and} \quad X' = \frac{C+S+\alpha S}{r}$$

The combined height of a cell row and one adjoining routing channel is $T/(1-\beta)$ tracks.

$$r = Y(1-\beta)/(yT)$$

$$Y' = Y + ry = Y + Y(1-\beta)/T$$

$$\begin{aligned}\text{Area overhead of scan} &= \frac{X'Y' - XY}{XY} \times 100\% \\ &= \left[(1+\alpha s)\left(1+\frac{1-\beta}{T}\right) - 1\right] \times 100\% \\ &\approx \left(\alpha s + \frac{1-\beta}{T}\right) \times 100\%\end{aligned}$$

Depending on the cell height (T) that is around 8-10 tracks, this part can contribute up to about 10% in a cell-dominant chip.

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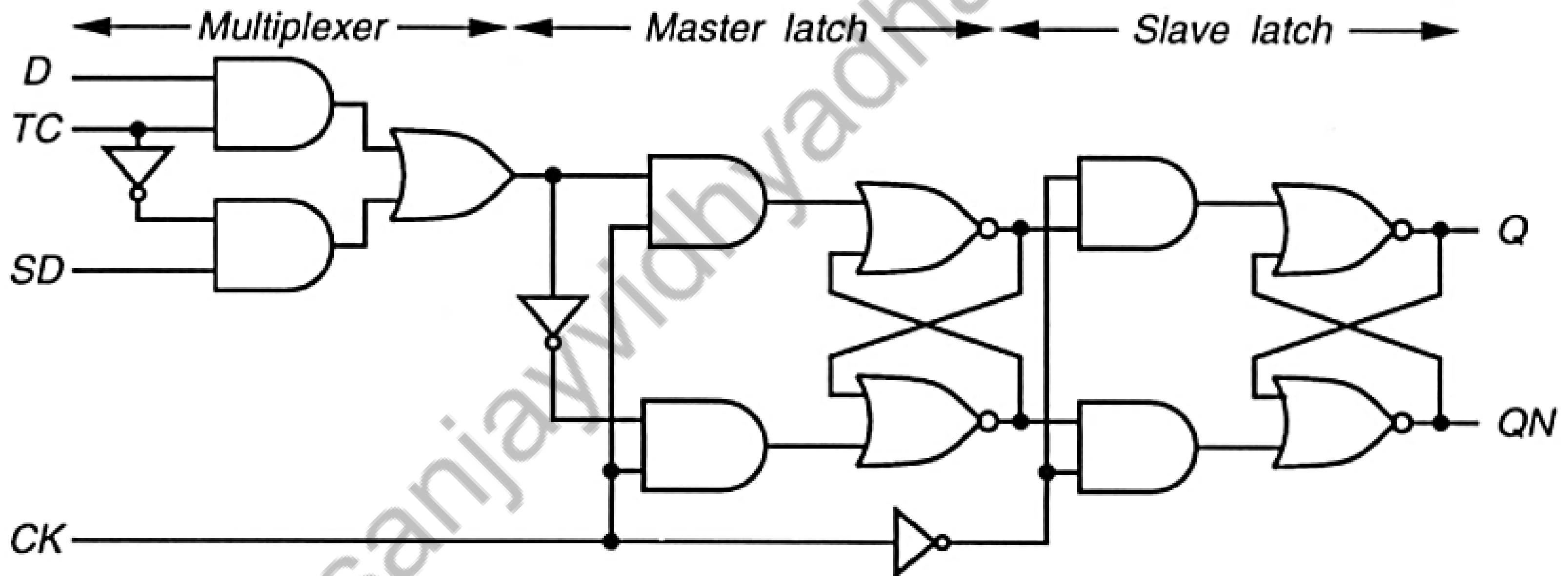
Overheads of Scan Design

3. ***Performance overhead***. Scan design also has a performance overhead. The multiplexer of the scan flip-flop adds delay equivalent to two gate-delays in all clocked paths. In addition, flip-flop outputs have one extra fanout, which increases the capacitive loading of the signal. In general, scan design can reduce the clock speed by 5 to 10%.



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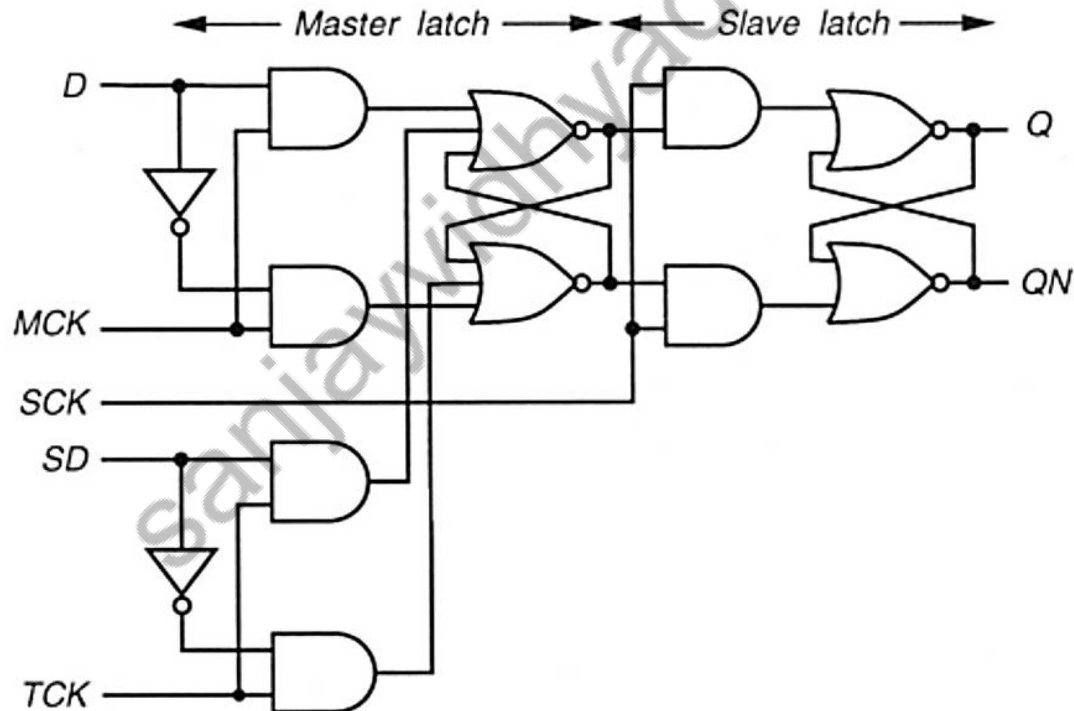
Overheads of Scan Design

*3. **Performance overhead**.* The two-clock design does not insert any gate delay in the data path. This results in reduced performance penalty. However, the routing of the two system clocks (*MCK* and *SCK*) and the test clock (*TCK*) requires extreme care. Relative skews between these clock signals should be carefully controlled for the correct operation in both normal and scan modes.



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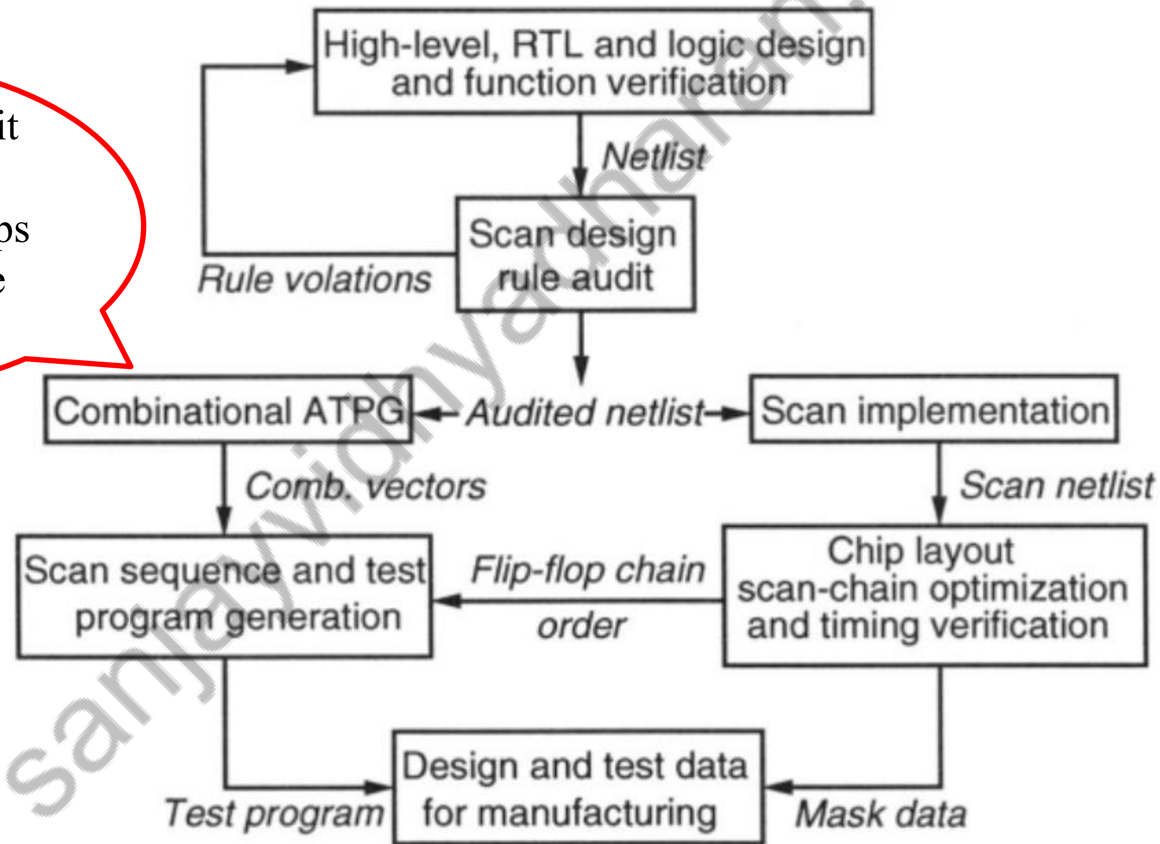
Design Automation

1. The **full-scan design** is considered the *best* DFT discipline. It can be completely automated using commercially available design tools

combinational circuit
netlist is generated
by removing flip-flops
and clocks from the
audited netlist



A flow-chart of automated scan design.

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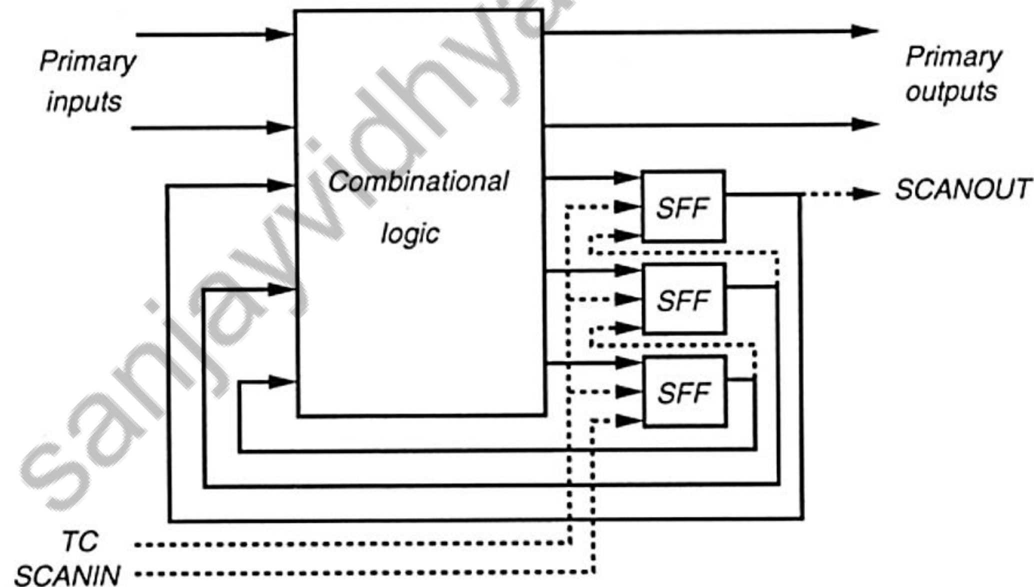
Design Automation

The **full-scan design:** **Physical Design and Timing Verification of Scan**

1.Very small delay in scan path. Because there is no logic gate in the scan path, signal propagation between two consecutive flip-flops of the scan registers may be very quick. A comparatively larger delay (skew) of the clock signal at the second flip-flop can produce a race condition.



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Design Automation

The **full-scan design:** **Physical Design and Timing Verification of Scan**

2. Large delay in scan path. Because the functional routing gets precedence over scan routing in the physical design, some parts of the scan path can be slow. The timing of the scan path should be analyzed to determine a proper clock frequency used for the scan operation. Sometimes, the scan clock is run slower than the rated clock of the chip for similar reasons.

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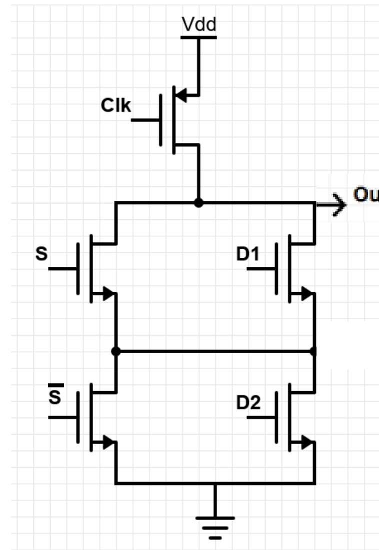
Design Automation

The **full-scan design:** **Physical Design and Timing Verification of Scan**

3. *Dynamic multiplexers.* Scan multiplexers can be economically implemented with dynamic logic (transmission gates.) However, a potential skew between the *TC* (test control) and signals can create a temporary short circuit between the two data inputs of the multiplexer. If the the two input signals are generated by flip-flops that are in different states, such a short can change the state of one of them. A static design of a multiplexer requires more transistors, but does not create a short due to the skew. It should be preferred. Alternatively, the multiplexer should be integrated within the flip-flop cell and carefully analyzed for any signal delay problems.



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Design Automation

The **full-scan design:** **Physical Design and Timing Verification of Scan**

4. Power dissipation during scan. Scan operation produces many changes at the inputs of the combinational logic. These can cause significantly higher power dissipation than the power rating of the device. Both average and peak power consumption should be controlled. Average power that is responsible for heating of the chip may be reduced by slowing down the scan clock. Increased peak power can cause a drop in the supply voltage and create noise problems in the chip. Its reduction may require redesign of test vectors.

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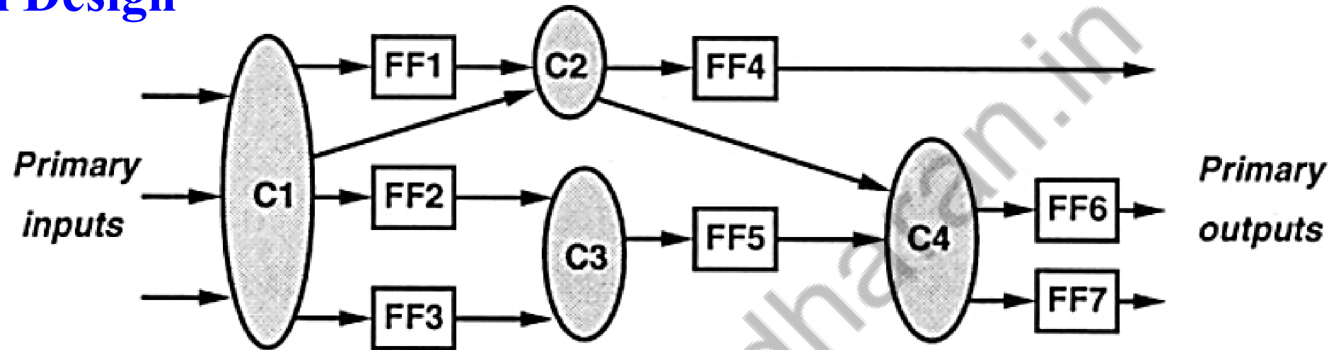
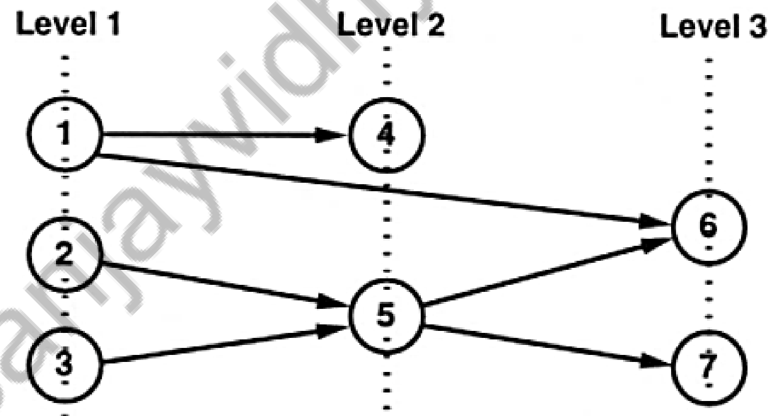
Partial-Scan Design



(a) A feedback-free sequential circuit.



(b) Structure graph (s-graph).

A feedback-free sequential circuit and its s-graph

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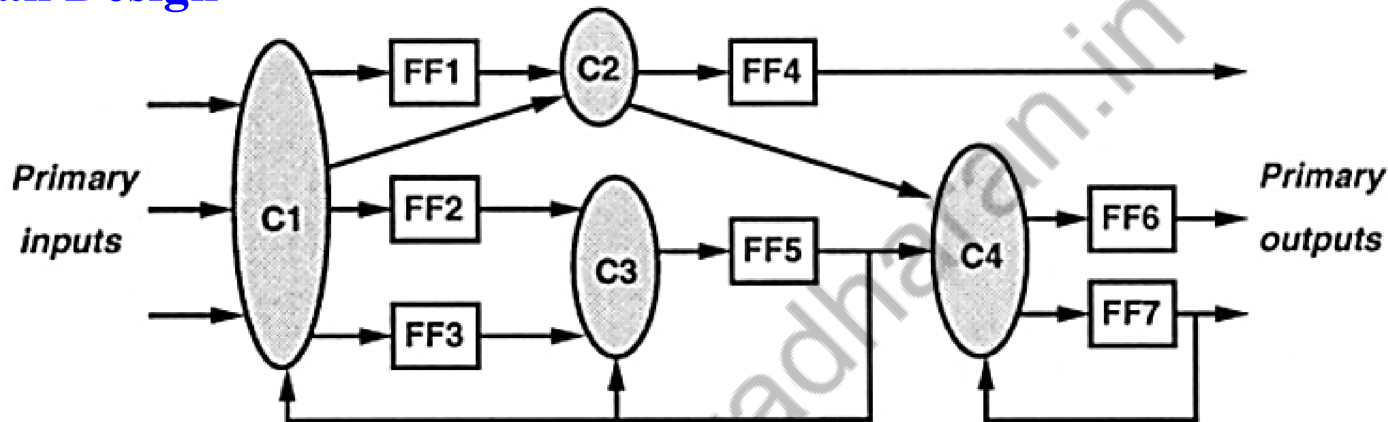
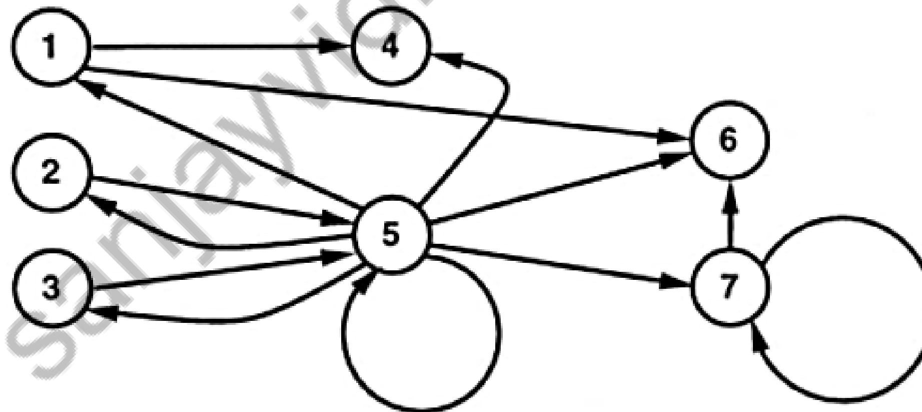
Design Automation

Partial-Scan Design



(a) A sequential circuit with feedback.

If we scan FF5 and FF7, then vertices 5 and 7 will be deleted and the s-graph becomes acyclic with a sequential depth of 2.



(b) Structure graph (s-graph).

A sequential ATPG program can achieve a fault coverage in excess of 95% when about 25 to 50% of the flip-flops are scanned.

A sequential circuit with feedback and its s-graph.

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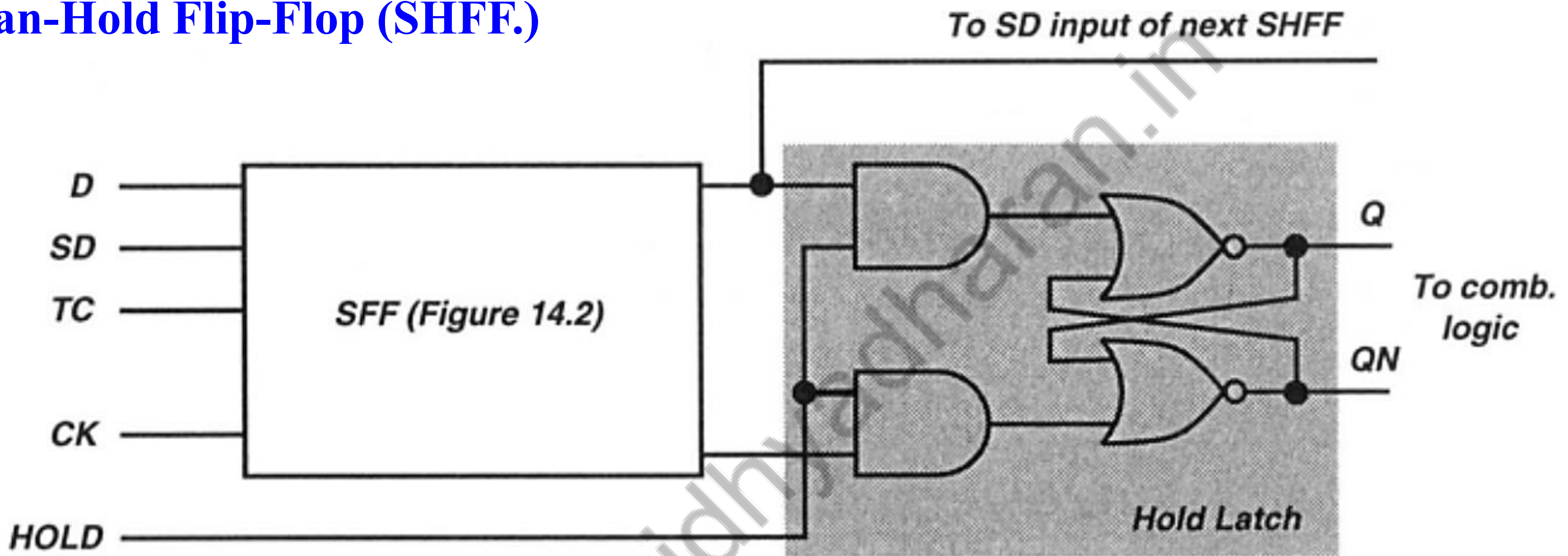
Variations of Scan

Scan-Hold Flip-Flop (SHFF.)



In the normal mode, *TC* = *HOLD* = 1. In the scan mode, *TC* = 1 and *HOLD* = 0. The state inputs of combinational logic driven by the hold latch remain *frozen* at their pre-scan values.

1. Isolates the scan and non-scan portions of a circuit.
2. Delay testing requires the application of vector-pairs to a combinational logic problem. The normal scan structure (with SFFs) places severe restrictions on the vector-pairs that can be produced. The use of the hold latch converts the delay testing problem completely into a combinational logic problem.
3.

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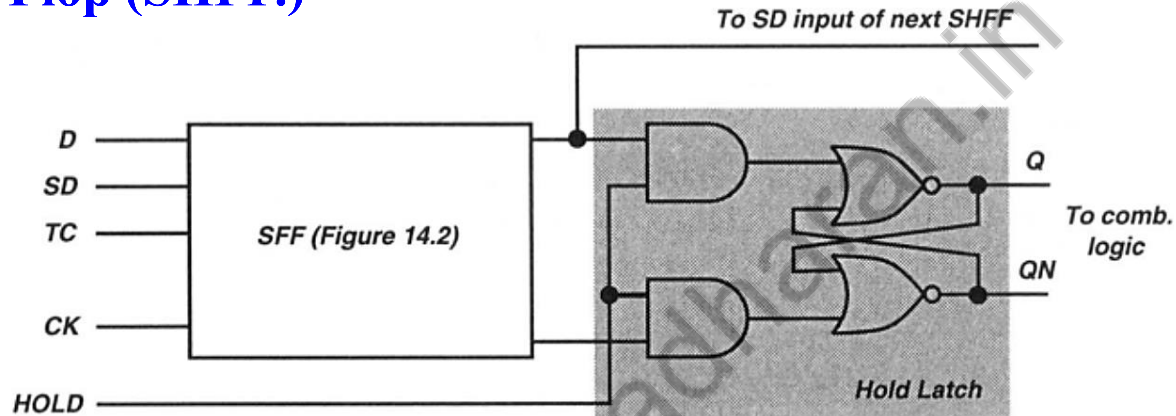
Variations of Scan

Scan-Hold Flip-Flop (SHFF.)



1. Set *HOLD* = 0 and *TC* = 0, and scan the state variable bits of into the scan register using the clock *CK*.
2. Set *TC* = 1.
3. Set *HOLD* = 1 and apply the primary input portion of Thus the entire vector appears at the inputs of the combinational logic.
4. Change *HOLD* to 0.
5. Repeat Steps 1, 2, and 3 for This produces a transition at the inputs of the combinational logic.
6. Change *HOLD* to 0, and capture the output of the combinational logic in FF by applying the clock *CK*.
7. Set *TC* = 0 and apply clocks to scan out the contents of flip-flops. This completes the application of one vector-pair delay test.

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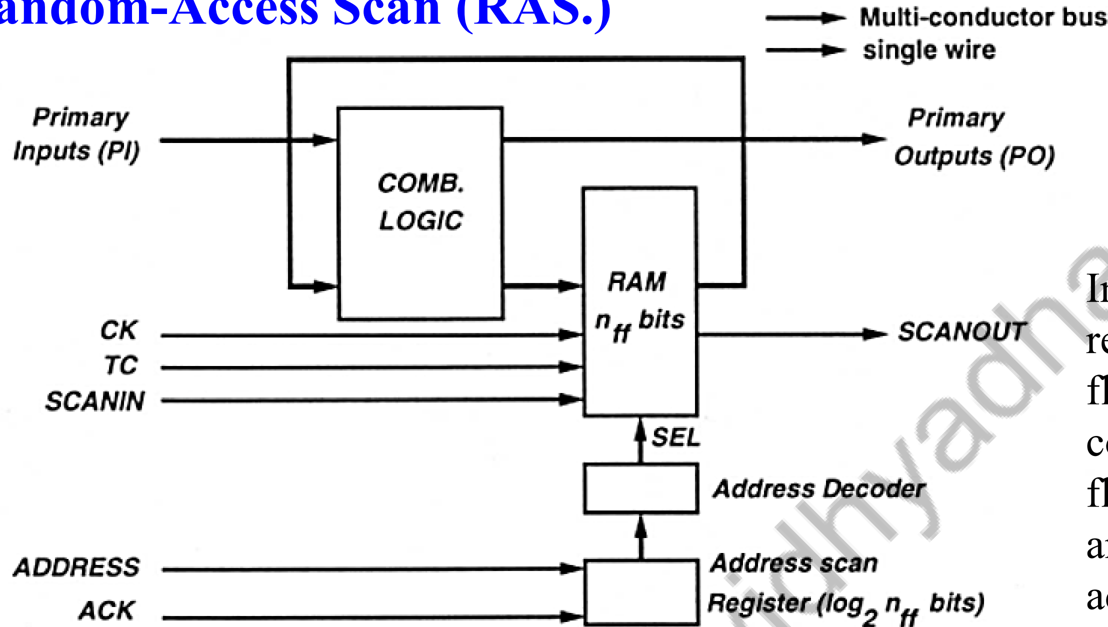
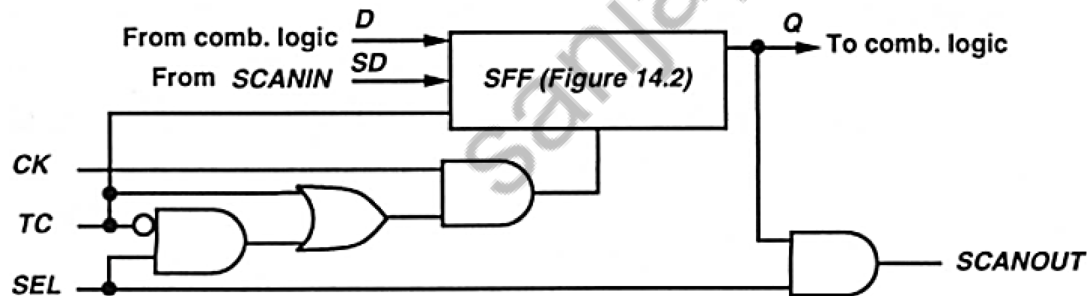
Variations of Scan

Random-Access Scan (RAS.)



(a) Architecture of random-access scan.



(b) A flip-flop for random-access scan.

In the normal mode (*TC* = 1), all flip-flops receive data from the combinational logic under the control of the clock *CK*.

In the scan mode, this scheme allows reading or writing of any selected flip-flop. The flip-flop address, which may contain $log_2 n_{ff}$ bits when there are flip-flops in the RAM, is serially loaded into an *address scan register* (ASR) using an address clock *ACK. The address decoder now produces the select signal SEL = 1 for the addressed flip-flop. The SEL signals to all other flip-flops remain 0. The SCANOUT signals of all flip-flops are tied together to the SCANOUT pin. An advantage of this method is that any flip-flop can be observed even when the circuit is in the normal mode (TC = 1.) For scanning data into a flip-flop, the scan mode (TC = 0) is used.*

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