Testability of VLSI

Lecture 10:
Delay Testing

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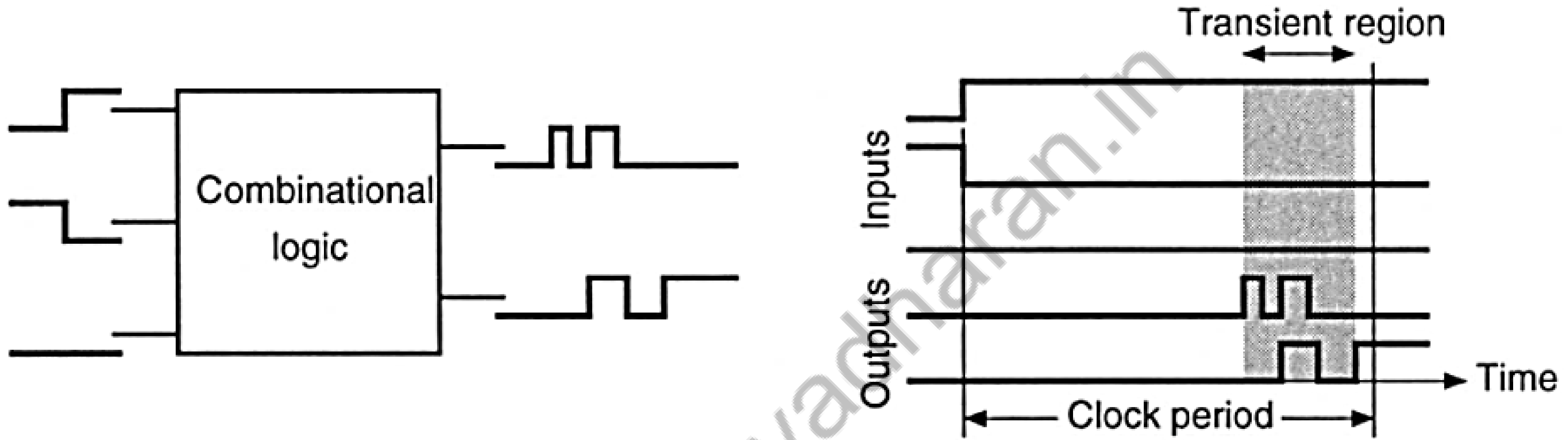
Delay Fault



1. The input signal consists of two vectors: *Delay tests consist of vector-pairs*
2. All input transitions occur at the same time. This, is an idealized illustration though it closely represents the real situation eve in pipelined structures with FFs.
3. Delay is determined by the last transition, or the delay of the longest combinational path
4. Should considering all possible input vector-pairs, "the longest delay combinational path" of the circuit is known as the *critical path.* There can be more critical paths than one if several paths meet the maximum delay criterion.
5. The delay of critical paths determines the smallest clock period at which the circuit can function correctly

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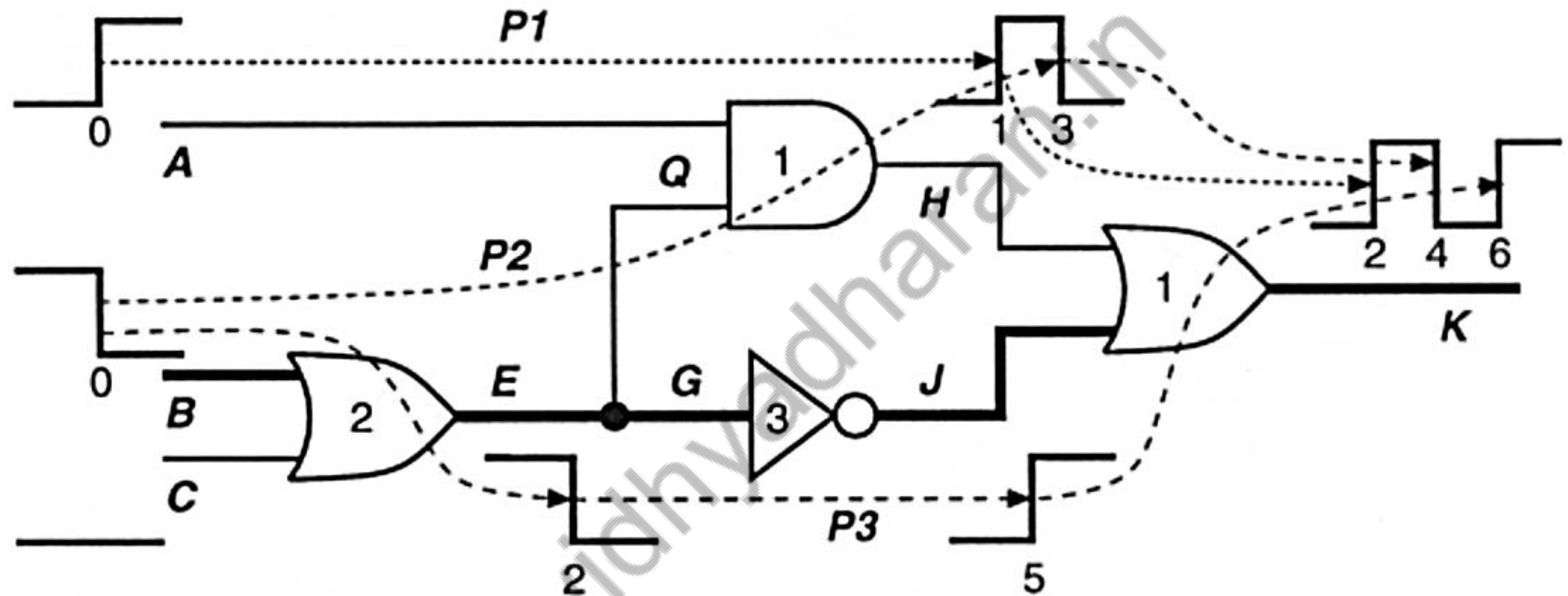
Delay Fault



Gates are modeled with equal rise and fall lumped delays that are integer multiples of some small time unit (nanosecond or picosecond.)

Critical path has a delay of 6 units in the fault-free circuit

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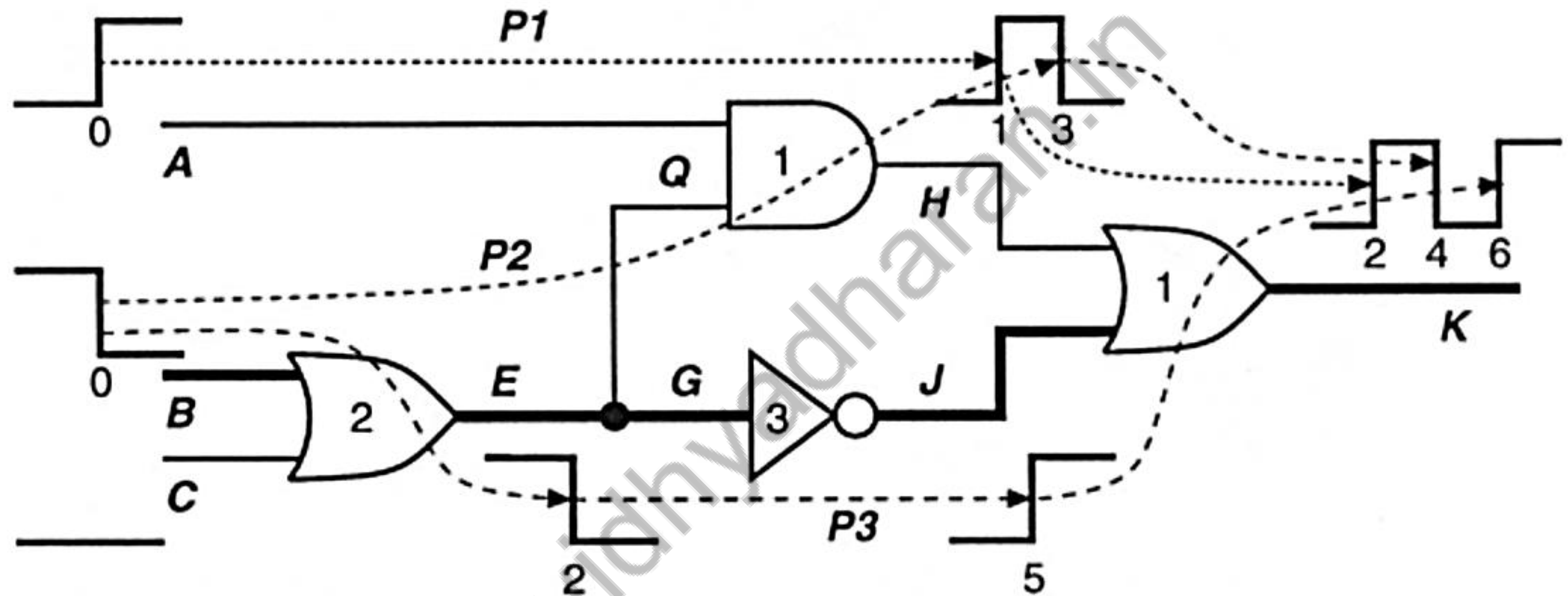
Delay Fault



Single faulty path: Test vector 010→ 100 can only detect delay fault of P3. It masks delay faults of P1 and P2.

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Path-Delay Test

Definition 1 Path-delay fault. *The delay defect in the circuit is assumed to cause the* ***cumulative delay*** *of a combinational path to exceed some specified duration. The combinational path begins at a primary input or a clocked flip-flop, contains a connected chain of gates, and ends at a primary output or a clocked flip-flop. Both* ***switching delays of devices and transport delays of interconnects*** *on the path contribute to the propagation delay. For each combinational path in a circuit, there are two path-delay faults corresponding to* ***rising and falling transitions****, respectively.*

The specified time duration can be the duration of the clock period (or phase), or the vector period.

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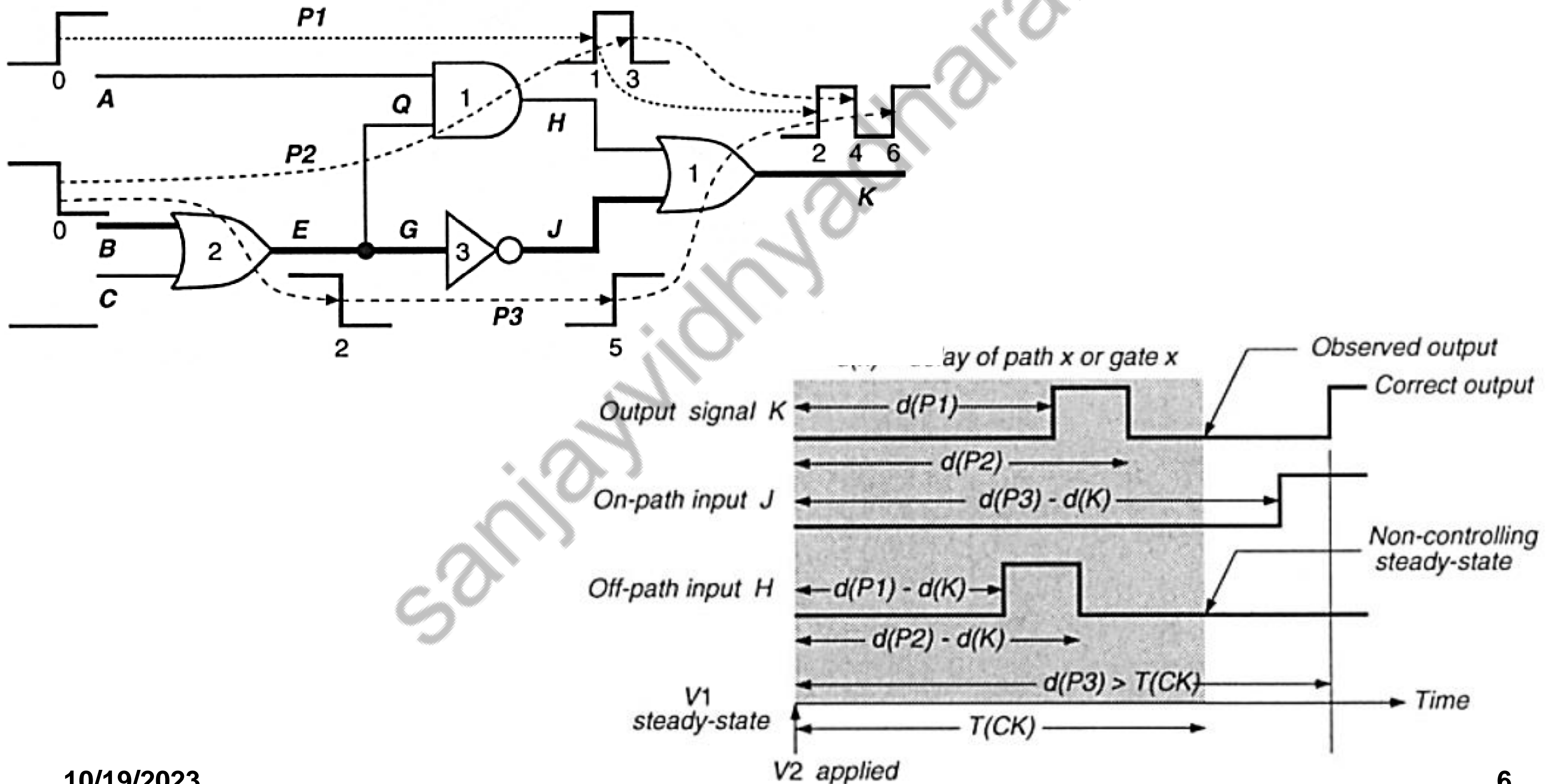
Path-Delay Test

Definition 2 Non-robust path-delay test. *A test that guarantees to detect a path-delay fault, when no other path-delay fault is present, is called a non-robust test for that path. A path-delay fault for which a non-robust test exists is called a "singly-testable path-delay fault.*



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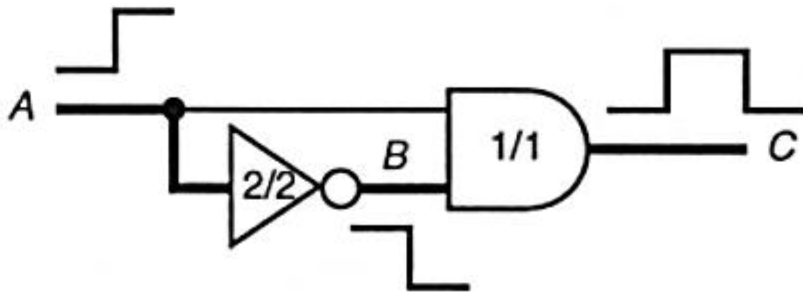
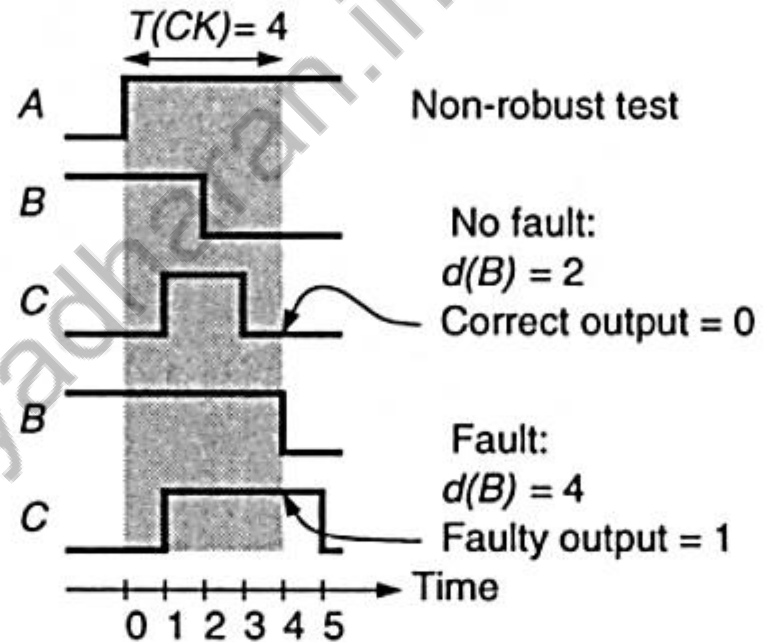
Path-Delay Test

An example of a non-robust test





Since this is a non-robust test, it is not guaranteed to work when other paths are faulty. For example, if an additional delay fault ↑ A – C is present (either due to increased routing delay or due to increase in the delay of the AND gate), then the signal C may remain as constant 0. Top input node of and gate charge to high slowly or fault within and gate

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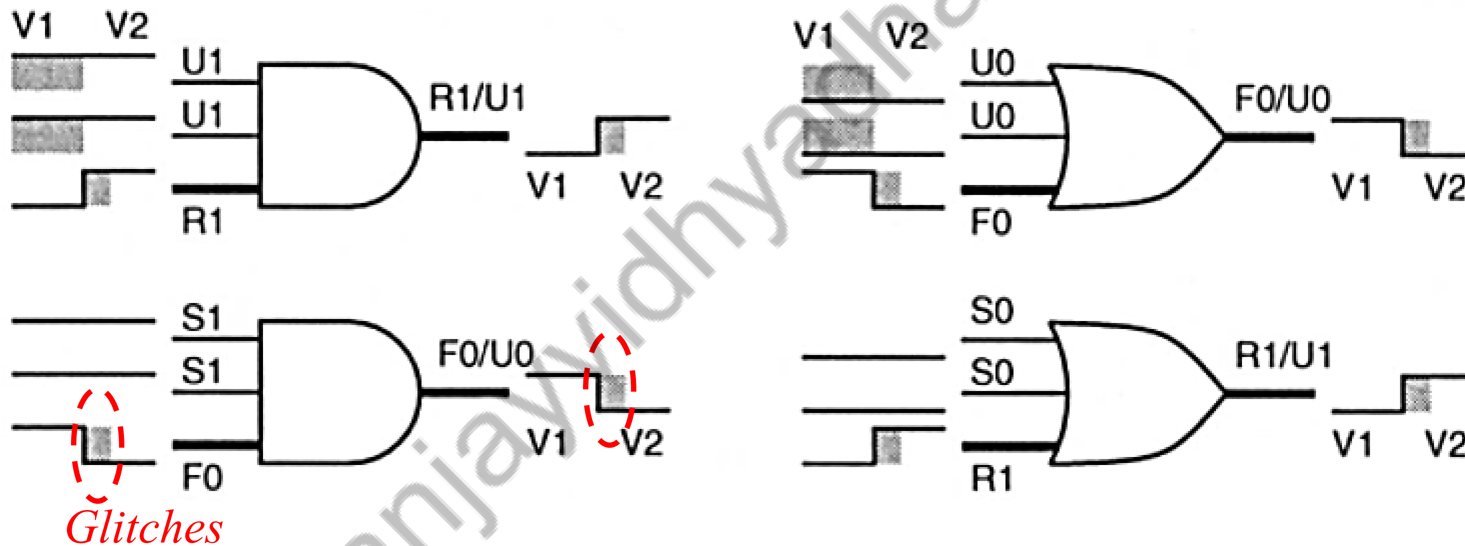
Path-Delay Test

Definition 3 Robust path-delay test. *A robust path-delay test guarantees to produce an incorrect value at the destination if the delay of the path under test exceeds a specified time interval (or clock period), irrespective of the delay distribution in the circuit.*



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Delay Algebra

Five-valued algebra for path-delay tests

AND (rows: Input 2, columns: Input 1)

Input 2 \ Input 1	S0	U0	S1	U1	XX
S0	S0	S0	S0	S0	S0
U0	S0	U0	U0	U0	U0
S1	S0	U0	S1	U1	XX
U1	S0	U0	U1	U1	XX
XX	S0	U0	XX	XX	XX

OR (rows: Input 2, columns: Input 1)

Input 2 \ Input 1	S0	U0	S1	U1	XX
S0	S0	U0	S1	U1	XX
U0	U0	U0	S1	U1	XX
S1	S1	S1	S1	S1	S1
U1	U1	U1	S1	U1	U1
XX	XX	XX	S1	U1	XX

NOT

Input	S0	U0	S1	U1	XX
Output	S1	U1	S0	U0	XX

S0 and S1 are steady (without glitch) 0 and 1 values for both vectors *V*1 and *V*2.

U0 and U1 specify the final value as 0 and 1, respectively, and leave the initial value as don't care or X.

In addition, XX is used to denote both vectors in the don't care state.

F0 and R1 are falling and rising transitions on the on-path signals.

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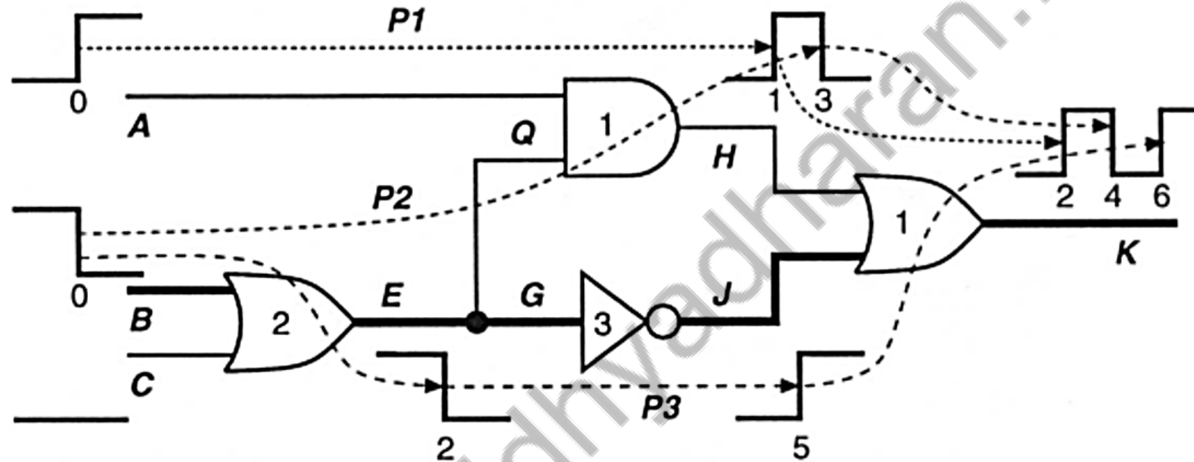
Test Generation for Combinational Circuits

Generation of a test for a path-delay fault requires placing the appropriate transition at the origin of the path and justifying the required off-path inputs of all gates on the path. This is easily accomplished using the five-valued algebra.



E.g. ↓P3

1. Place a transition at the path origin, B = F0.

2. Propagate value F0 to line E, set C = S0/U0, E = F0.

3. G = F0 J = R1.

4. F0 is interpreted as U0 for off-path logic, Q = U0.

5. Propagate value R1 from J to K, set H = S0 K = R1.

6. Justify H = S0, set A = S0.

7. Test is A = S0, B = F0, C = S0; or V1 = 010, V2 = 000

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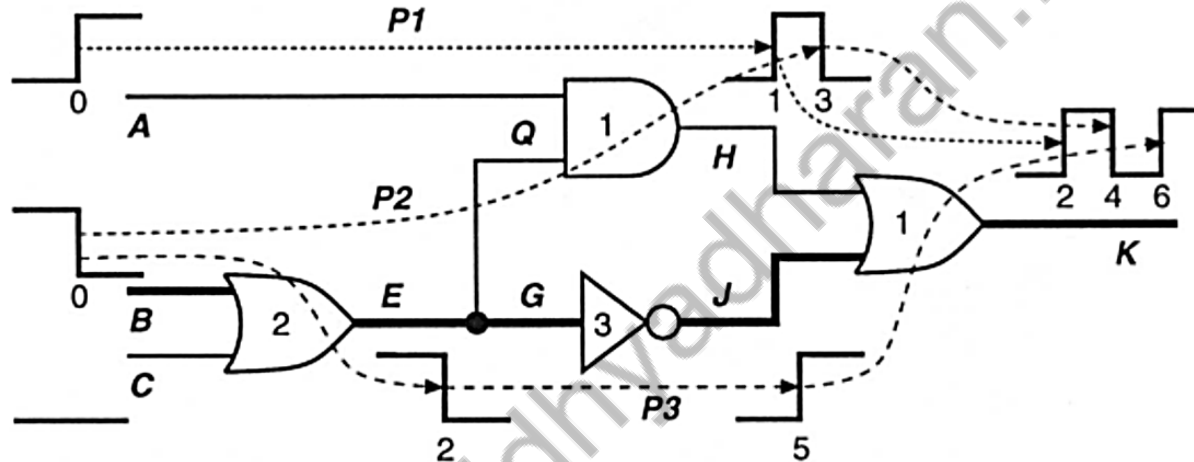

E.g. ↑P2

1. Place a transition at path origin, B = R1.

2. Propagate R1 to E, set C = S0.

3. R1 is interpreted as U1 for off-path logic, G = U1 J = U0.

4. Q = R1, Propagate R1 to H, set A = S1.

5. H = R1, Propagate R1 to K, must set J = S0 conflict since J = U0 in step 3.

6. Since no step has any alternatives, a robust test is not possible.

The reliability of non-robust tests is questionable

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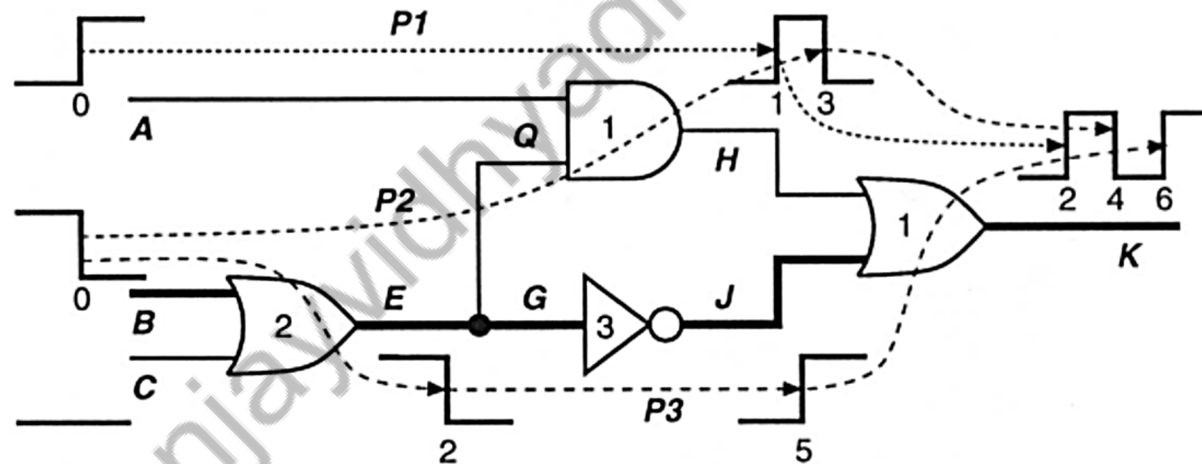
Test Generation for Combinational Circuits

The presence of robust tests for some paths can improve the reliability of non-robust tests for other paths. For example,

$\uparrow P1, \downarrow P1, \uparrow P3, \downarrow P3, \uparrow C - E - G - J - K$ and $\downarrow C - E - G - J - K$

are robustly testable.



By including the six robust tests we can ensure that if the circuit passes those, there will be no delayed signal at off-path inputs of the path $P2$. We can conclude that in the presence of the other four tests, the non-robust test for $\uparrow P2$ is as good as a robust test. Such a test is called a *validatable non-robust* (VNR) test

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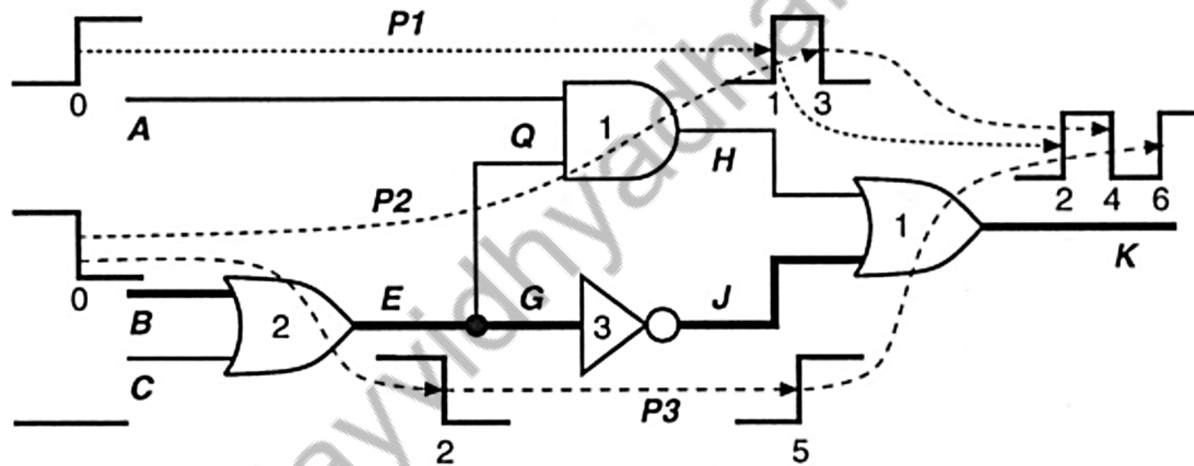
Test Generation for Combinational Circuits

Untestable path delay fault.

Consider the path-delay fault ↓P2 . A falling transition (F0) is placed at B and is easily propagated to H by setting appropriate values on A and C. However, a forward implication sets the off-path input of the output OR gate to U1 (i.e., controlling value in V2.) This path-delay fault has no test.



A path for which both (rising and falling) path-delay faults (PDFs) are singly (i.e., non-robustly) testable is called a *testable path.* A path having one singly testable PDF and one singly untestable PDF is called a *partially testable path.* When no non-robust test exists for both PDFs of a path, that path is called a *singly-untestable path.* Such a path can be eliminated by circuit transformations that preserve the logic function.

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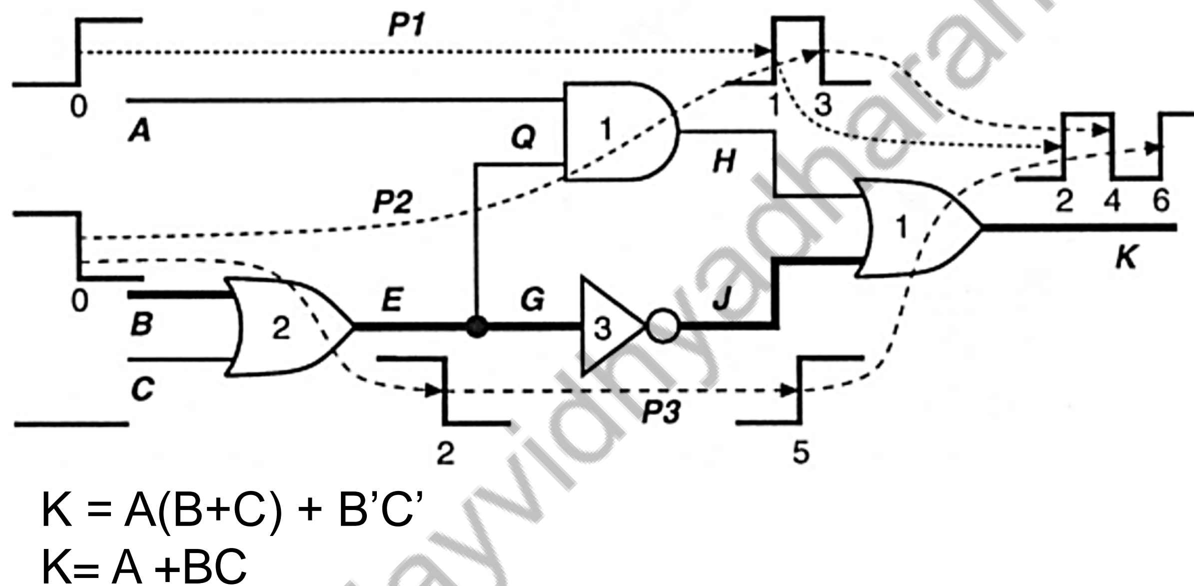
Test Generation for Combinational Circuits

An untestable path is (and a partially testable path may be) associated with one or more redundant single stuck-at faults



In general, a partially testable path may not have a redundant stuck-at fault. However, there are procedures for modifying the circuit to expose redundant faults that can be removed. The resulting circuit always has fewer paths, a greater percentage of testable paths.

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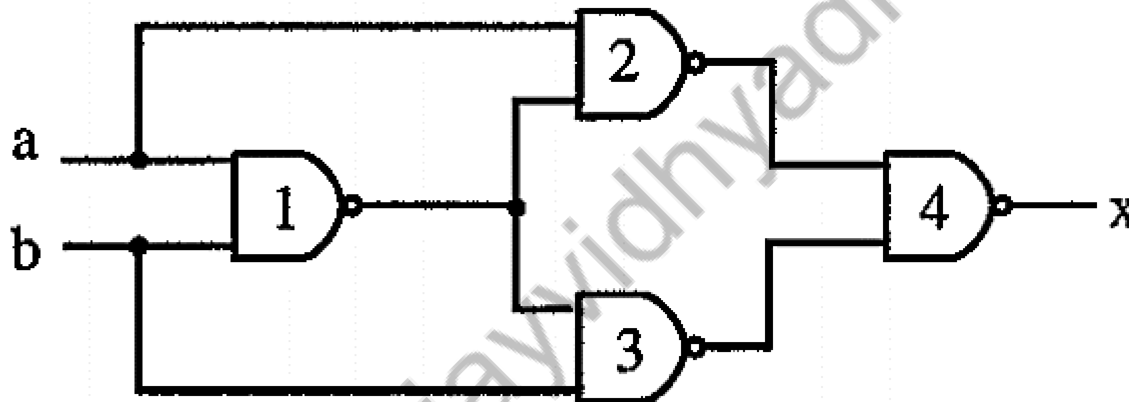
Test Generation for Combinational Circuits

A combinational circuit may have paths whose delays cannot affect the time of signal change at the output. These paths are called *false paths*.

PDFs ↓a124x and ↓b134x are non-ST



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Test Generation for Combinational Circuits

Fault Simulation Algorithm

1. Vertices in Path-status graph PSG correspond to inputs, outputs and gates with multi-fanouts. Single fanout are not represented in the PSG.

M. A. Gharaybeh, V. D. Agrawal, M. L. Bushnell, and C. G. Parodi, "False-Path Removal Using Delay Fault Simulation," *Journal of Electronic Testing: Theory and Applications,* vol. 16, no. 5, pp. 463–476, Oct. 2000.

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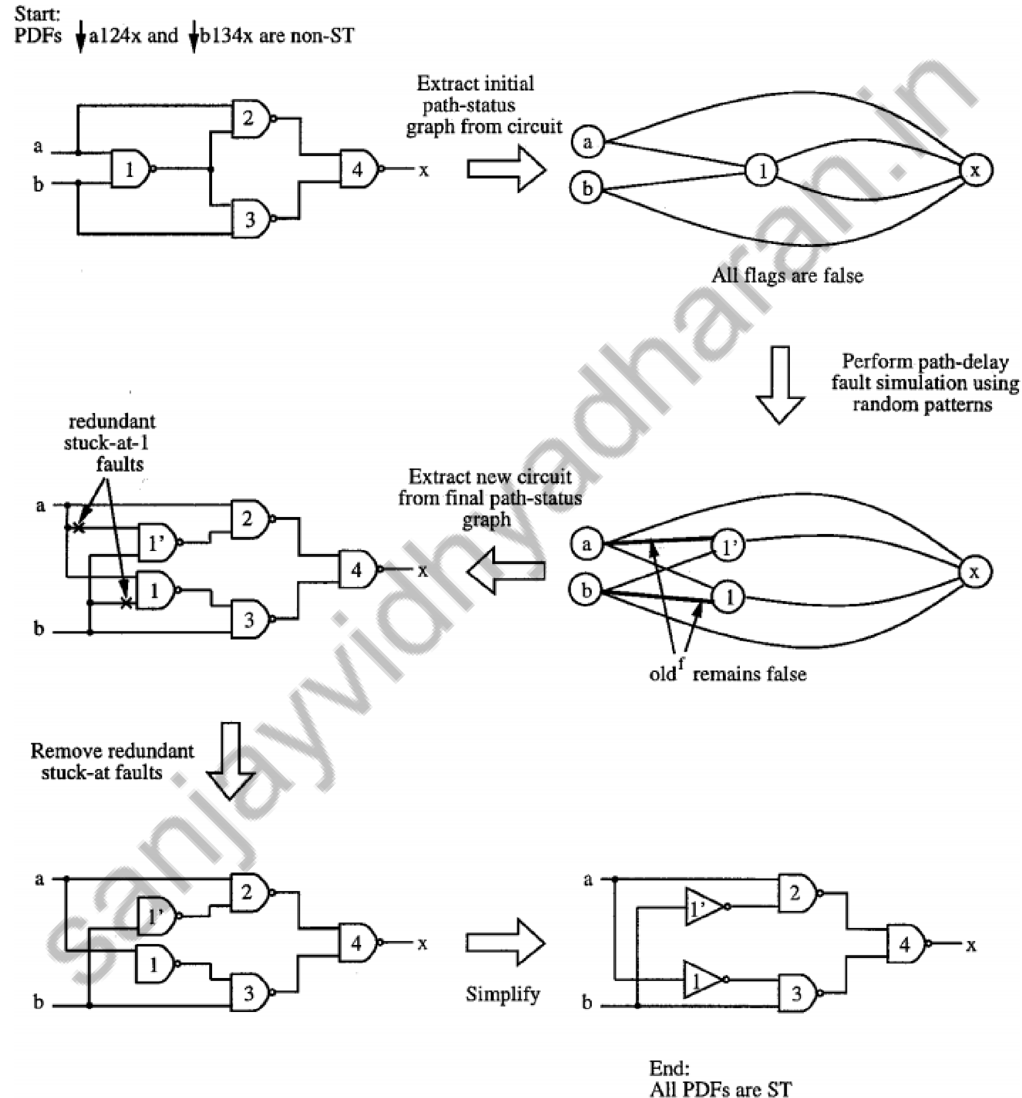
Test Generation for Combinational Circuits



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Test Generation for Combinational Circuits

The paths of singly-untestable PDFs are not always false paths. For example, a singly-untestable PDF may be co-sensitized (sensitized simultaneously) with other singly-untestable PDFs and the timing of the circuit would be affected if all co-sensitized paths have excess delays. These paths belong to the classes of *multiply-testable PDFs* [245] and *functionally sensitizable PDFs* [155].

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Transition Faults

- ***Transition fault:*** A simpler delay fault model
- A transition fault on a line makes the signal change on that line slow
- The two possible faults are *slow-to-rise* and *slow-to-fall* types
- For detecting a slow-to-rise fault on a line, we take a test for a stuck-at-0 fault on that line. This test will set the line to 1 in the fault-free circuit and propagate the state of the line to a primary output. *Two test vectors required :* V1 sets the line to 0 and V2 sets it to 1. **V2 also creates an observation path to a primary output.**

- The basic assumption in this test is that the faulty delay of the signal rise has to be large, since the observation path may be, and often is, a short path. Besides, the effects of hazards and glitches can interfere with the observation of the output value. As a result, the tests for transition faults **can detect localized (spot) delay defects of large (gross) delay amounts.** Because of sensitization of short paths these tests may **fail to detect distributed defects**, where small delay increases in a large number of gates cause a long path to fail.

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Transition Faults

The advantages of the transition fault model are:

- The number of faults has an upper bound of twice the number of lines.

- Tests are easy to generate. A stuck-at fault test generator can be easily modified to produce tests for transition faults.
- Circuits that either have, or are modified to have, a high stuck-at fault coverage usually also have high transition fault testability.

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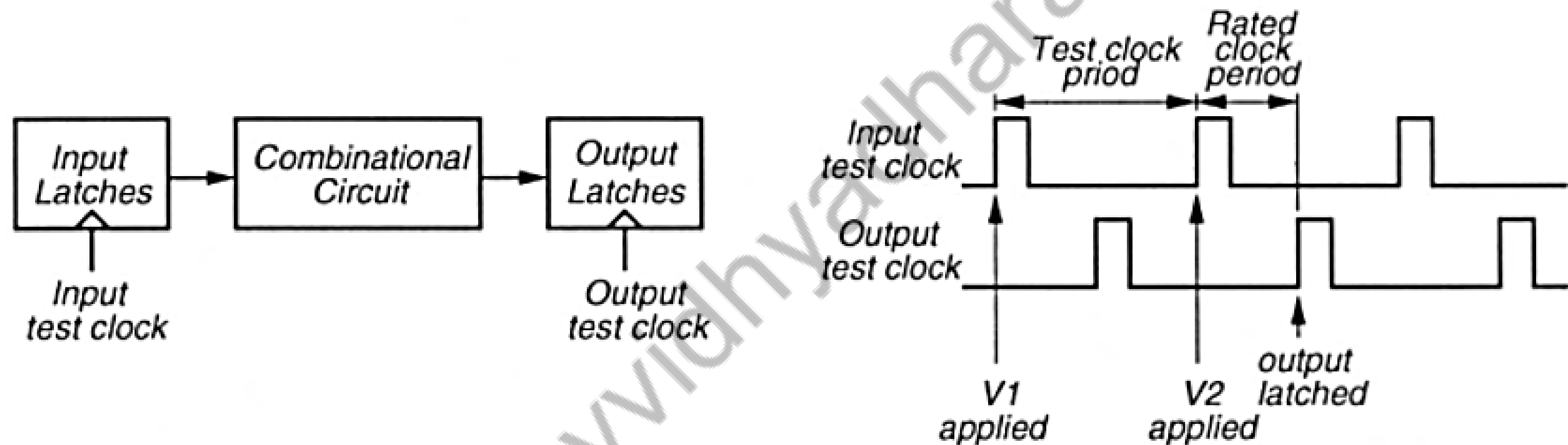
Delay Test Methodologies

1. Slow-Clock Combinational Test

This procedure is applicable to combinational circuits or to those sequential circuits that are internally combinational with flip-flops only at PIs and POs.



A two-vector delay test assumes that all signals due to the first vector $V1$ will have reached their steady state when $V2$ is applied. If this assumption is not valid, then the actual circuit may still have some transient signals when $V2$ is applied. These transients can interfere with the testing of the targeted path. To avoid this problem, vectors are applied at a slower than the rated clock frequency.

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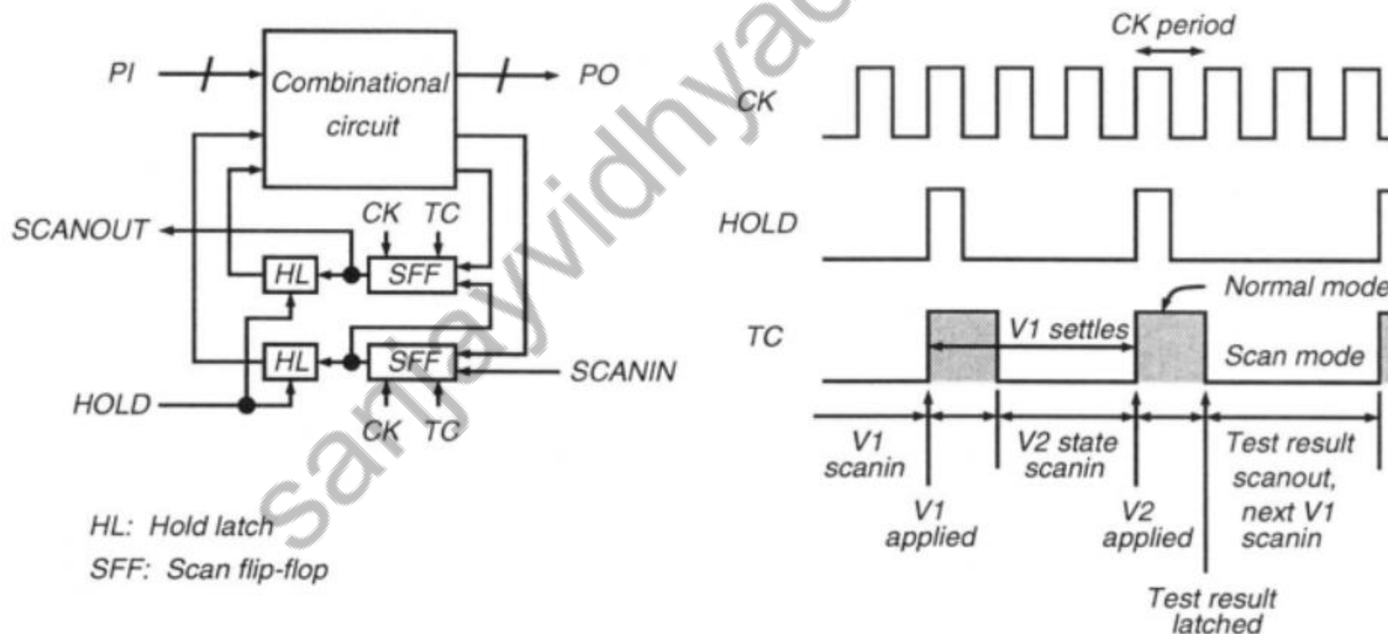
Delay Test Methodologies

2. Enhanced-Scan Test

This method is applicable to scan types of sequential circuits. Its main advantage is that any arbitrary vector-pair can be applied. So, delay tests can be generated by considering the combinational logic alone, making the test generation easier. However, a normal scan circuit should be enhanced by inserting *hold latches* and an additional *HOLD* signal. The design and operation of the enhanced flip-flop, known as *scan-hold flip-flop* (SHFF),



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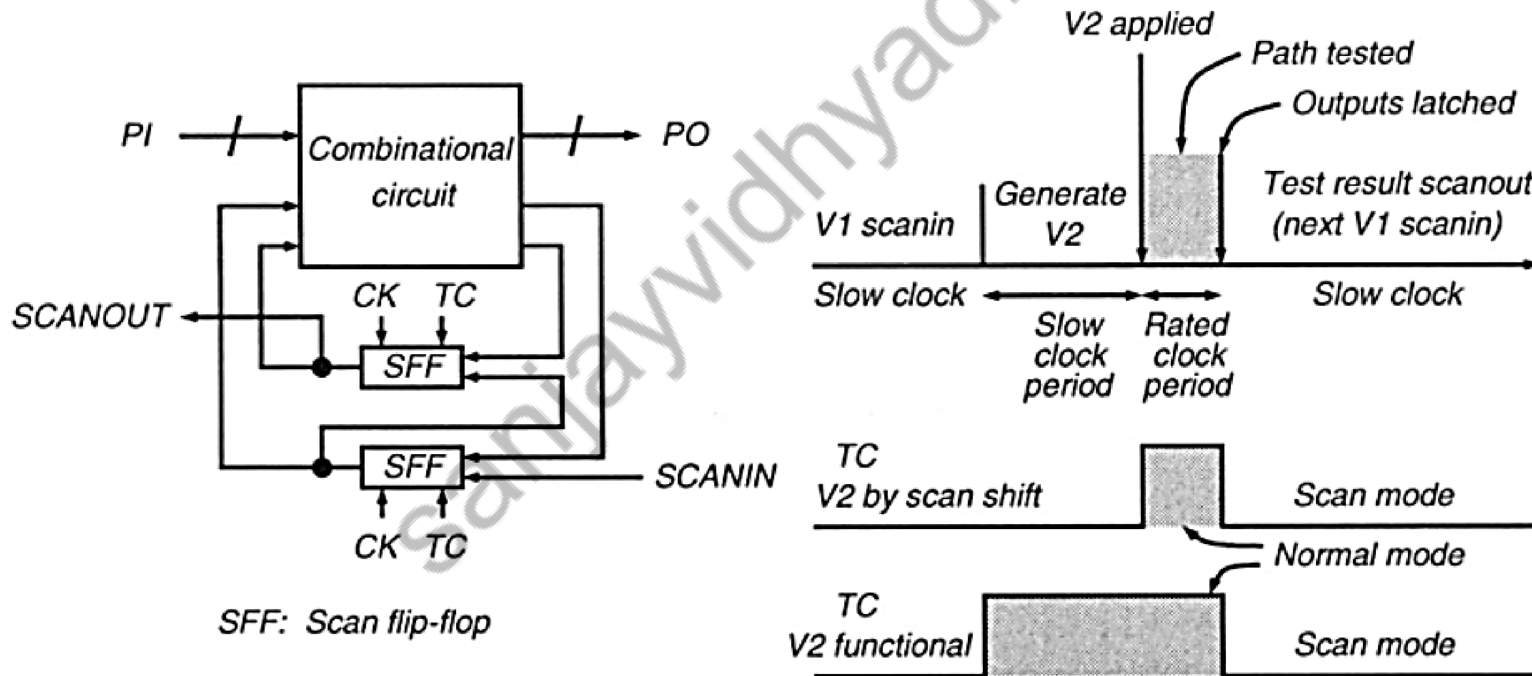
Delay Test Methodologies

3. Normal-Scan Sequential Test

Normal full-scan circuits (with no hold latches) can be tested for delay faults, but the vector-pairs must be especially generated. Here, the first vector V1 is scanned in (usually with a slow scan clock) and is then replaced in the scan register by either (a) applying a one-bit shift to the scan register, or (b) propagating V1 through the combinational logic in the normal mode.



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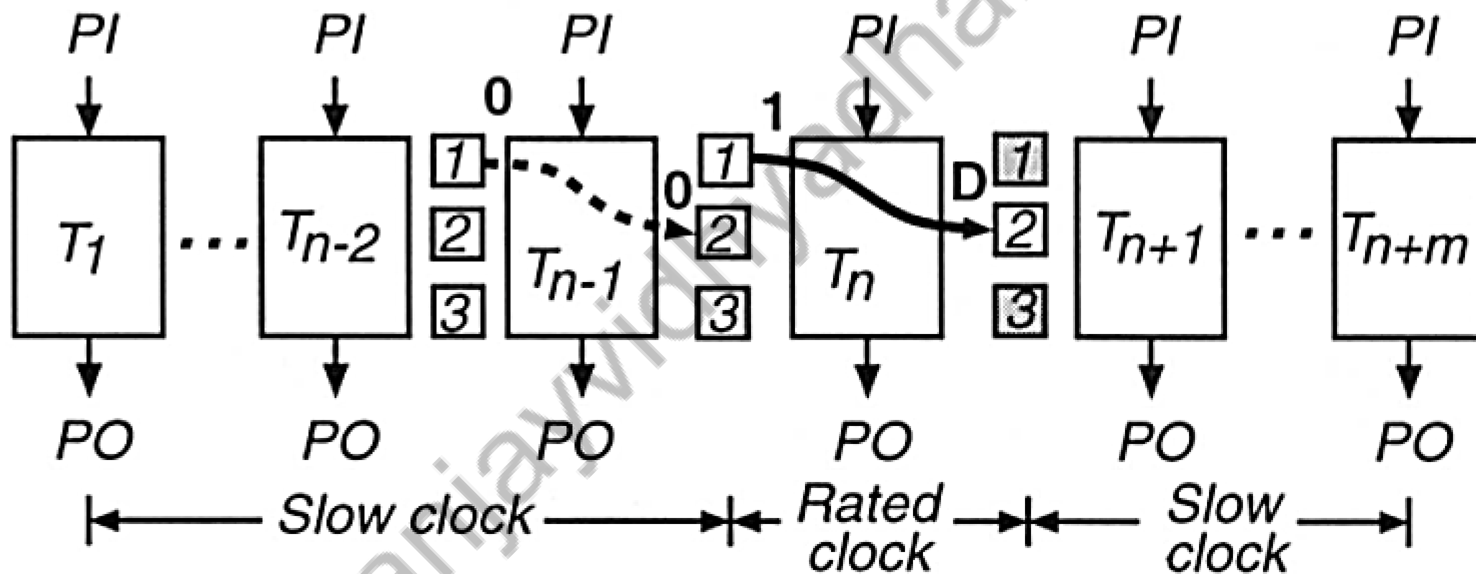
Delay Test Methodologies

4. Variable-Clock /Slow Clock Non-Scan Sequential Test

Testing of a delay fault in a non-scan sequential circuit requires more than two vectors like in the case of sequential circuit testing



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5. Rated-Clock Non-Scan Sequential Test

All vectors, either functional or those generated to cover any types of faults, are applied at the rated speed. A target delay fault can be activated in several time frames. If robust detection is desired, one must consider all delay combinations to be potentially possible. Even fault simulation requires massive computation. Nevertheless, it shows a much reduced PDF coverage for vectors generated for variable-clock test.

"Static timing analysis." done with enough slack in commercial tools like *Primetime*

- *Timing simulation*
- *Critical path tests*
- *Layout optimization*

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