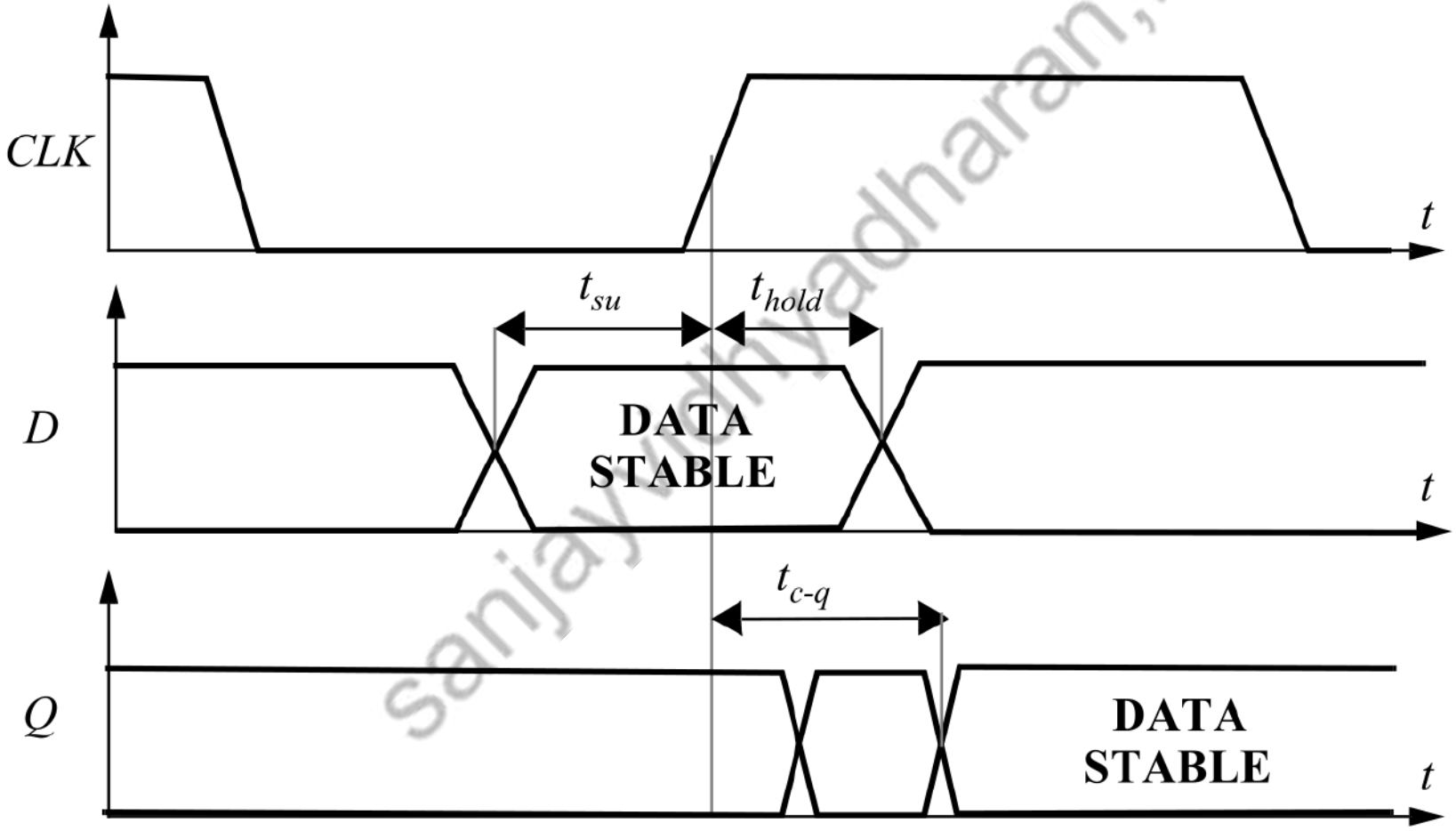
Advanced VLSI Design: 2023-24
Lecture 5
Static Timing Analysis

By Dr. Sanjay Vidhyadharan

Timing Constraints of a Flip-flop

- Setup Time
- Hold Time



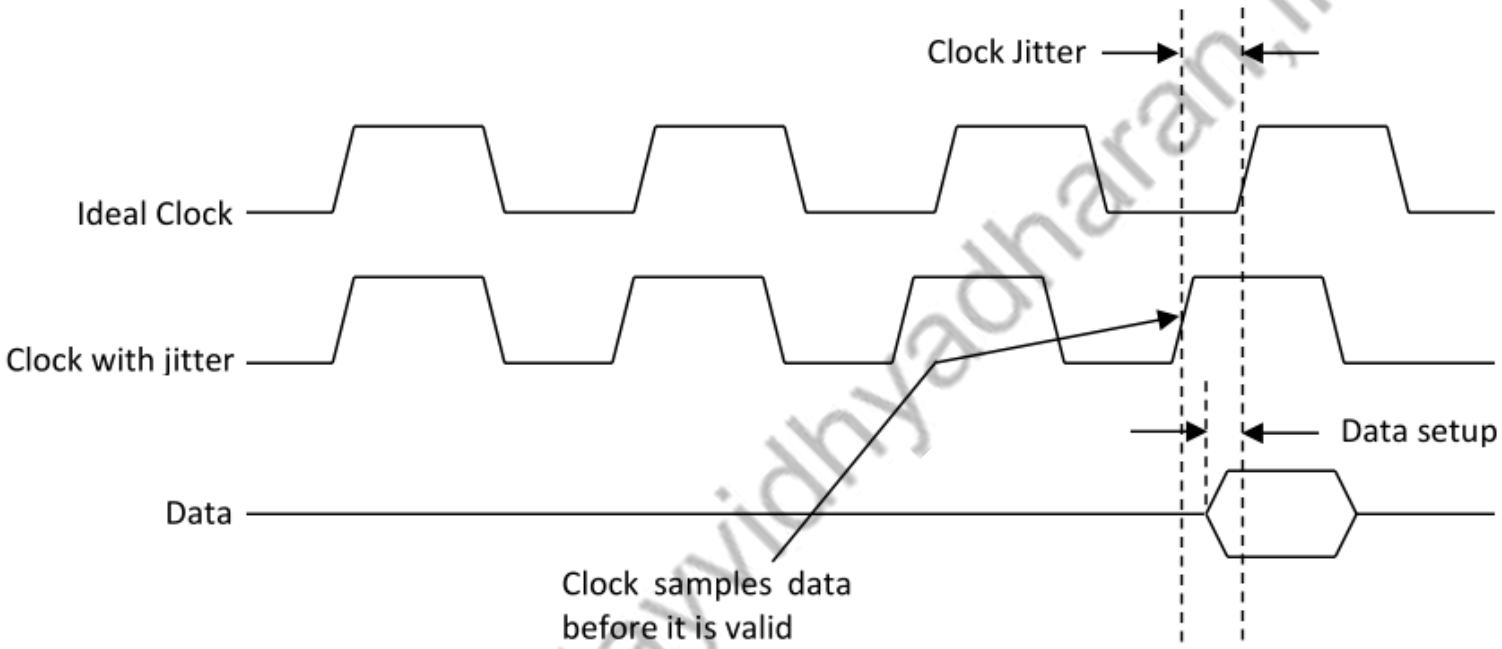
Clock Skew and Jitter

Clock skew (sometimes called timing **skew**) is a phenomenon in synchronous digital circuit systems (such as computer systems) in which the same sourced **clock** signal arrives at different components at different times. Cause : Wires , Buffers etc

Clock Jitter: Sometimes some external sources like noise, voltage variations may cause to disrupt the natural periodicity or frequency of the clock. This deviation from the natural location of the clock is termed to be clock jitter.

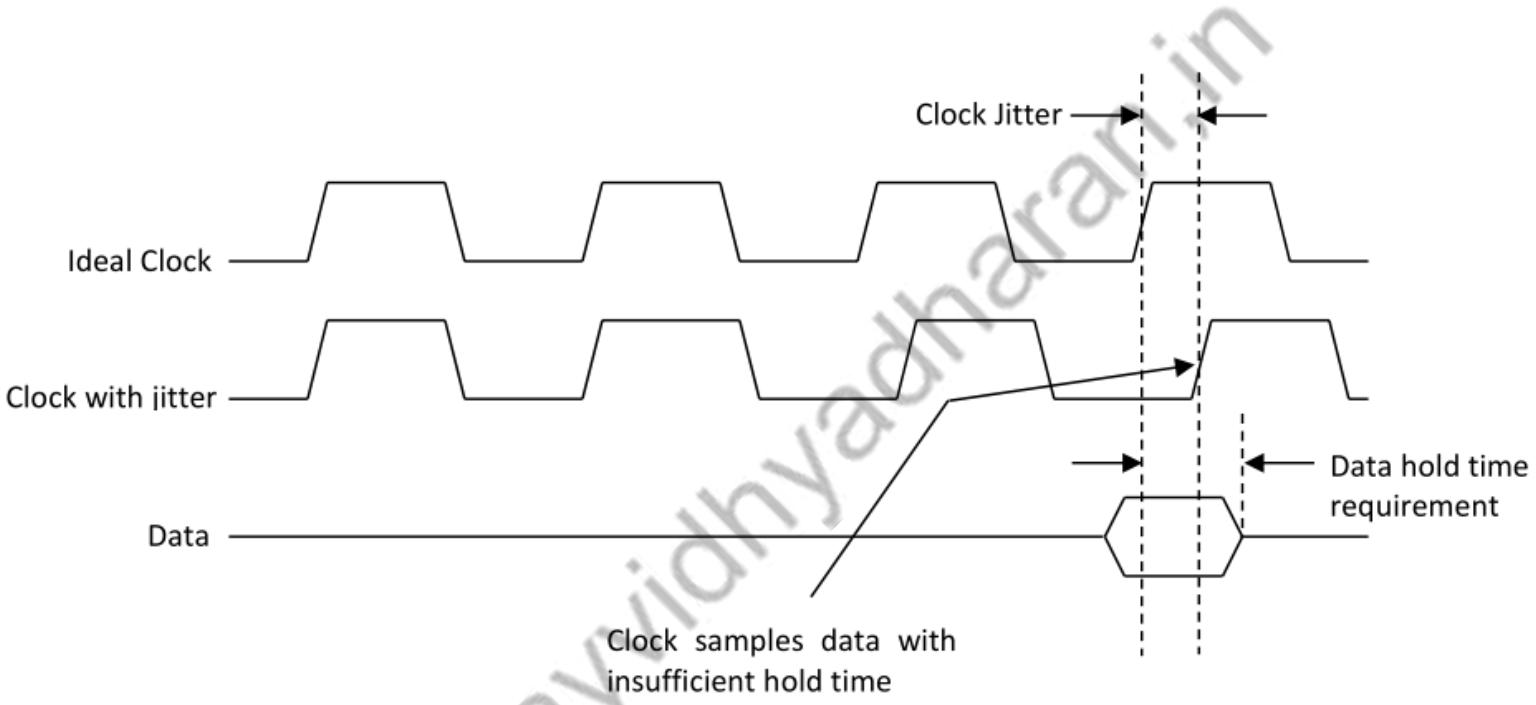
Clock Uncertainty = Clock Jitter + Clock Skew

Timing Constraints of a Flip-flop



Data setup violation caused by clock uncertainty

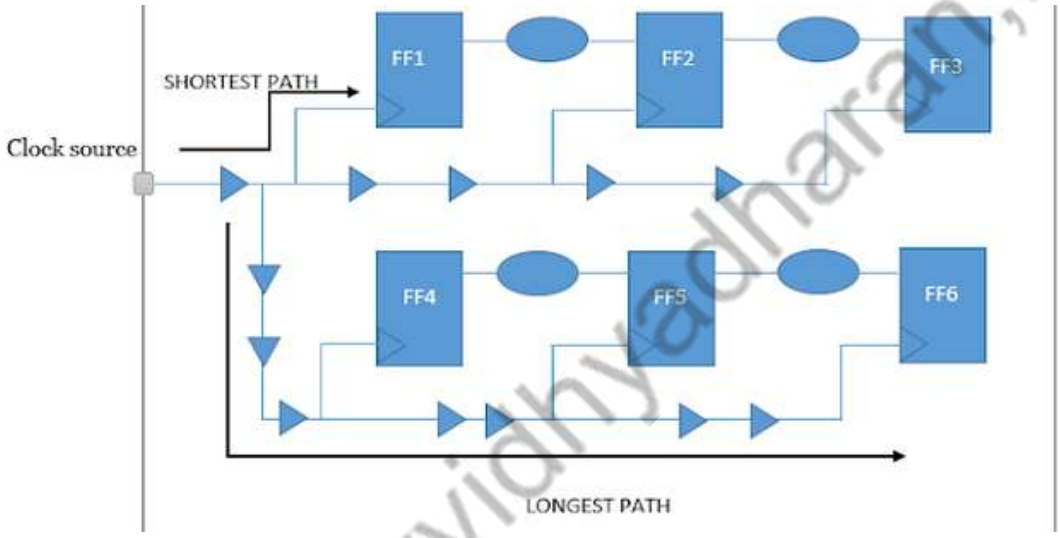
Timing Constraints of a Flip-flop



Data hold time violation caused by uncertainty

Clock Skew

The Difference in arrival of clock at two consecutive pins of a sequential element.

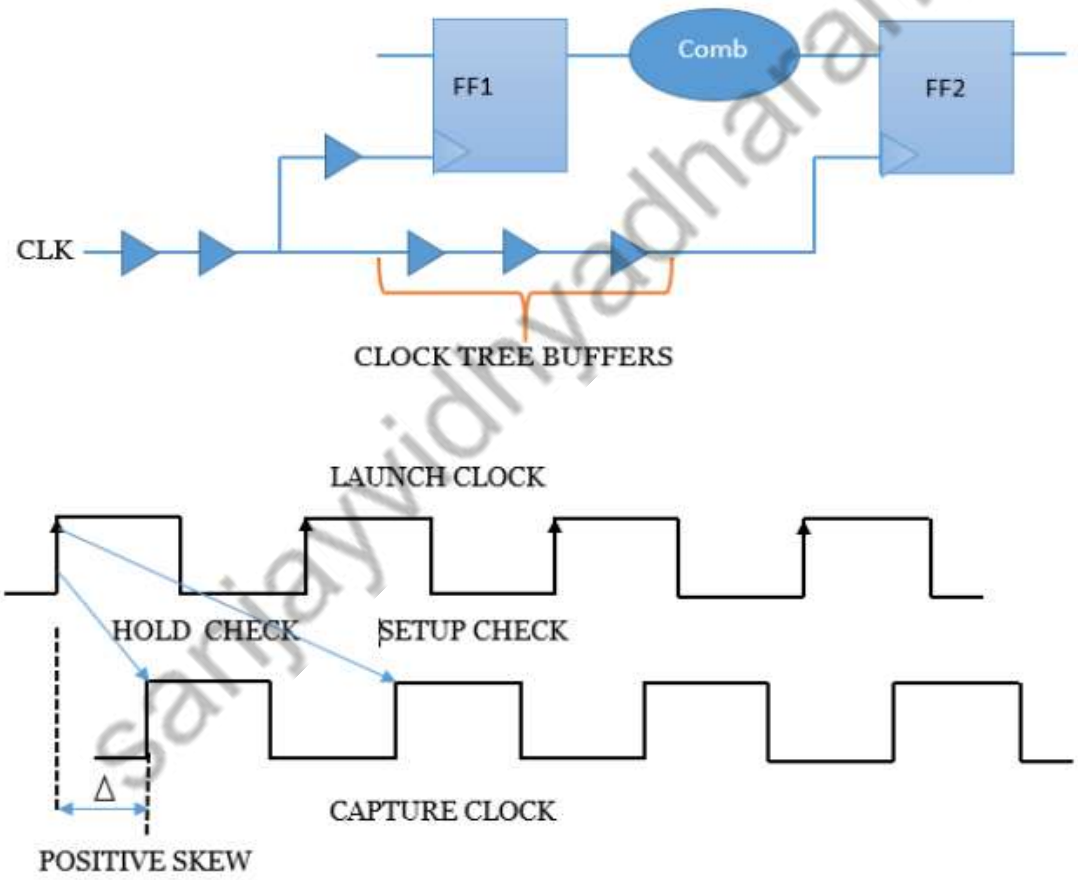


Sources of skew:

- Wire mismatch (Clock interconnect length)
- Differences in input capacitance on the clock
- Varying number of Buffers input interconnect length

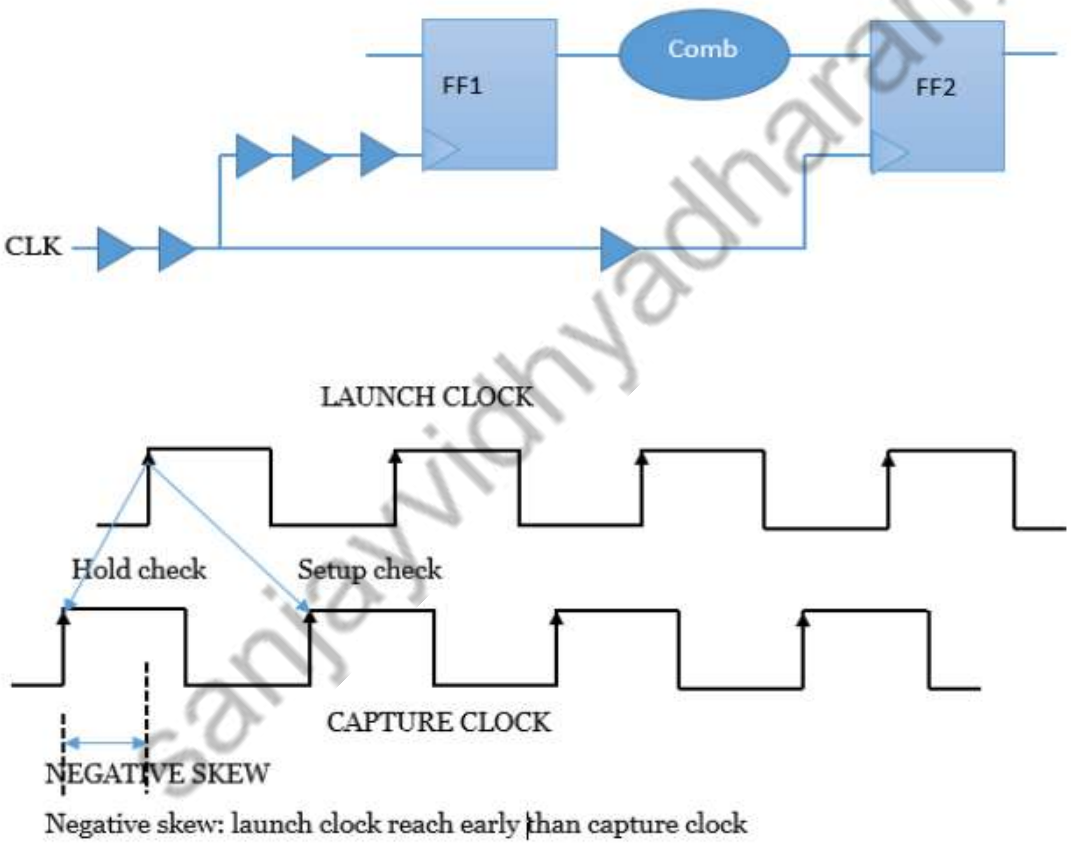
Clock Skew

Positive skew: if the capture clock comes late than the launch clock.



Clock Skew

Negative skew: : if the capture clock comes early than the launch clock.



Negative skew: launch clock reach early than capture clock

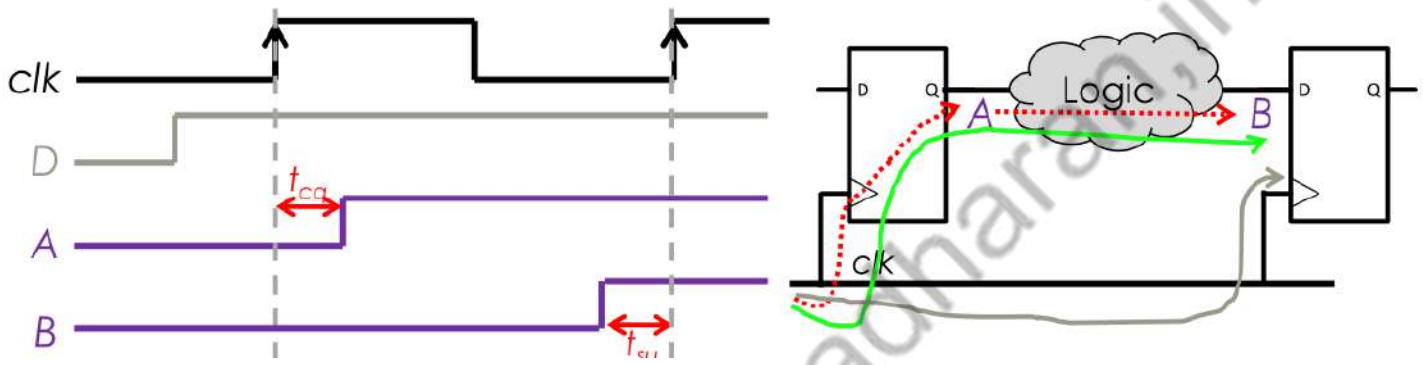
Static Time Analysis

There are two main problems that can arise in synchronous logic:

- Max Delay: The data doesn't have enough time to pass from one register to the next before the next clock edge.
- Min Delay: The data path is so short that it passes through several registers during the same clock cycle.
- Max delay violations are a result of a slow data path, including the registers, $\mathbf{t_{su}}$ therefore it is often called the "Setup" path.
- Min delay violations are a result of a short data path, causing the data to change before the $\mathbf{t_{hold}}$ has passed, therefore it is often called the "Hold" path.

Static Time Analysis

Setup (Max) Constraint



- After the clock rises, it takes t_{cq} for the data to propagate to point A.
- Then the data goes through the delay of the logic to get to point B.
- The data has to arrive at point B, t_{su} before the next clock.

$$T > t_{CQ} + t_{\text{logic}} + t_{SU}$$

$$T + \delta_{\text{skew}} > t_{CQ} + t_{\text{logic}} + t_{SU} + \delta_{\text{margin}}$$

Setup Slack = Data Required Time – Data Arrival Time

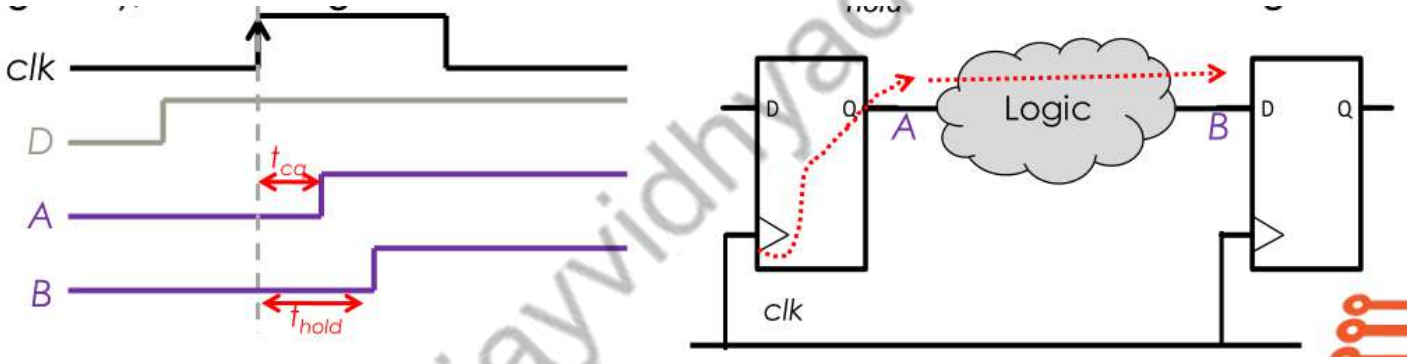
- Positive Slack : No Timing Violation
- Negative Slack : Timing Violation

Static Time Analysis

Hold (Min) Constraint

Hold problems occur due to the logic changing before t_{hold} has passed.
This is not a function of cycle time – it is relative to a single clock edge!

- The clock rises and the data at A changes after t_{cq} . The data at B changes t_{pd} (logic) later.
- Since the data at B had to stay stable for t_{hold} after the clock (for the second register), the change at B has to be at least t_{hold} after the clock edge.



$$t_{CQ} + t_{\text{logic}} > t_{hold}$$

$$t_{CQ} + t_{\text{logic}} - \delta_{\text{margin}} > t_{hold} + \delta_{\text{skew}}$$

Hold Slack = Data Arrival Time– Data Required Time

- Positive Slack : No Timing Violation
- Negative Slack : Timing Violation

Static Time Analysis

Launch Path

- Launch path is launch clock path which is responsible for launching the data at launch flip flop

Capture Path

- Capture path is capture clock path which is responsible for capturing the data at capture flip flop

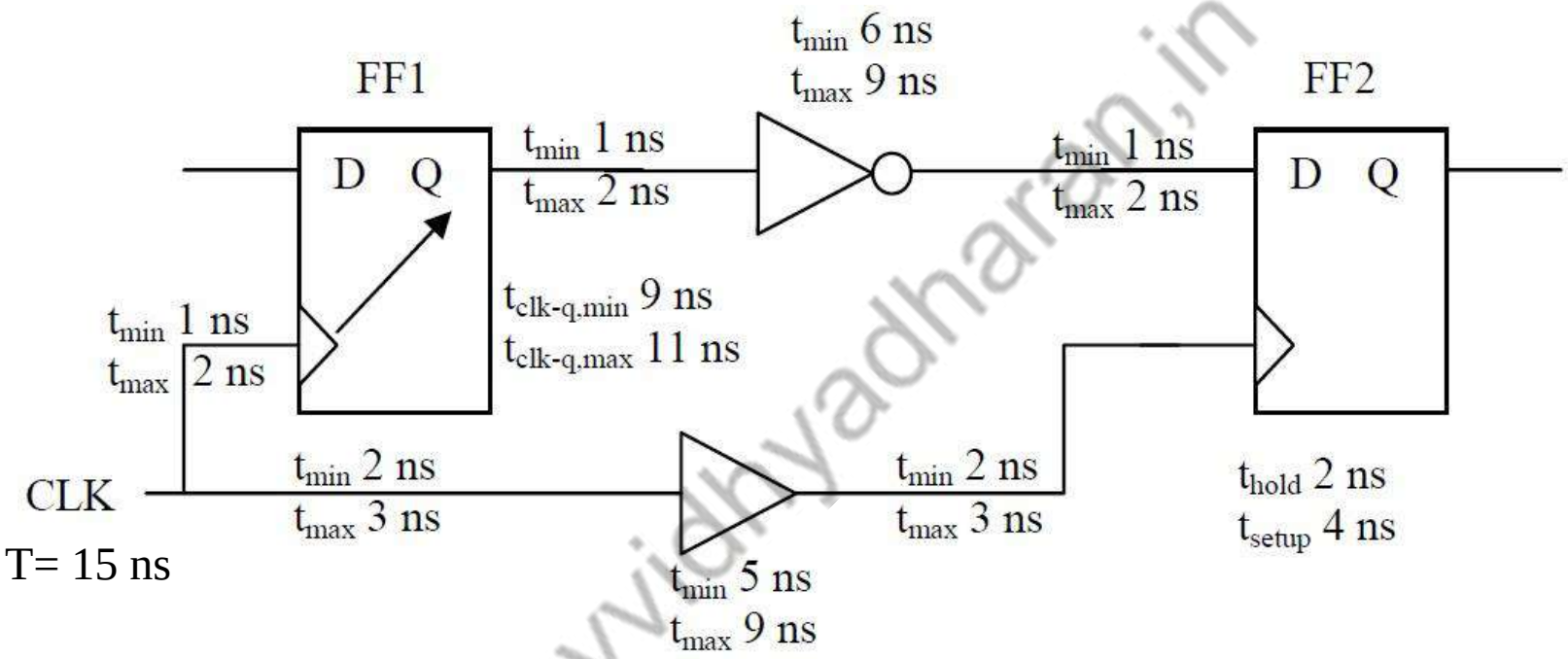
Arrival Time

- Launch path and data path together constitute arrival time of data at the input of capture flip-flop

Required Time

- Capture clock period and its path delay together constitute required time of data at the input of capture register

Static Time Analysis



Setup slack = Min. Clock Path Delay - Max. Data Arrival Time

= (15 ns + 2ns + 5 ns + 2 ns - 4 ns) - (2 ns + 11 ns +2 ns + 9 ns + 2 ns)

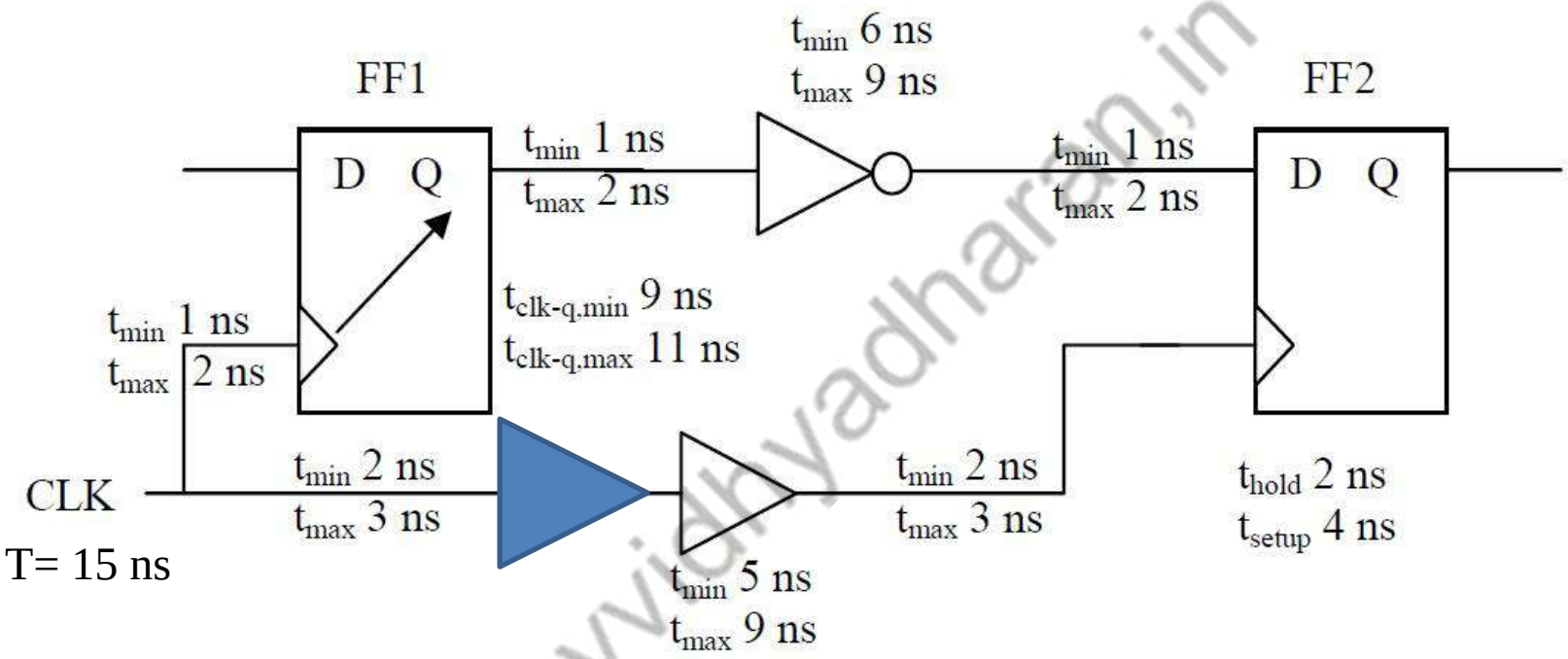
= 20 ns – 26 ns = -6 ns : Setup Time Violation.

Hold time slack = Min. Data Arrival Time - Max. Clock Path Delay

= (1 ns + 9 ns + 1 ns + 6 ns + 1 ns) - (3 ns + 9ns + 3 ns + 2 ns)

= 18 ns – 17 ns = + 1ns : No Hold Time Violation.

Static Time Analysis



Setup slack = Min. Clock Path Delay - Max. Data Arrival Time

= (15 ns + 2ns + 5 ns + 2 ns + 6 ns - 4 ns) - (2 ns + 11 ns +2 ns + 9 ns + 2 ns)

= 20 ns – 26 ns = 0ns : Setup Time Violation.

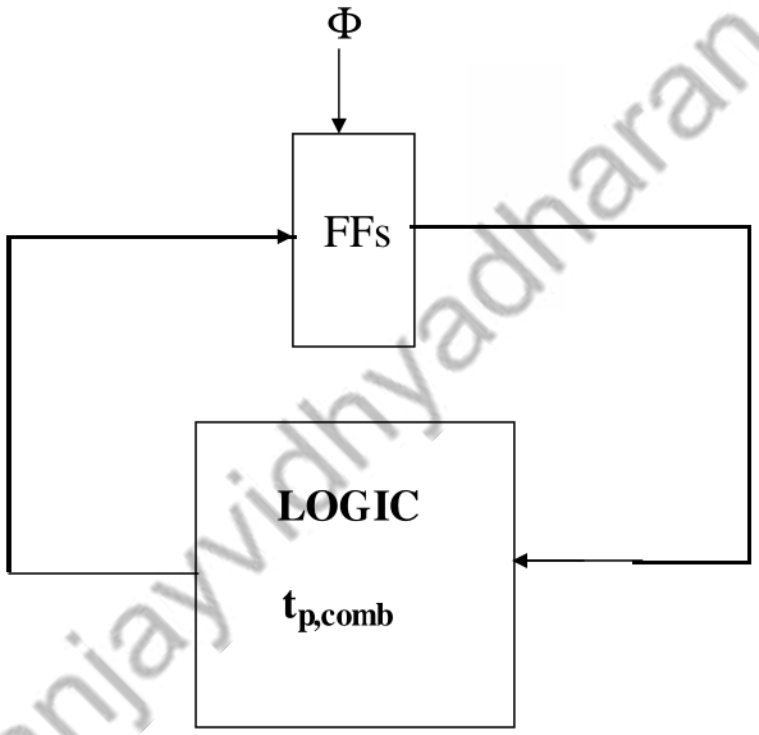
Hold time slack = Min. Data Arrival Time - Max. Clock Path Delay

= (1 ns + 9 ns + 1 ns + 6 ns + 1 ns) - (3 ns + 6 ns +9ns + 3 ns + 2) ns)

= 18 ns – 23 ns = -5ns : Hold Time Violation.

Timing Constraints of a Sequential Circuit

Maximum Clock Frequency



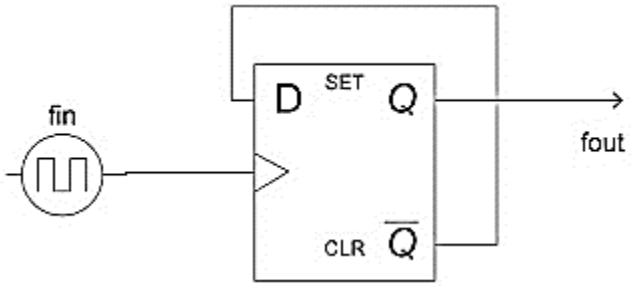
$$t_{pFF} + t_{pComb} + t_{setup} < T$$

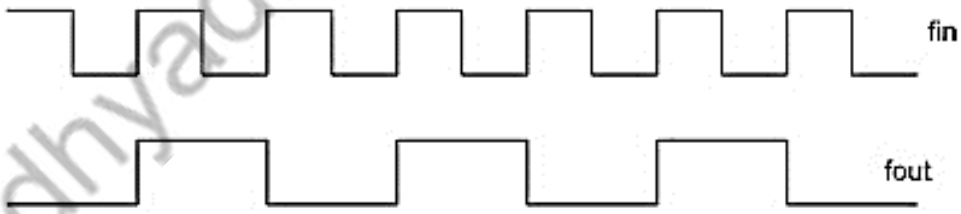
Static Time Analysis

Given the data setup time of the flop is 6ns, the hold time of the flop is 2ns, and the clock to Q delay is given as 10ns.

a. Calculate the minimum clock period required to handle the circuit by drawing a digital logic circuit for function clock frequency divided by 2.

b. Also determine the status of hold time violation and give a proper reason.





$T_{minimum} >= T_{setup\_time} + T_{clock\_Q} + dly$

$T_{minimum} >= 6ns + 10ns + 0$

$T_{minimum} >= 16ns$

$f_{maximum}$ = 1/16ns = 62.5MHz is the maximum possible frequency of operation

$T_{hold\_time} <= T_{clock\_Q} + delay$

2ns <= 10ns + 0

2ns <= 10ns No Hold Time Violation

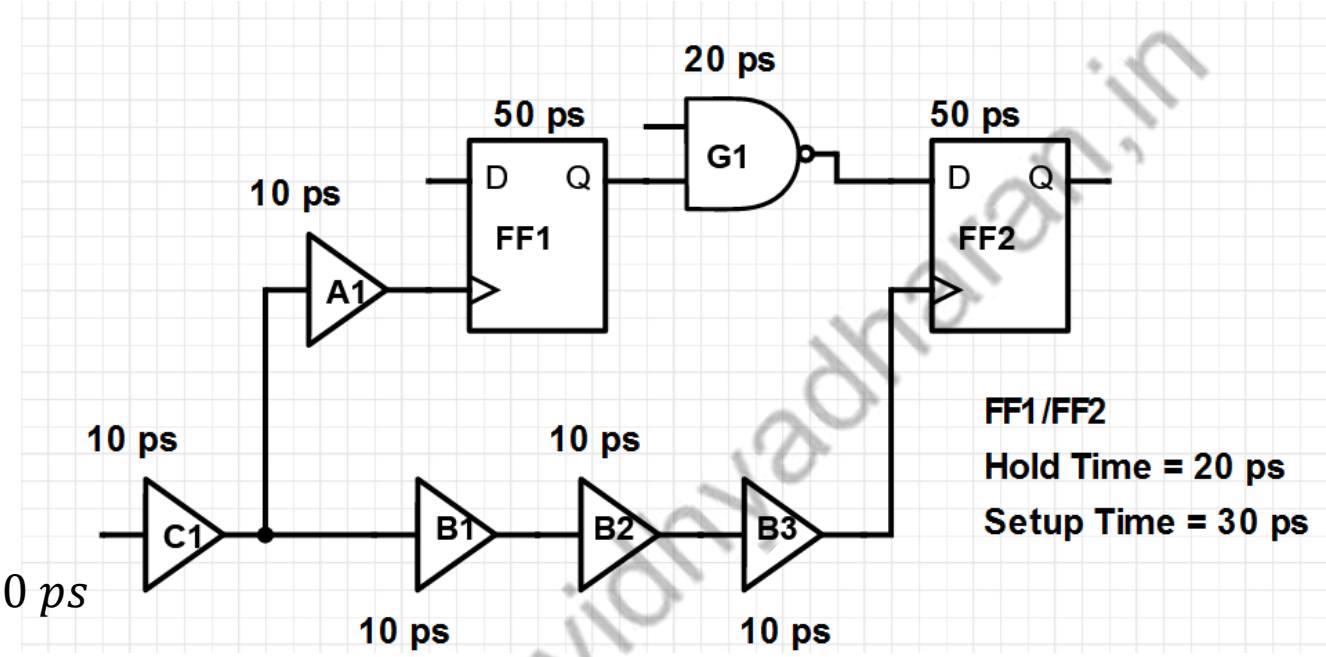
Static Time Analysis

Due to manufacturing limitations in the technology same cells show different delays and output transition times **at different locations** and different **instances of time** which is termed as on-chip variation or OCV in STA

The tool minimizes all the timing parameters that improve the timing slack by using early/fast models while for all the elements that degrade the slack the delay is maximized by using the late/slow model.

Assuming that the technology benchmark for OCV variations is +/-10%, So the launch path gets 10% faster for hold and 10% slower for setup while the converse happens with the capture path.

Static Time Analysis



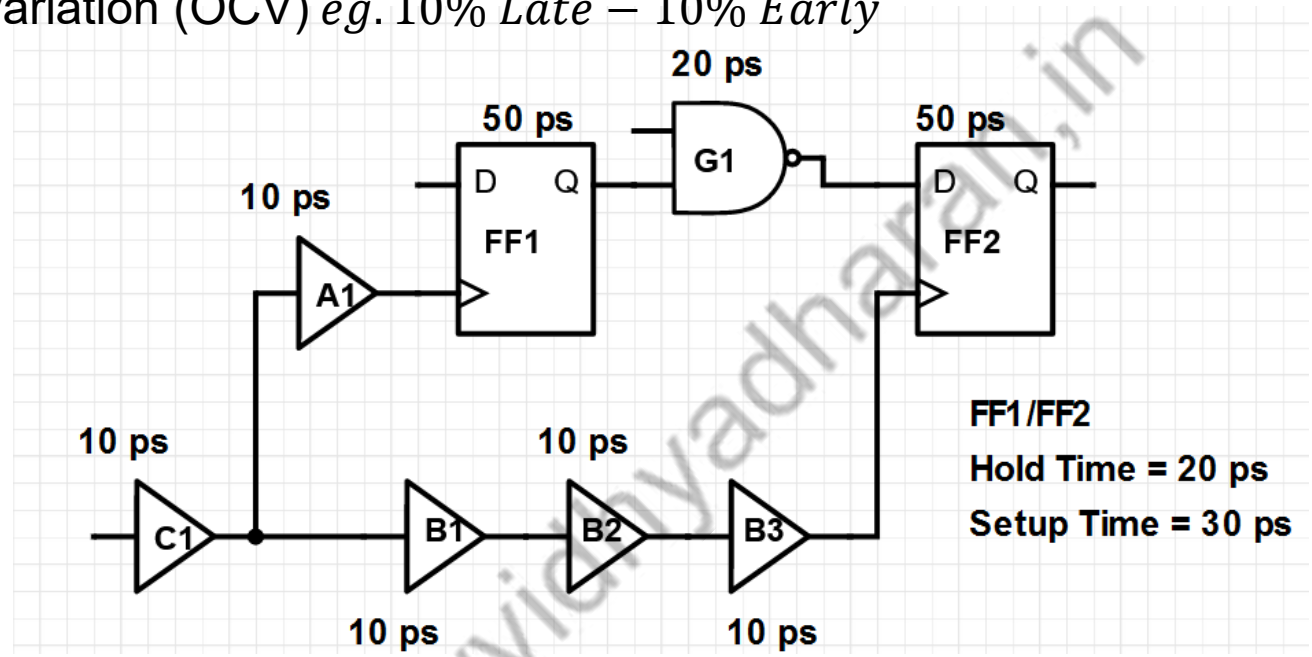
$T = 100\ ps$

$$Setup\ Slack = [100(T) + 10\ (C1) + 30(B1 - B3) - 30(t_{setup})] - [10(C1) + 10(A1) + 50(\mathrm{FF1}) + 20(\mathrm{G1})] = 20\ \mathrm{ps}$$

$$Hold\ Slack = [10(C1) + 10\ (A1) + 50(FF1) + 20(G1)] - [10(C1) + 30(B1 - B3) + 20(t_{hold})] = 30\ \mathrm{ps}$$

Static Time Analysis

On−chip variation (OCV) $eg. 10\%\ Late - 10\%\ Early$

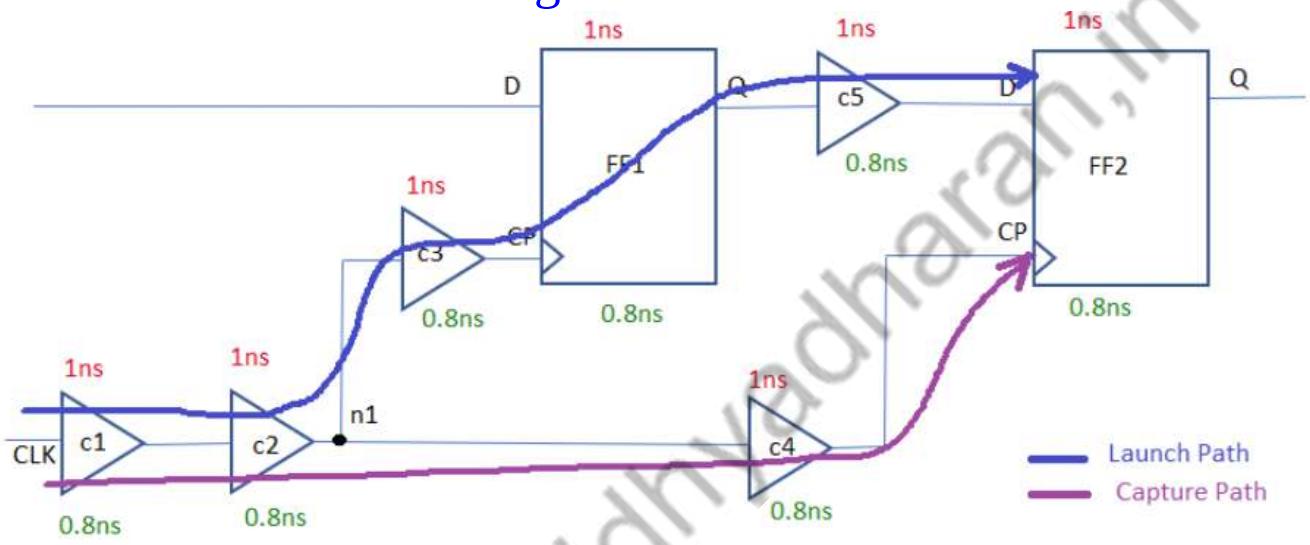


$$Setup\ Slack = \{100(T) + [10\ (C1) + 30(B1 - B3)] * 0.9 - 30(t_{setup})\}$$
$$-\{[10(C1) + 10(A1) + 50(\mathrm{FF1}) + 20(\mathrm{G1})] * 1.1\} = \cdots \ldots$$

$$Hold\ Slack = \{[10(C1) + 10\ (A1) + 50(FF1) + 20(G1)] * 0.9\}$$
$$-\{[10(C1) + 30(B1 - B3)] * 1.1 + 20(t_{hold})]\} = \cdots .. \mathrm{ps}$$

Static Time Analysis

Common Path & Clock Reconvergence Pessimism Removal



Launch path is *c1->c2->c3 -> CP-to-Q of FF1 -> c5 -> FF2/D (setup=1 ns)*

Max Data Arrival Time=1+1+1+1+1+1= 6ns

The capture path is *c1->c2->c4->FF2/CP*

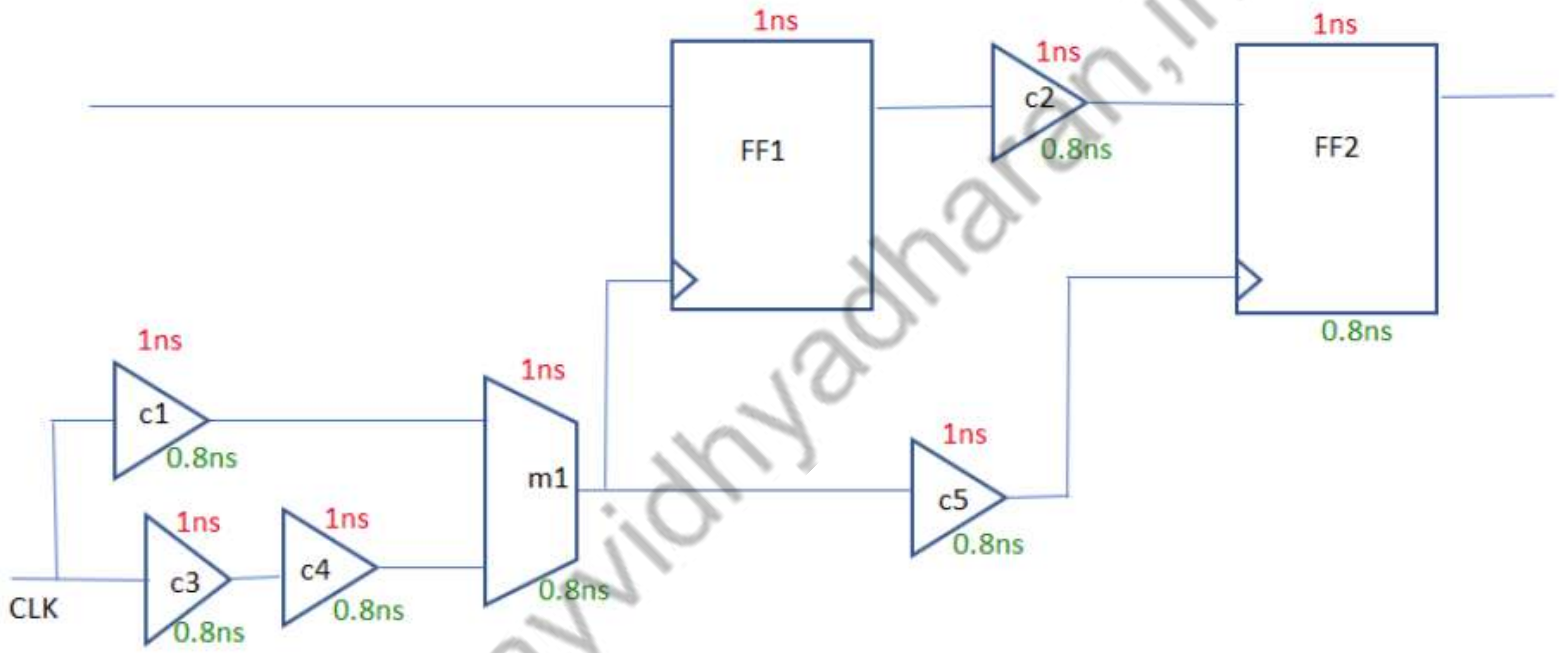
Min Clock Arrival Time=0.8+0.8+0.8+0.8 +T

CPPR Adjustment 0.4 (Assuming only Process Variation)

Mathematically this statement is only correct for paths being launched and captured at the same edge or commonly known as zero-cycle checks like default hold or zero cycle setup checks, as there is also a minor temporal component involved in variation of cells i.e. a cell will not always have same delay arcs at different instances of time.

Static Time Analysis

Common Path & Clock Reconvergence Pessimism Removal



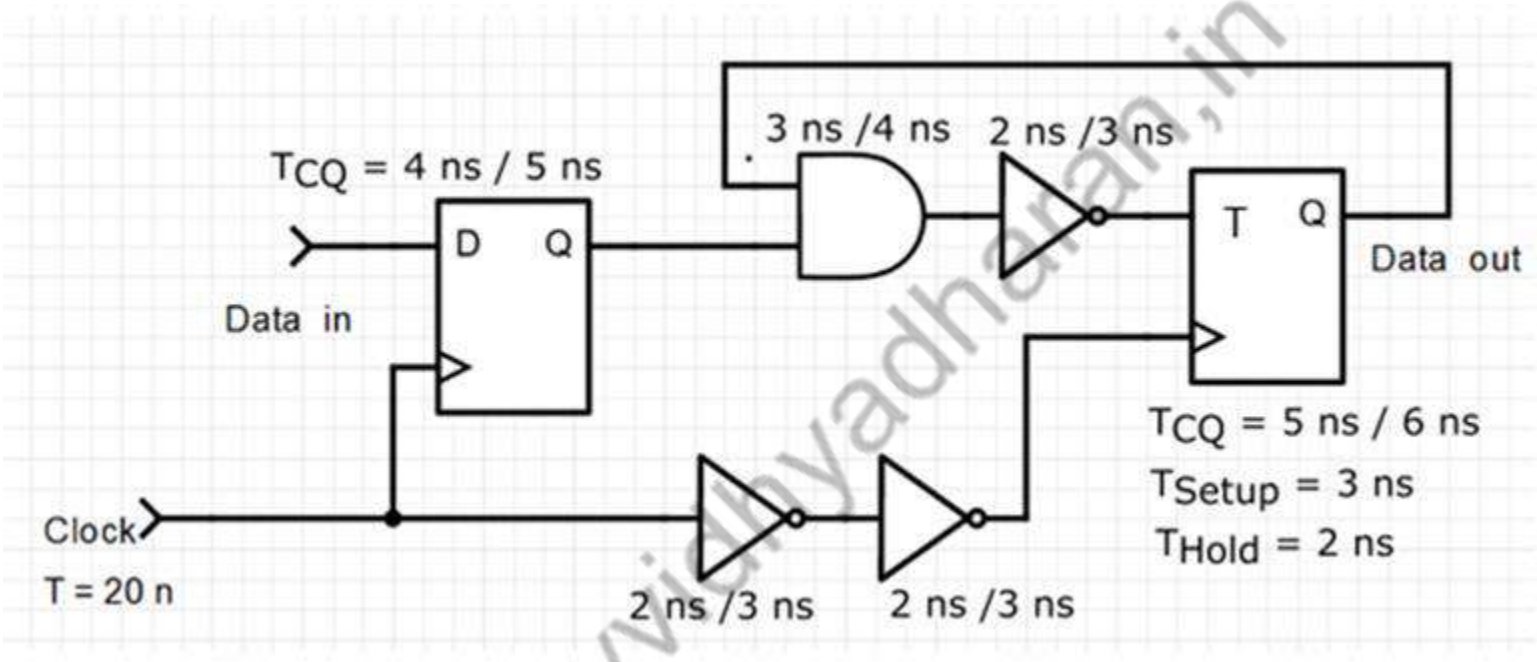
Launch path is c3->c4->m1

The capture path c1->m1->c5

Clock reconvergence pessimism: 1.4ns

Source: https://vlsi.pro/common-path-clock-reconvergence-pessimism-removal/

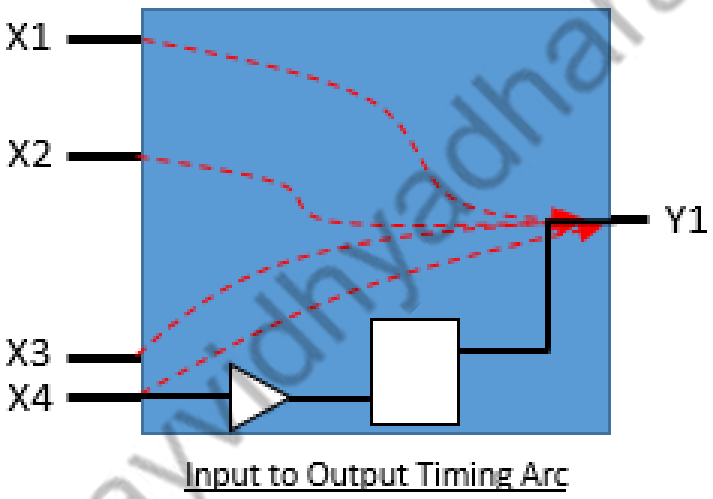
Static Time Analysis



Setup Slack = (20 + 2 + 2 – 3) – (3+3+6+4+3) = 2 ns (No Violation) Without CPPR
Setup Slack = (20 + 2 + 2 – 3) – (2+2+6+4+3) = 4 ns (No Violation) With CPPR
Hold Time Slack = (4 + 3+2) – (3+3+2) = 1 ns (No Violation)
T Min = T - Slack= 20-2= 18 ns
Max Freq = 1/18 GHz

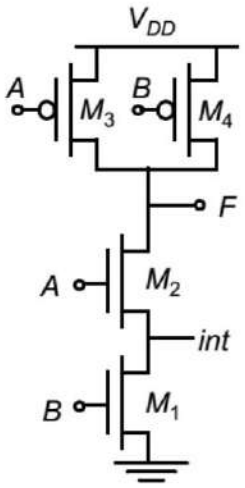
Timing ARCS

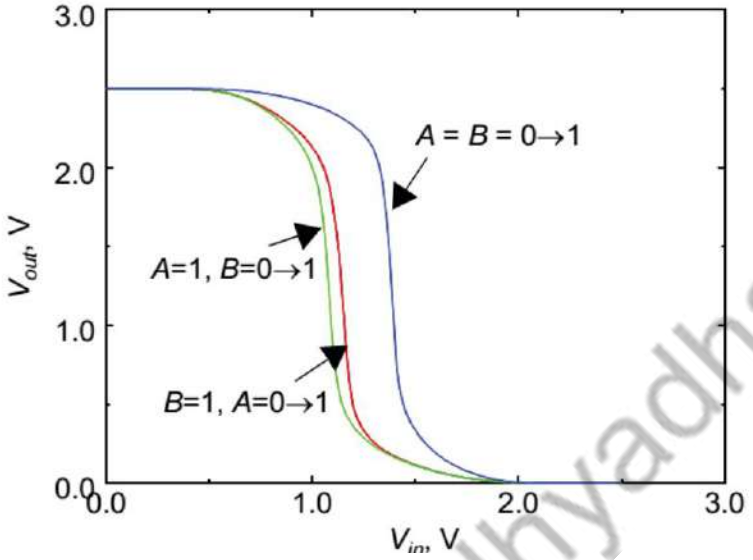
The timing arc means a path from each input to each output of the cell.



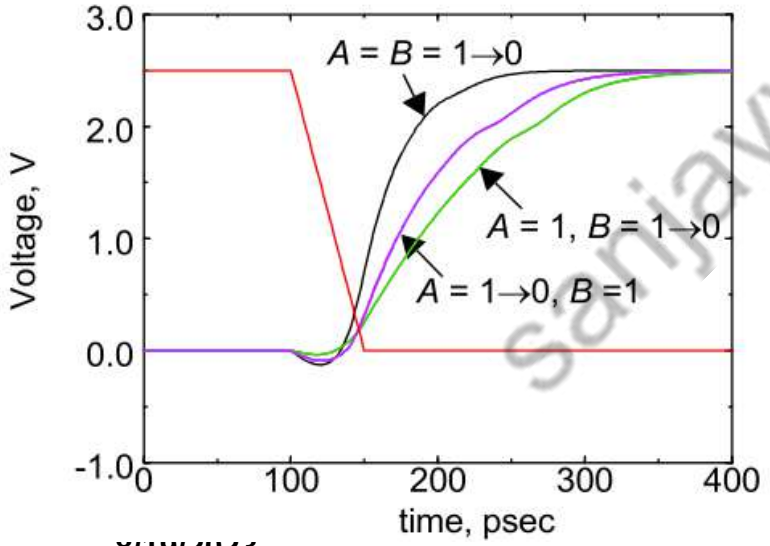
Input to Output Timing Arc

Timing ARCS





Noise Margin and Delays are input/pattern dependent!!



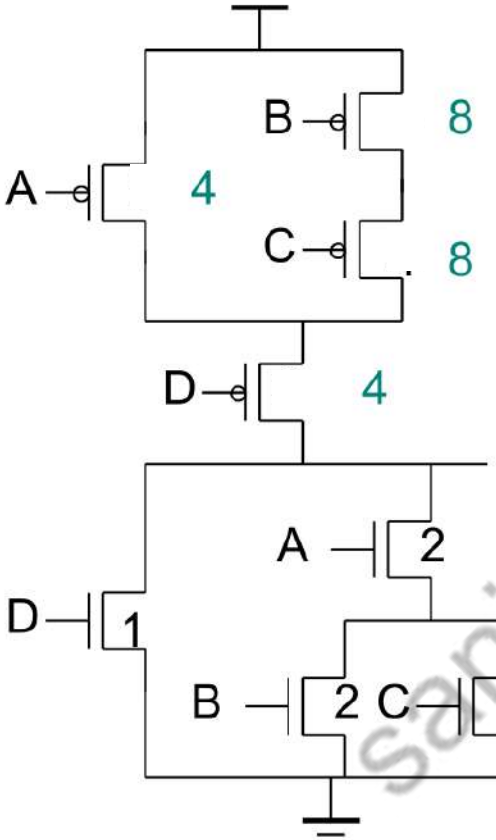
Input Data Pattern	Delay (psec)
$A = B = 0 \rightarrow 1$	69
$A = 1, B = 0 \rightarrow 1$	62
$A = 0 \rightarrow 1, B = 1$	50
$A = B = 1 \rightarrow 0$	35
$A = 1, B = 1 \rightarrow 0$	76
$A = 1 \rightarrow 0, B = 1$	57

Timing ARCS

Shortest Path First Sizing

$$R_N = \frac{12.5}{(W/L)_n}\ \text{k}\Omega \qquad R_P = \frac{30}{(W/L)_p}\ \text{k}\Omega$$

OUT = !(D + A • (B + C))

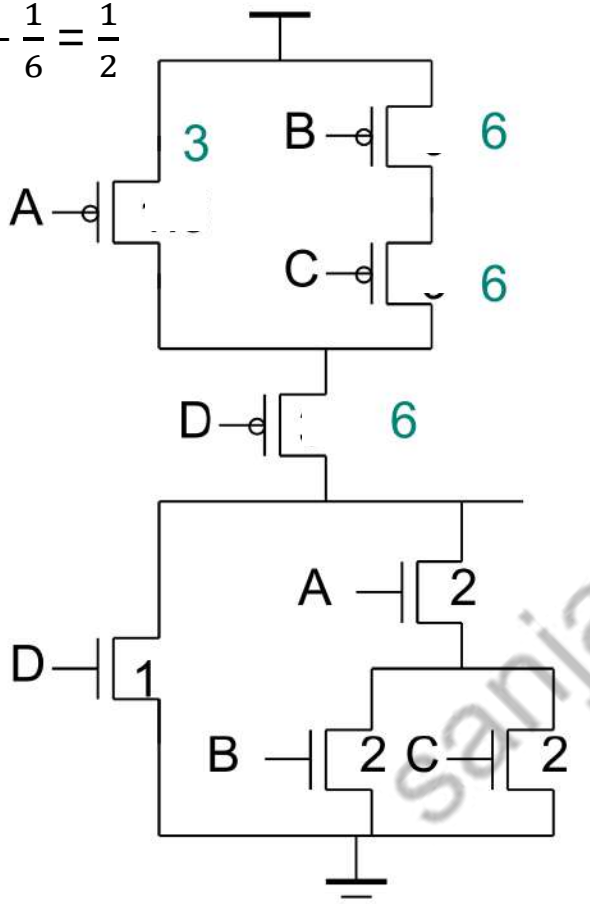


- Total Wp=24
- Shortest path resistance:
  - $Rp_{eff} = \beta(1/4 + 1/4)$
    $= 2 \times (1/2) = 1$
    (same as for an inverter)
- Worst case path resistance:
  - $Rp_{eff} = \beta(1/8 + 1/8 + 1/4)$
    $= 2 \times (1/2) = 1$
- Best case pull up resistance:
  - $Rp_{eff} = \beta\,[((1/8 + 1/8) \,||\, (1/4)) + 1/4]$
    $= \beta\,[1/8 + 1/4] = (3/8)\boldsymbol{\beta} = 0.75$

Timing ARCS

Worst Path First Sizing

$\frac{1}{X} + \frac{1}{6} = \frac{1}{2}$



OUT = !(D + A • (B + C))

- Total Wp=21 (less area, intrinsic cap)
- Worst case path resistance:
  - $Rp_{eff} = \beta(1/6 + 1/6 + 1/6)$
    $= 2 \times (1/2) = 1$
    (same as for an inverter)
- Shortest path resistance:
  - $Rp_{eff} = \beta(1/3 + 1/6)$
    $= 2 \times (1/2) = 1$
- Best case pull up resistance:
  - $Rp_{eff} = \beta\,[((1/6 + 1/6) \,||\, (1/3)) + 1/6]$
    $= \beta\,[1/6 + 1/6] = (1/3)\boldsymbol{\beta} = 0.66$

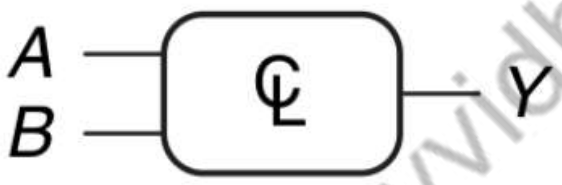
(even better than shortest path first sizing!)

Creates larger disparity in delays as a function of inputs

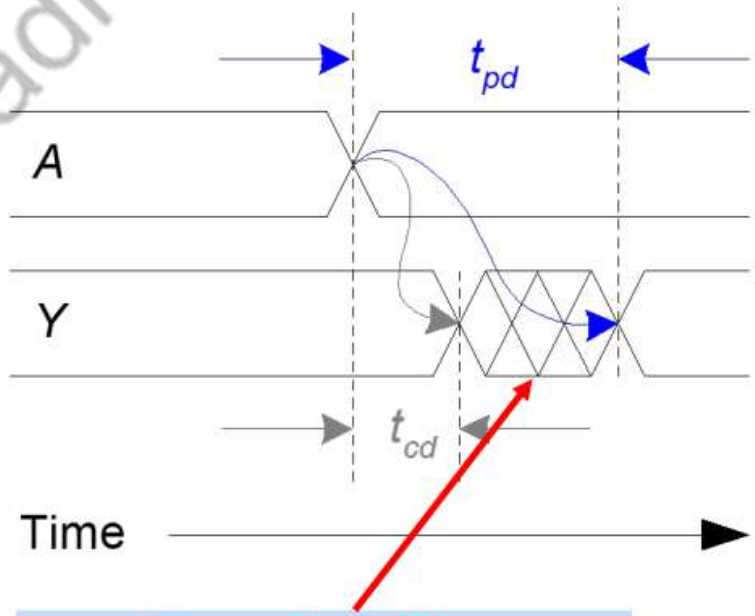
Timing ARCS

- **Contamination delay (t_{cd}): *minimum* delay**
- **Propagation delay (t_{pd}): *maximum* delay**

Example Circuit

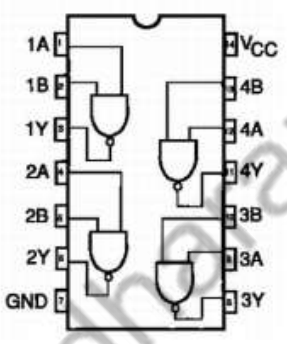


Effect of Changing Input 'A'



Cross-hatching means value is changing

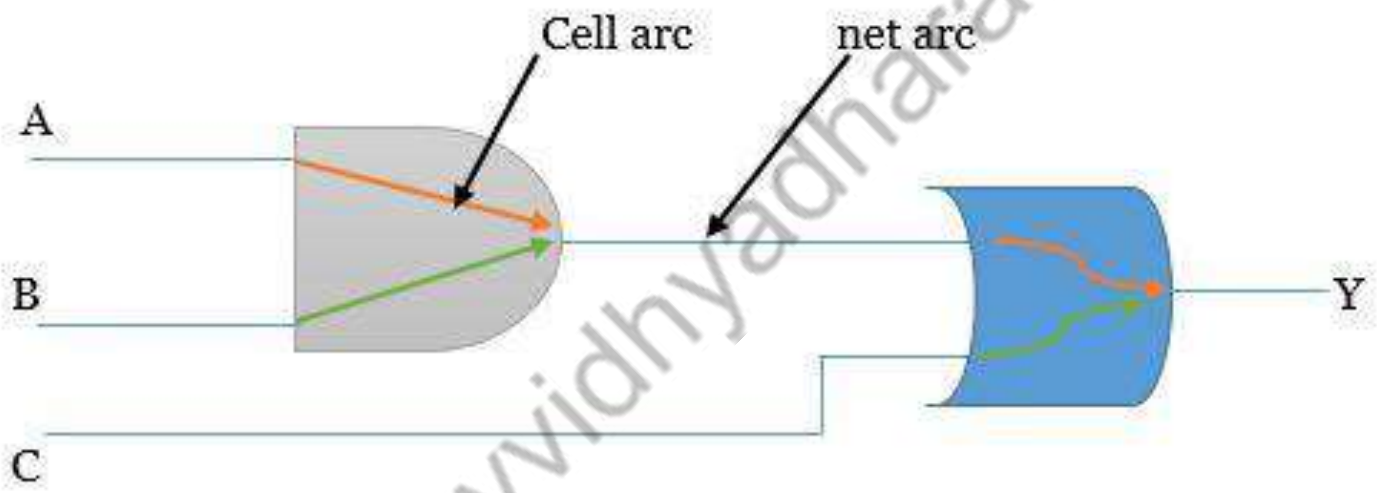
Timing ARCS



Symbol	Parameter	Conditions	25 °C			–40 °C to +125 °C		Unit
			Min	Typ	Max	Max (85 °C)	Max (125 °C)	
74HC00								
t_{pd}	propagation delay	nA, nB to nY; see Figure 6 [1]						
		V_{CC} = 2.0 V	-	25	-	115	135	ns
		V_{CC} = 4.5 V	-	9	-	23	27	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	7	-	-	-	ns
		V_{CC} = 6.0 V	-	7	-	20	23	ns

- Heavy **dependence** on **voltage** and **temperature**!

Timing ARCS

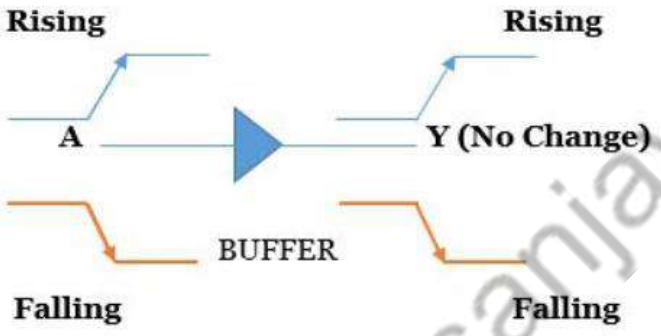


Unateness of ARCS

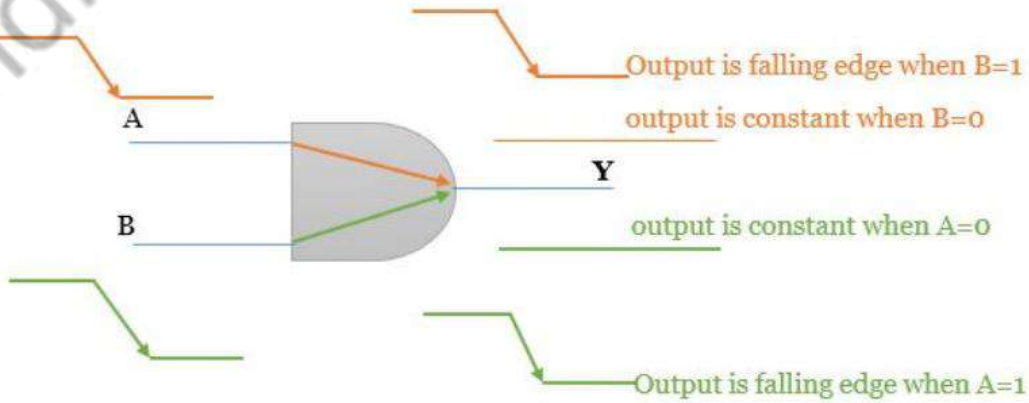
Positive unate: If a rising transition on the input gives the output to rise and falling transition on the input gives the output to fall i.e. there is no change in transition of input and output then that timing arc is called positive unate.

Example: Buffer, AND, OR gate

Buffer



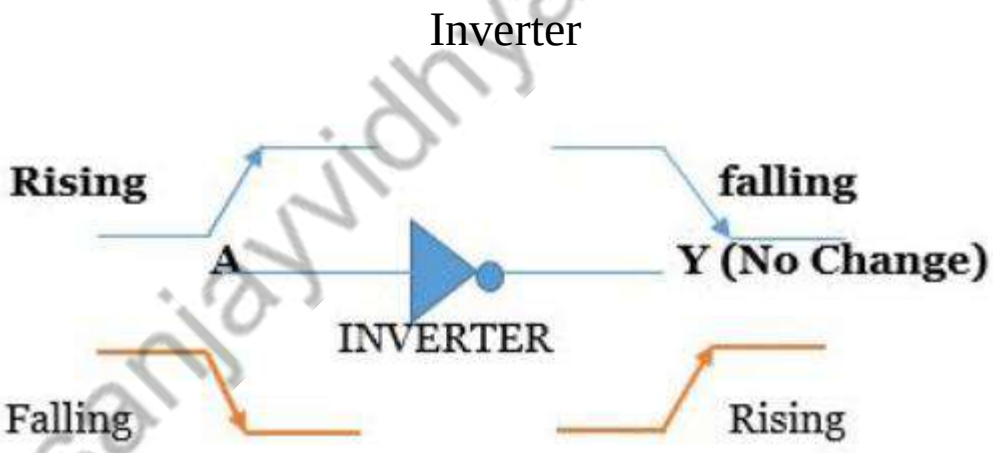
2 I/P AND (four cases for each Edge)



Unateness of ARCS

Negative unate: If a rising transition on the input gives the output to fall and falling transition on the input gives the output to rise i.e. there is a change in transition of input and output then that timing arc is called negative unate.

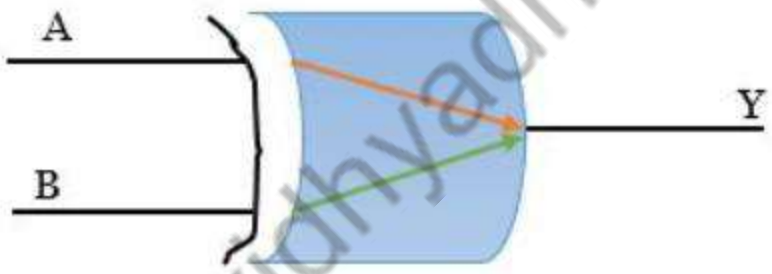
Example: inverter, NAND, NOR gate



Unateness of ARCS

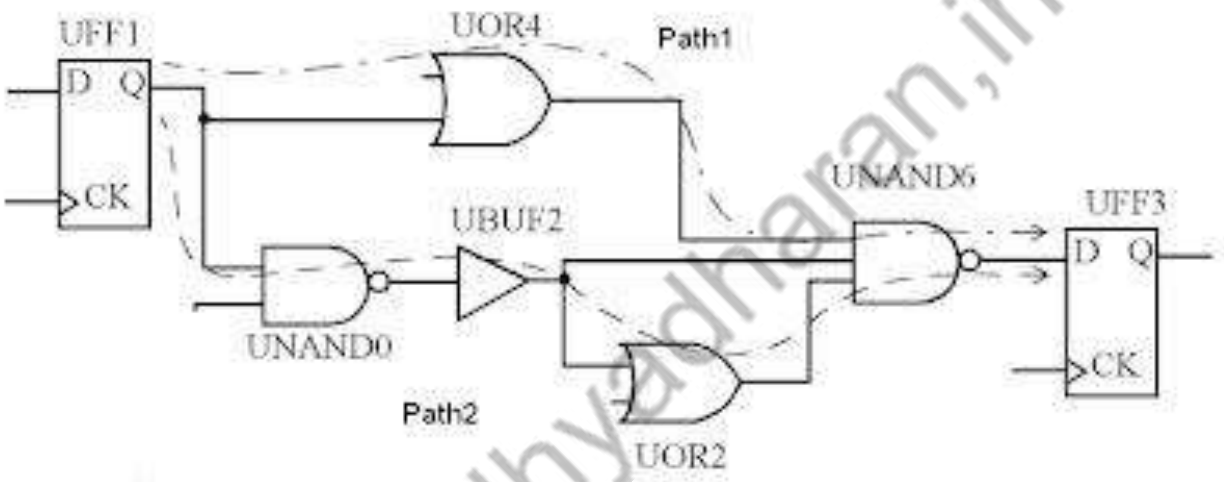
Non-unate: The output transition cannot be determined by not only the direction of an input but also depends on the state of the other inputs.

Example: XOR, XNOR gate



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Static Time Analysis



Information1:

	UOR4	UNAND6	UNAND0	UBUF2	UOR2
DELAY(ns)	5	6	6	2	5

Calculation:

Delay in Path1 : 5+6=11ns,

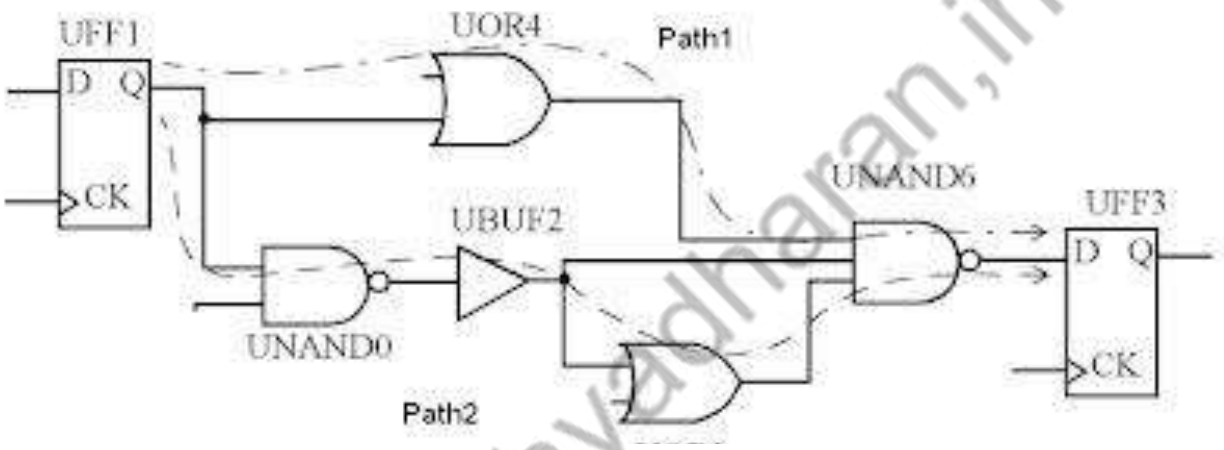
Delay in Path2: 6+2+5+6=19ns,

So

Max Delay = 19ns - Path2 - Longest Path - Worst Path

Min Delay = 11ns - Path1 - Smallest Path - Best Path

Static Time Analysis



Information2:

	UOR4	UNAND6	UNAND0	UBUF2	UOR2
Rise Delay (ns)	5	6	4	1	1
Fall Delay (ns)	6	7	3	1	1

Calculation:

Delay in Path1 : Rise Delay : 5+6=11ns, Fall Delay: 6+7=13ns

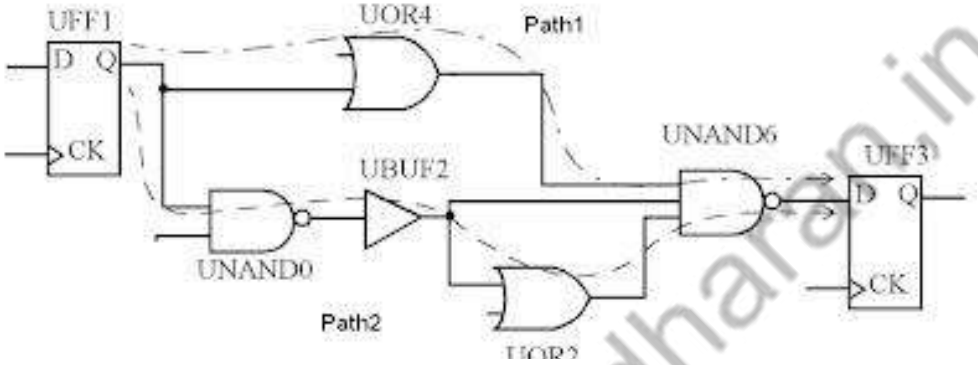
Delay in Path2: Rise Delay : 4+1+1+6=12ns, Fall Delay: 3+1+1+7=12ns

So

Max Delay = 13ns -Path1 (Fall Delay)

Min Delay = 11ns - Path1 (Rise Delay)

Static Time Analysis

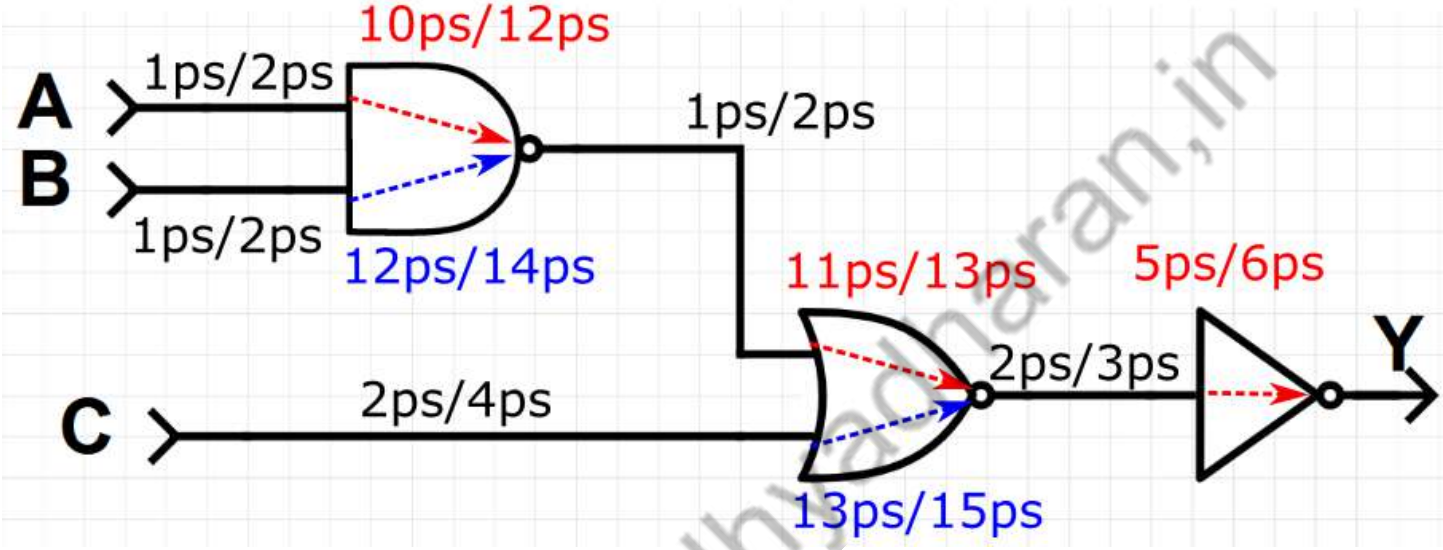


Information3:

Library	Delay	UOR4	UNAND6	UNAND0	UBUF2	UOR2
Library 1	Rise Delay (ns)	5	6	4	1	1
	Fall Delay (ns)	6	7	3	1	1
Library 2	Rise Delay (ns)	5.5	6.5	4.5	1.5	1.5
	Fall Delay (ns)	5.5	6.5	2.5	0.5	0.5

Calculation:
For Library1:
Delay in Path1 : Rise Delay : 5+6=11ns, Fall Delay: 6+7=13ns
Delay in Path2: Rise Delay : 4+1+1+6=12ns, Fall Delay: 3+1+1+7=12ns
For Library2:
Delay in Path1 : Rise Delay : 5.5+6.5=12ns, Fall Delay: 5.5+6.5=14ns
Delay in Path2: Rise Delay : 4.5+1.5+1.5+6.5=14ns, Fall Delay: 2.5+0.5+0.5+6.5=10ns
So
Max Delay = 14ns- Path1(Fall Delay)/Path2(Rise Delay)
Min Delay = 10ns - Path2(Fall Delay)

Path Based Delay



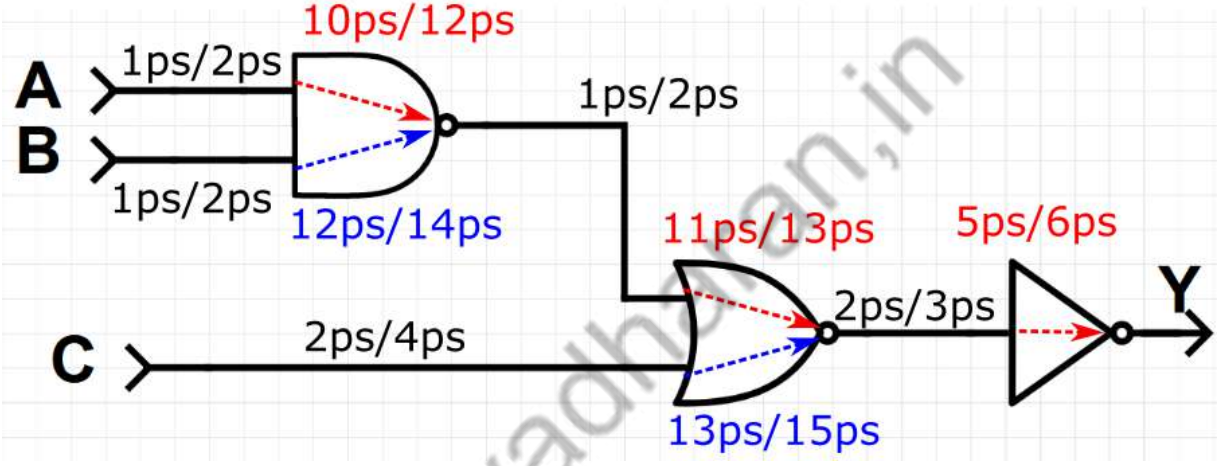
Path A-Y Max Delay = 2+12+2+13+3+6 = 38 ps Min Delay = 1+10+1+11+2+5= 30

Path B-Y Max Delay = 2+14+2+13+3+6 = 40 ps Min Delay = 1+12+1+11+2+5= 32

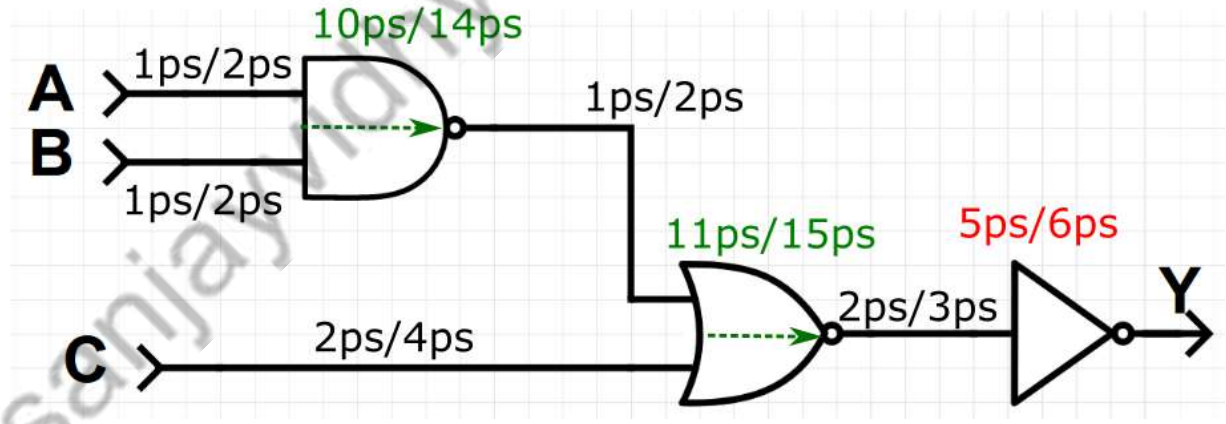
Path C-Y Max Delay = 4+15+3+6 = 28 ps Min Delay = 2+13+2+5= 22

Path Based Delay vs. Graph Based Delay

Path Based Delay



Graph Based Delay

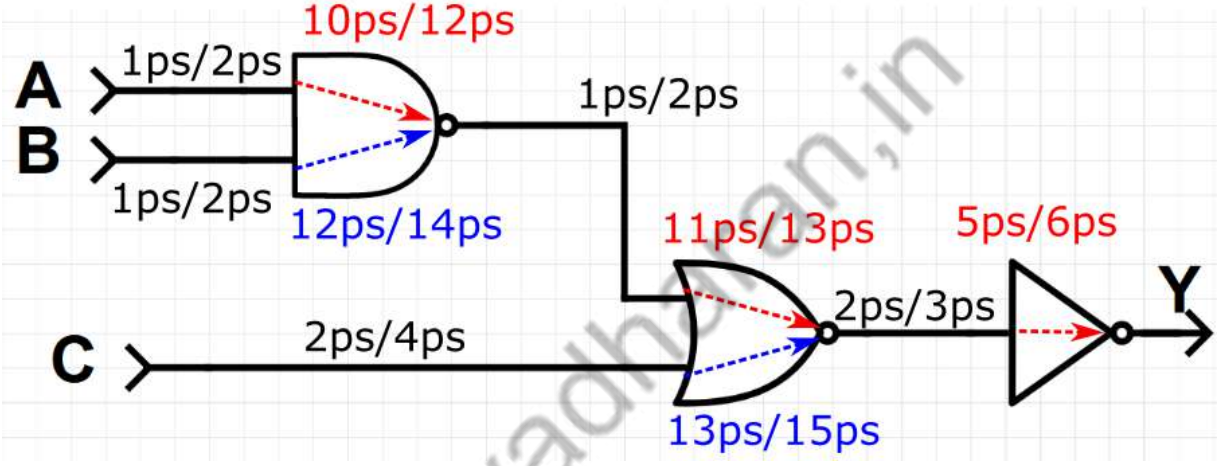


PBM Path A-Y Max Delay = 2+12+2+13+3+6 = 38 ps Min Delay = 1+10+1+11+2+5= 30

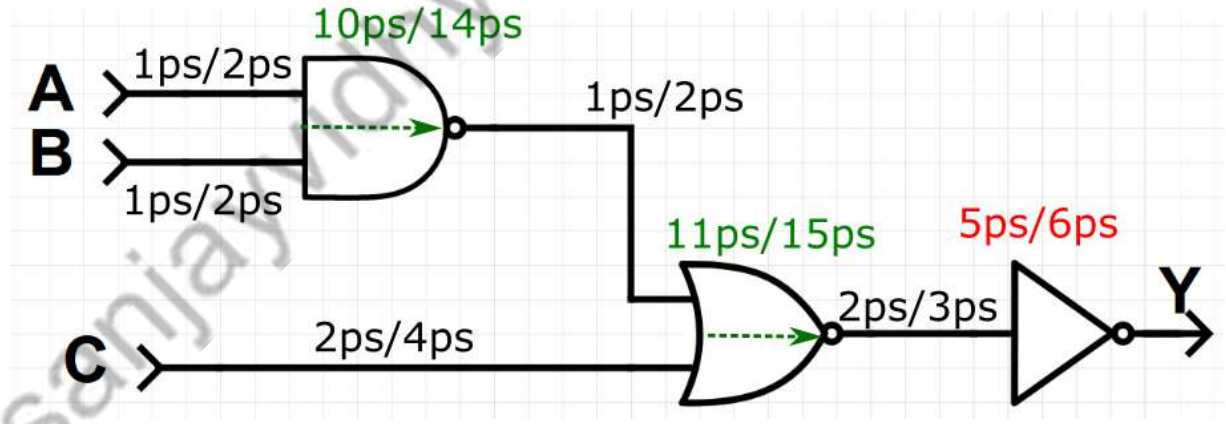
GBM Path A-Y Max Delay = 2+14+2+15+3+6 = 42 ps Min Delay = 1+10+1+11+2+5= 30

Path Based Delay vs. Graph Based Delay

Path Based Delay



Graph Based Delay

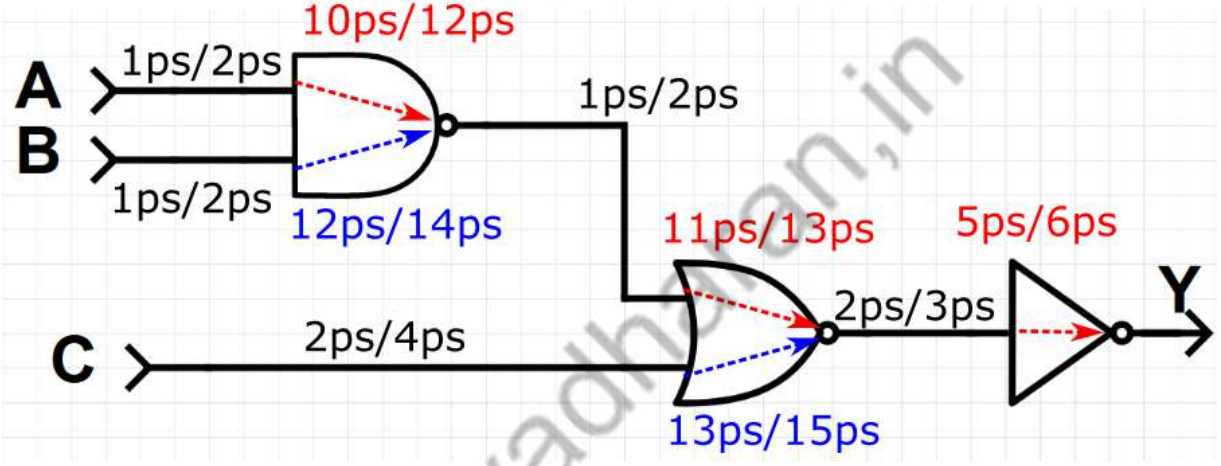


Path B-Y Max Delay = 2+14+2+13+3+6 = 40 ps Min Delay = 1+12+1+11+2+5= 32

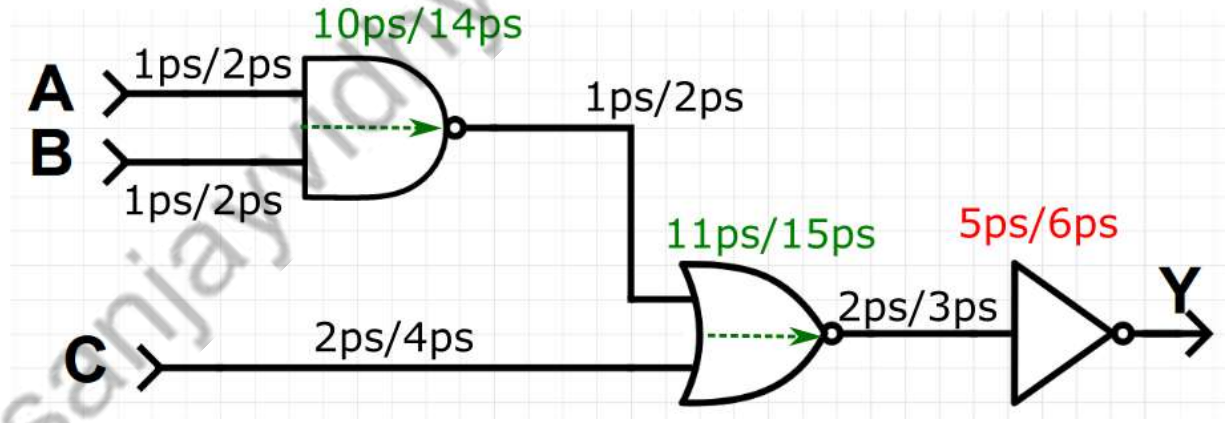
GBM Path B-Y Max Delay = 2+14+2+15+3+6 = 42 ps Min Delay = 1+10+1+11+2+5= 30

Path Based Delay vs. Graph Based Delay

Path Based Delay



Graph Based Delay



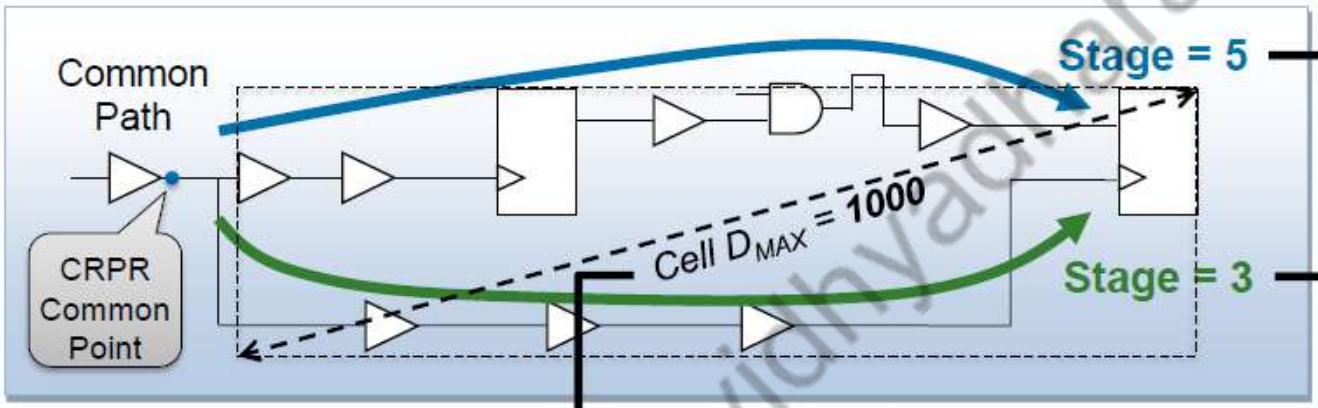
PBM Path A-Y Max Delay = 2+12+2+13+3+6 = 38 ps Min Delay = 1+10+1+11+2+5= 30

GBM Path A-Y Max Delay = 2+14+2+15+3+6 = 42 ps Min Delay = 1+10+1+11+2+5= 30

Advanced On-Chip Variation

AOCV

In A0CV derate is applied on each cell based **on path depth and distance** of the cell in the timing path and it also varies with cell type and drive strength of the cell.



Depth

Distance

	1	2	3	4	5	15
500	1.203	1.165	1.141	1.130	1.123	1.082
1000	1.204	1.166	1.142	1.131	1.124	1.084
1500	1.205	1.167	1.144	1.132	1.126	1.086

Courtesy : Synopsys AppNote

Advanced On-Chip Variation

Limitations of AOCV

- The AOCV's distance and depth-based derate factor works well for technology nodes over 40 nm, but we still need to make it better for nodes below that.

- POCV models timing as true statistical distributions
  –Delay/Transition/Constraint variation modeling

- In technology nodes 20nm and below, POCV is particularly efficient.

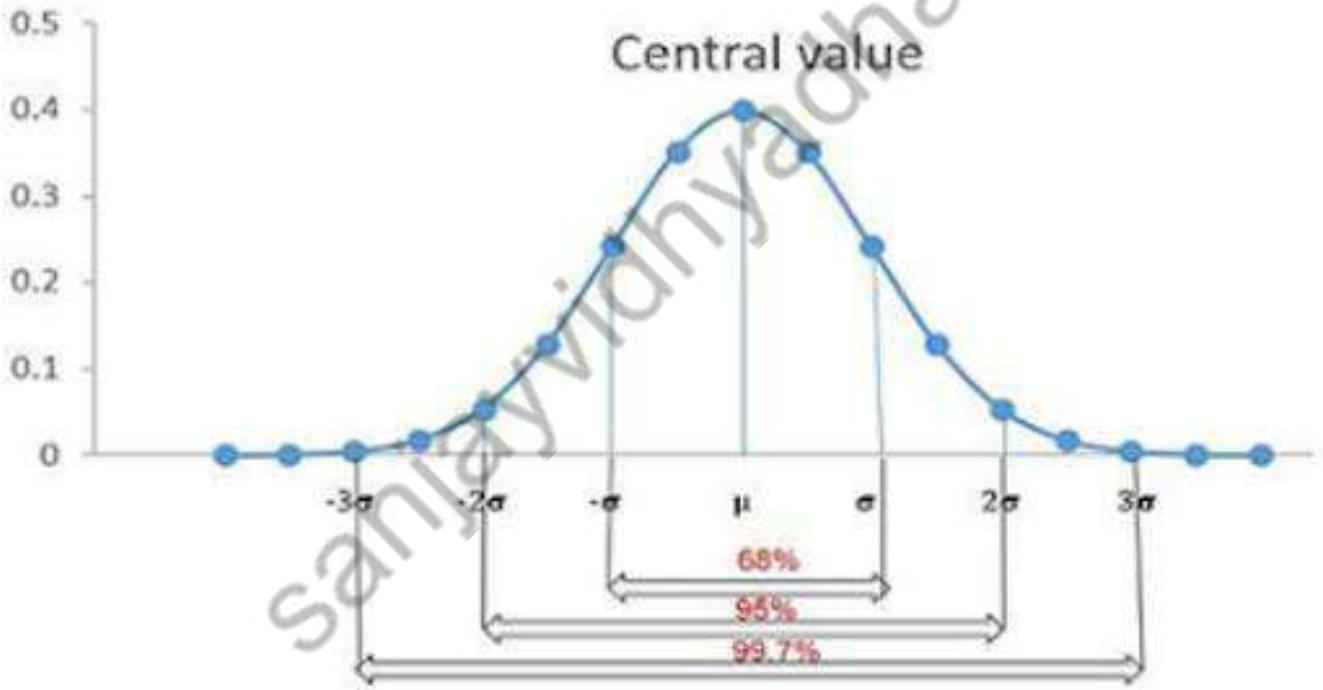
Parametric On chip Variation

POCV

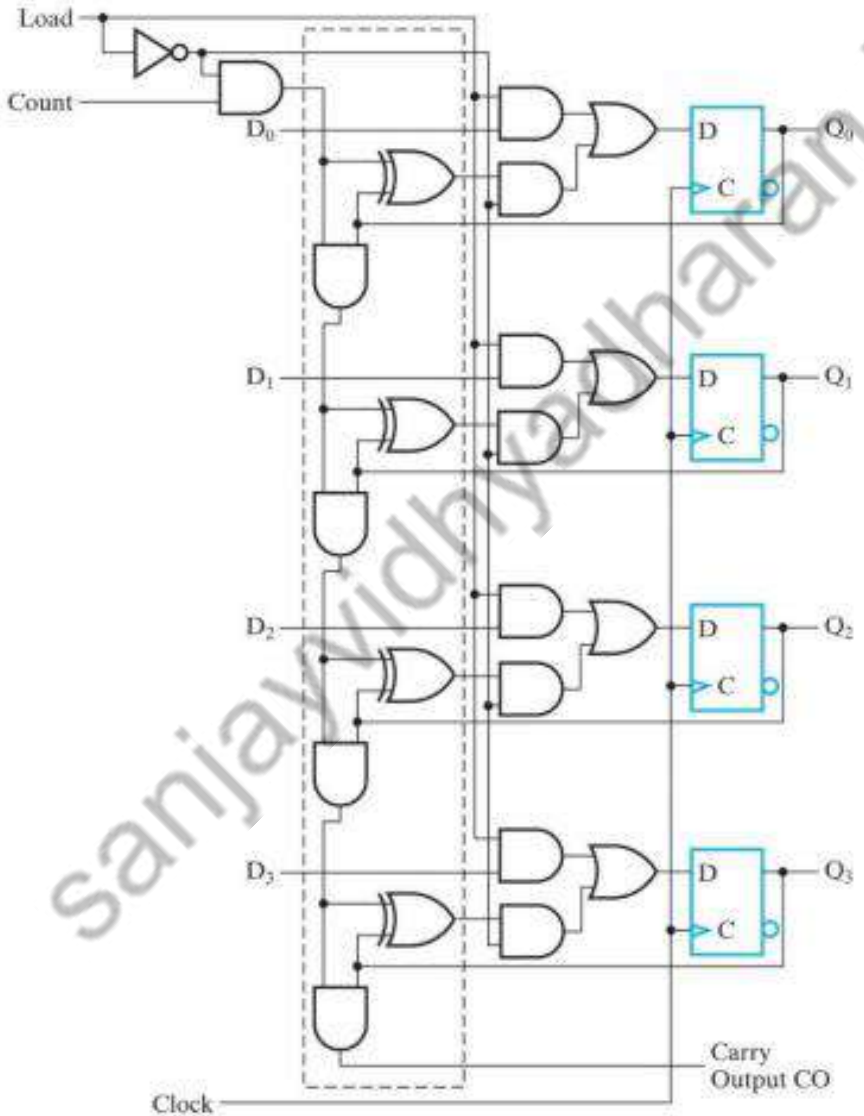
- In POCV instead of applying the specific derate factor to a cell, cell delay is calculated based on delay variation (σ) of the cell.
- In other words, the instance delay is parameterized as a function of this random variable.

Parametric On chip Variation

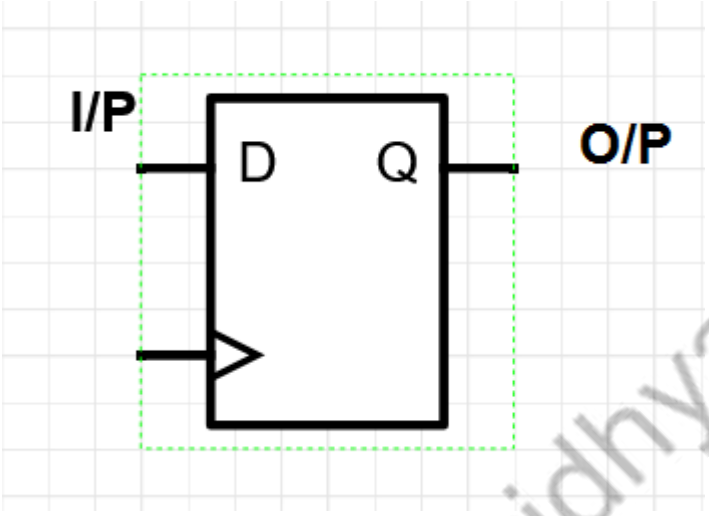
Standard Deviation of Data from Mean



Timing Constraints of a Sequential Module



Hold-time and Setup-time

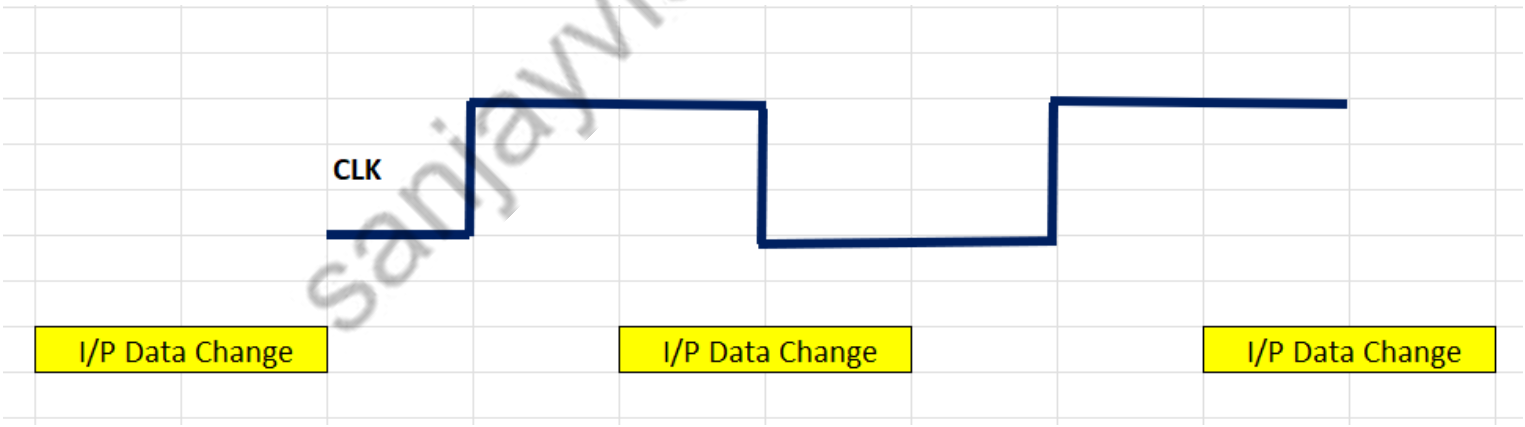


$Hold\ time\ \ 1ns$

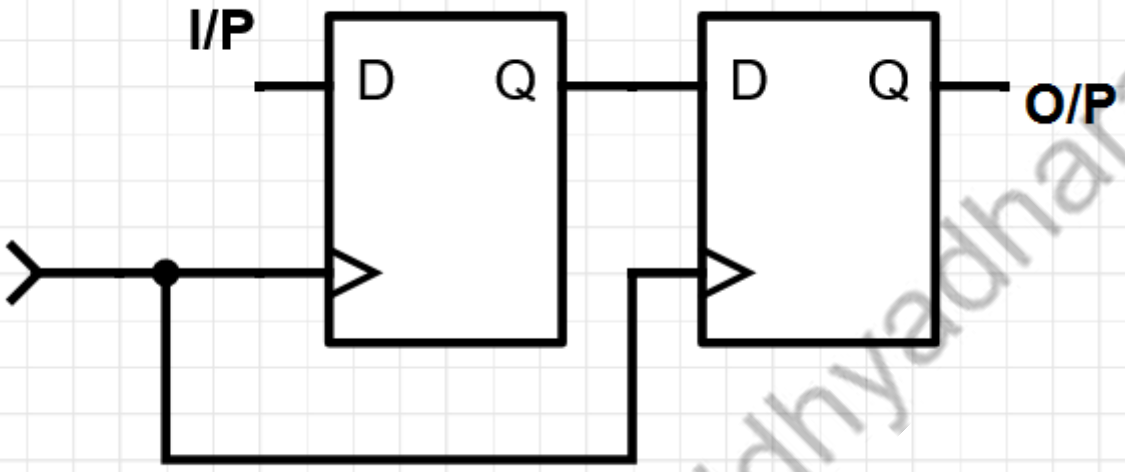
$Setup\ time\ \ 1ns$

$Tcq = 4ns$

$Max\ Freq = 1/4ns$



Hold-time and Setup-time



$Hold\ time\ \ 1ns$

$Setup\ time\ \ 1ns$

$Tcq = 4ns$

$Min\ Tclk = 4 + 1 = 5ns$

$Max\ Freq = \frac{1}{5} GHz$

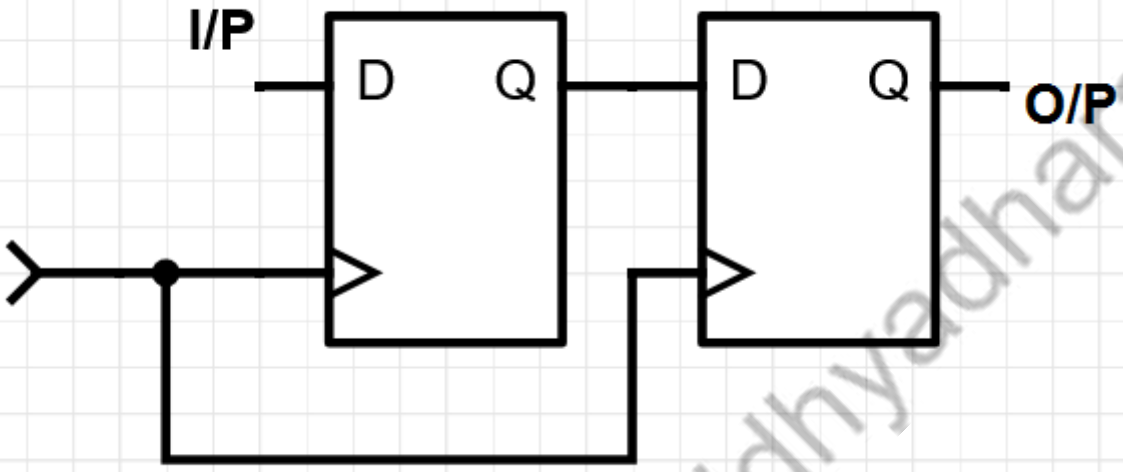
$Hold\ Slack = 4 - 1 = 3ns$

$Hold\ Slack\ and\ Hold\ Time\ are\ different$

$Setup\ Slack\ cannot\ be\ calculated\ without\ Tclk$

$Max\ Freq < \frac{1}{5} GHz$

Hold-time and Setup-time



$Hold\ time\ \ 2ns$

$Setup\ time\ \ 2ns$

$Tcq = 1ns$

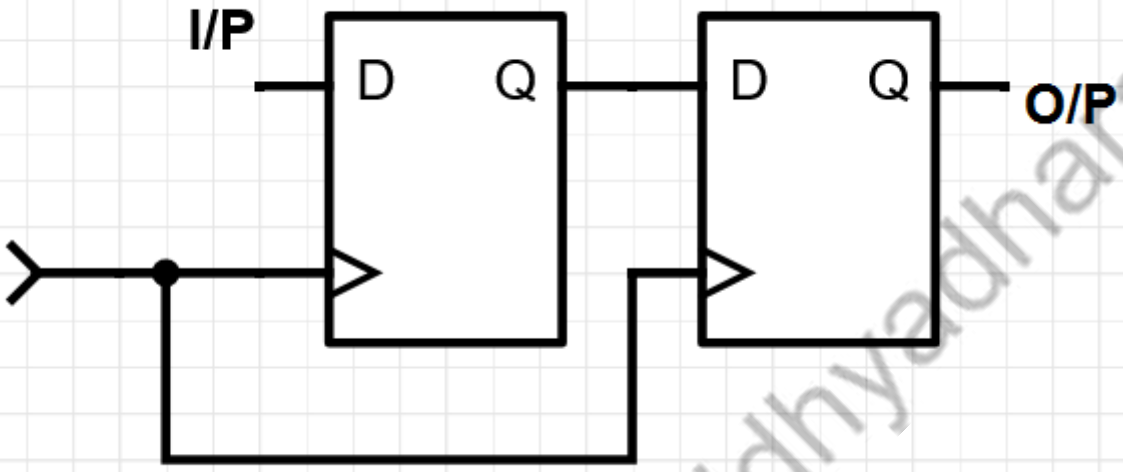
$Min\ Tclk = \ 1 + 2 = 3ns$

$Max\ Freq = \frac{1}{3} GHz$

$Hold\ Slack = 1 - 2 = -1ns$

Solution is not to change hold time of module but to delay data bewtween FFs or delay clock of launch FF

Hold-time and Setup-time



$Hold\ time\ \ 1ns$

$Setup\ time\ \ 1ns$

$Tcq = 4ns$

$Min\ Tclk = 4 + 1 = 5ns$

$Max\ Freq = \frac{1}{5} GHz$

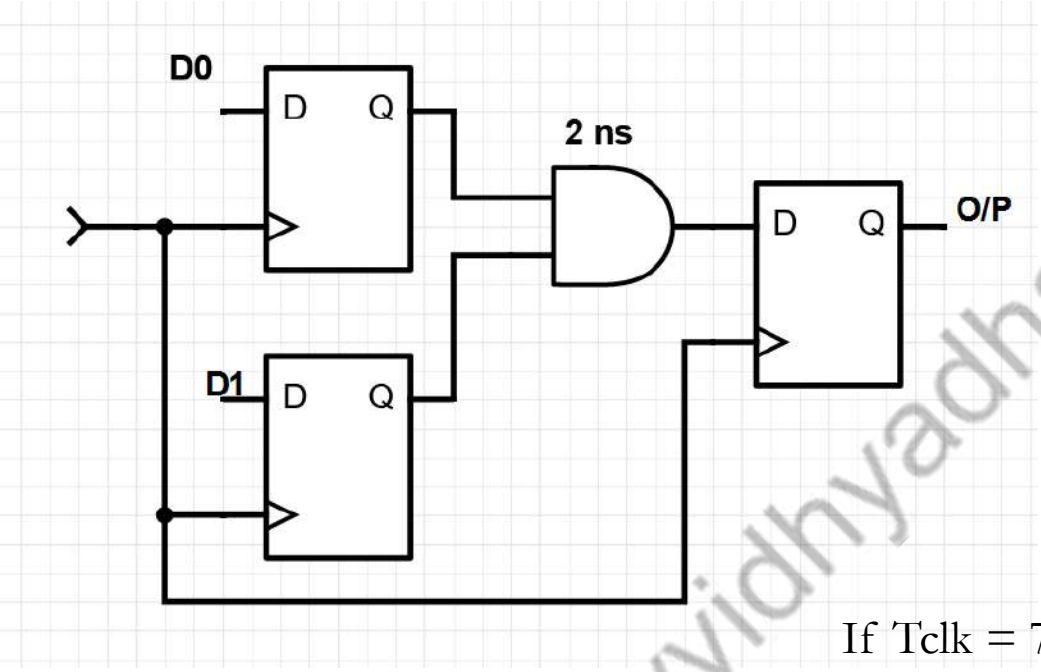
$Hold\ Slack = 4 - 1 = 3ns$

$T\ Clk = \ \ 10\ ns$

$Setup\ Slack\ = \ \ 10 - 4 - 1 = 5ns$

Setup Slack indicates we can increase the frequency of operation

Hold-time and Setup-time



$Hold\ time\ \ 1ns$

$Setup\ time\ \ 1ns$

$Tcq = 4ns$

$Min\ Tclk = 4 + 2 + 1 = 7ns$

$Max\ Freq = \frac{1}{7} GHz$

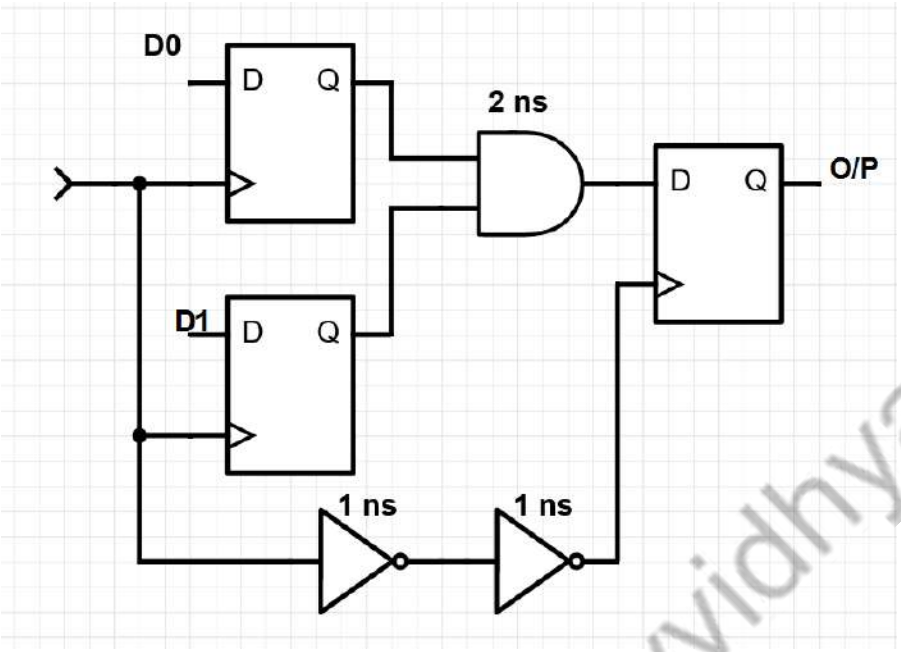
$Hold\ Slack = 4 + 2 - 1 = 5ns$

If Tclk = 7 ns
T= 0 Data Change
T = 1 ns Clk goes High (Set up 1ns)
T = 1+ 4 + 2 =7 ns Data Settles at input of FF3
T =8 ns Clock at FF3 (ins setup available)

$T\ Clk = \ \ 10\ ns$

$Setup\ Slack \ = \ \ 10 - 4 - 2 - 1 = 3ns$

Hold-time and Setup-time



$Hold\ time\ \ 1ns$

$Setup\ time\ \ 1ns$

$Tcq = 4ns$

$Min\ Tclk = 4 + 2 + 1 - 2 = 5ns$

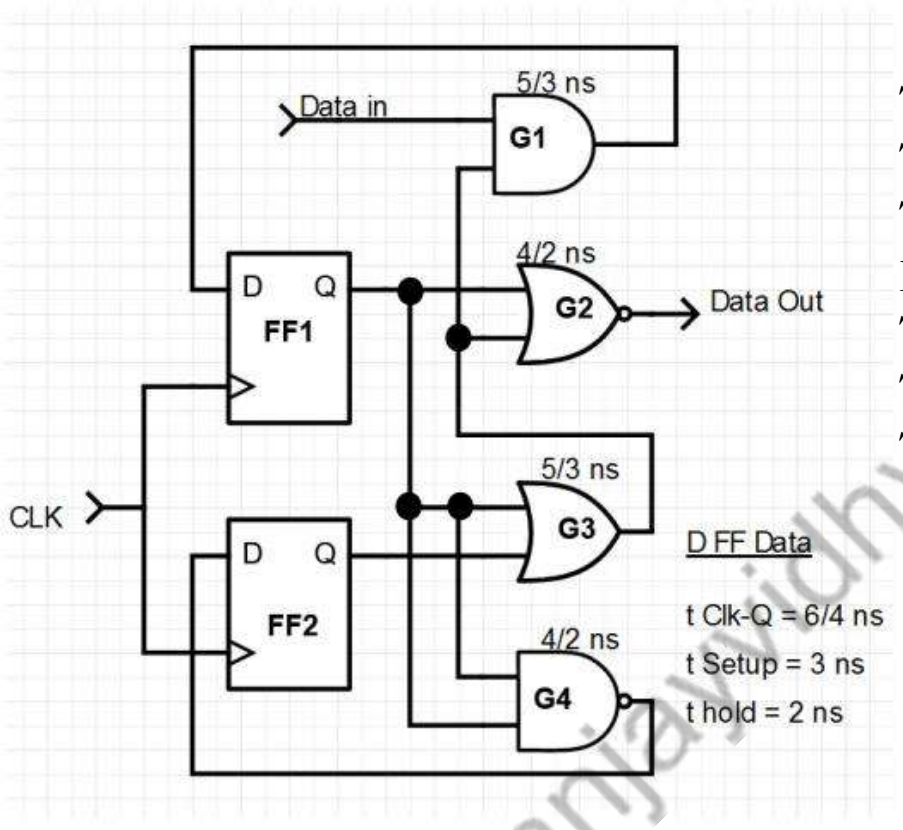
$Max\ Freq = \frac{1}{5} GHz$

$Hold\ Slack = 4 + 2 - 1 - 2ns = 3ns$

$T\ Clk = \ \ 10\ ns$

$Setup\ Slack\ = \ \ 10 + 2 - 4 - 2 - 1 = 5ns\ \ (\ doesnot\ effect\ setup\ time)$

Hold-time and Setup-time



T= 0 Data Change
T = 8 ns Clk goes High
T= 8+6 (Tc-q FF1/FF2)+5(G3)+5 (G1) = 19 ns
Data Settles at input of G1
T=19 ns Second data (27-8)
T= 19+5 = 24 ns data arrival at FF
T= 27 ns Second Clock goes high

(i) Min T Clock = 6 (Tc-q FF1/FF2) + 5 (G3) + 5 (G1) + 3 (Setup FF1) = 19 ns
(ii) Setup Time = 5 (G1) + 3 (Setup Time FF1) = 8 ns
(iii)Hold Time = 2(Hold Time FF1) - 3(G1) = - 1 ns

Thank you