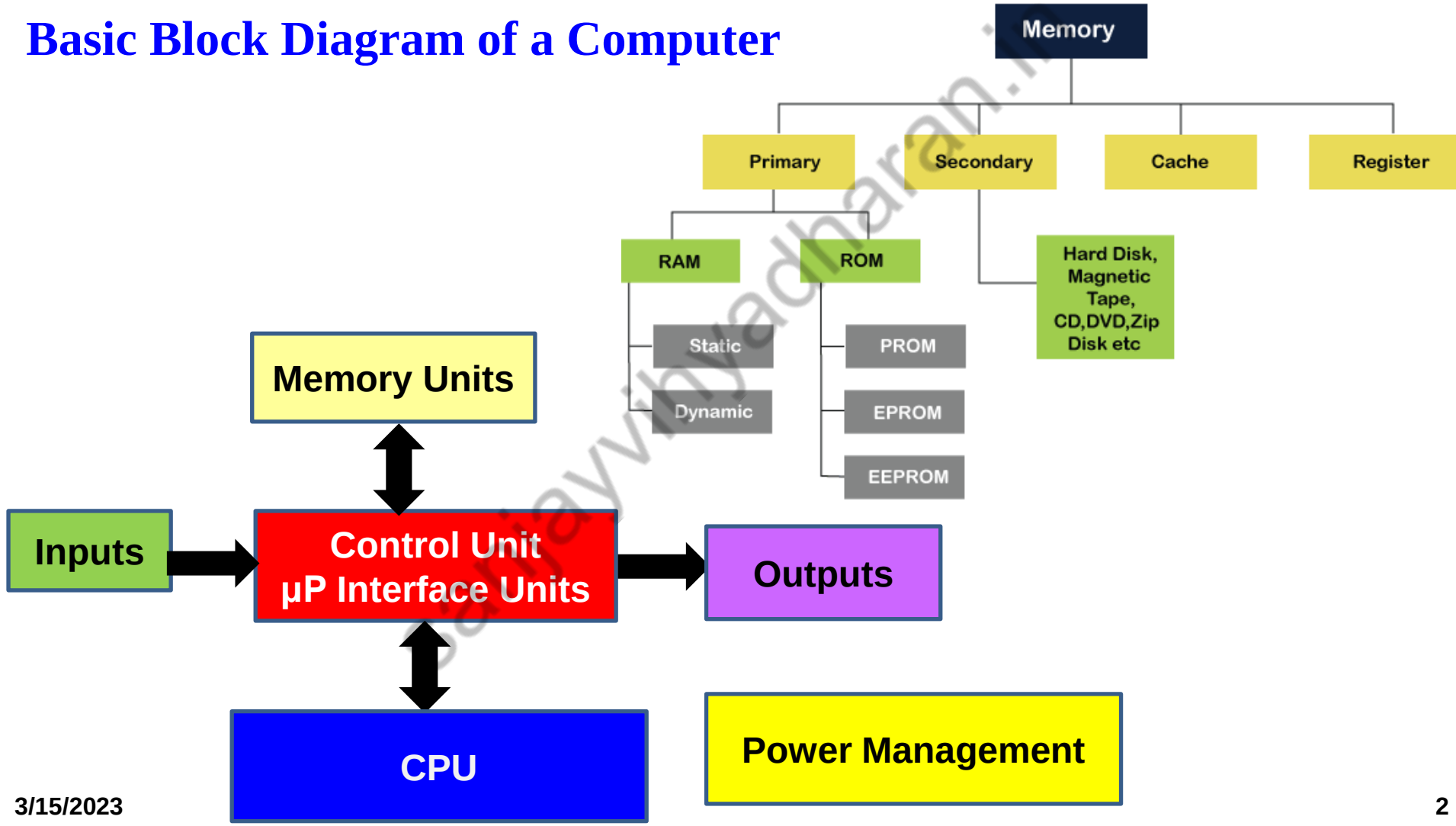
Microprocessor Programming and Interfacing

Lecture-2 : Introduction to Microprocessors

Dr. Sanjay Vidhyadharan

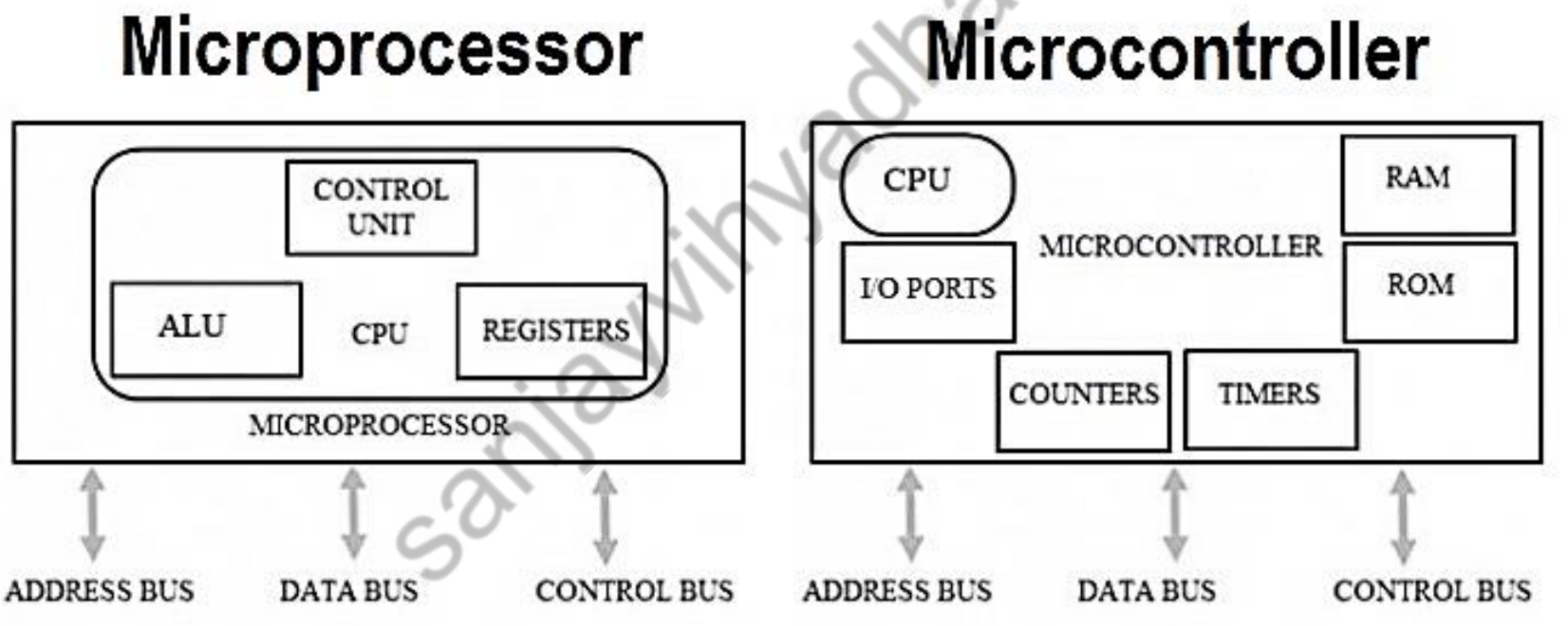
Introduction to Microprocessors

Basic Block Diagram of a Computer



Introduction to Microprocessors

Microprocessor vs. Microcontroller

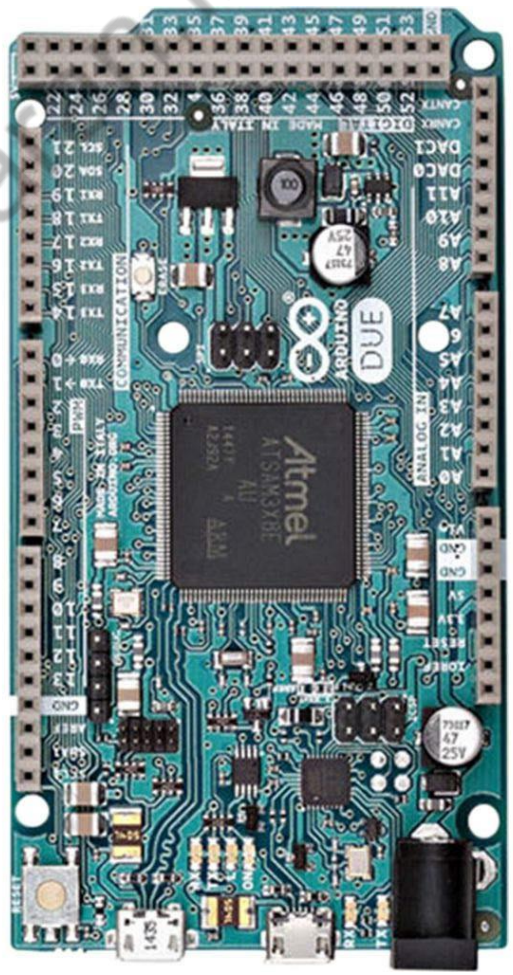


Introduction to Microprocessors

Introduction to Microprocessors

Microprocessor

Microcontroller



Instructions in Microprocessor

WHAT IS INSTRUCTIONS?

Tells the µp what action to perform

Instructions in Microprocessor

HOW DOES A MICROPROCESSOR HANDLE AN INSTRUCTION?

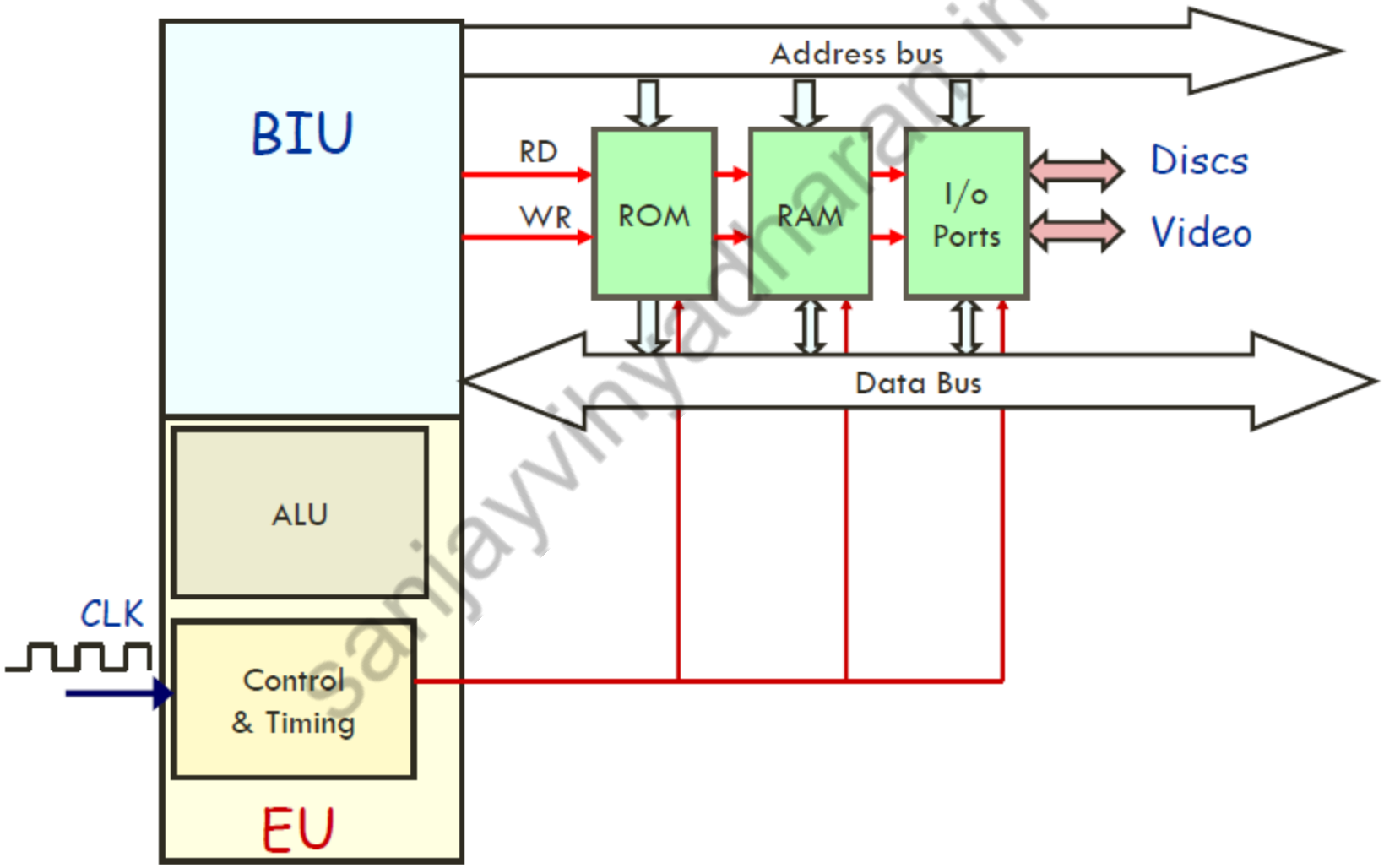
Fetch Cycle

The fetch cycle takes the instruction required from memory, stores it in the instruction register

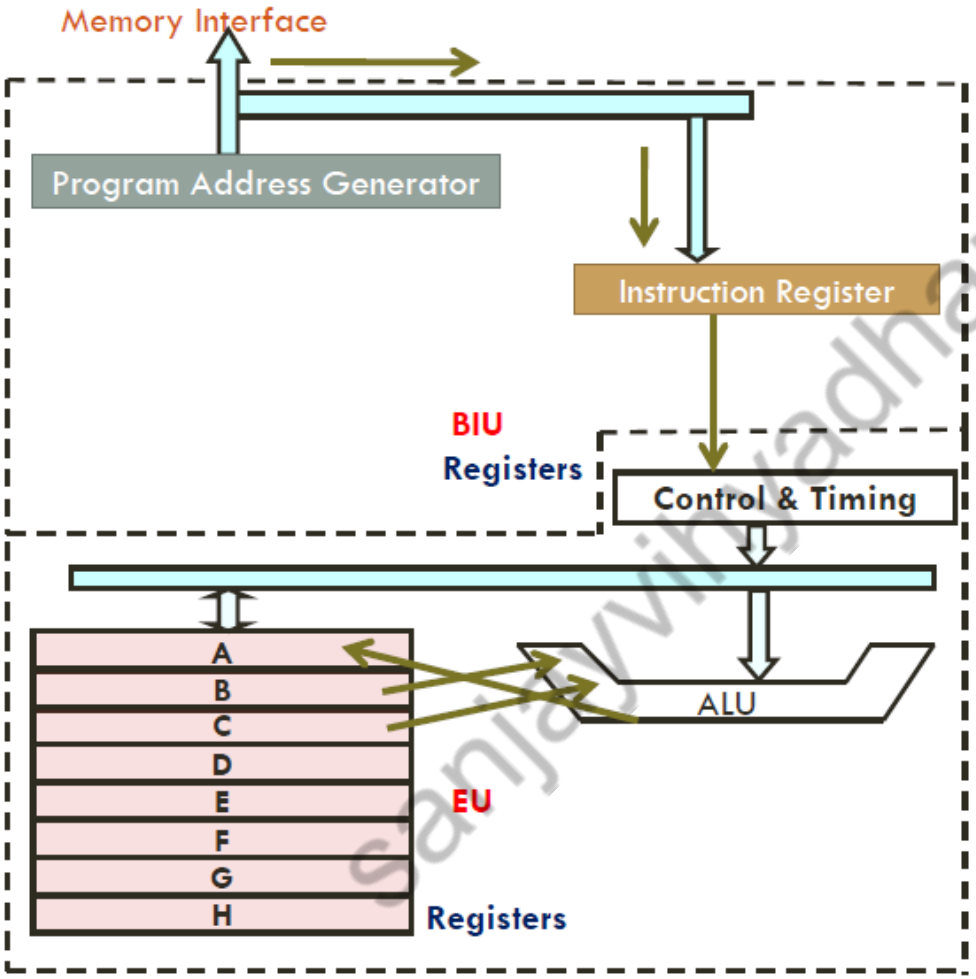
Execute Cycle

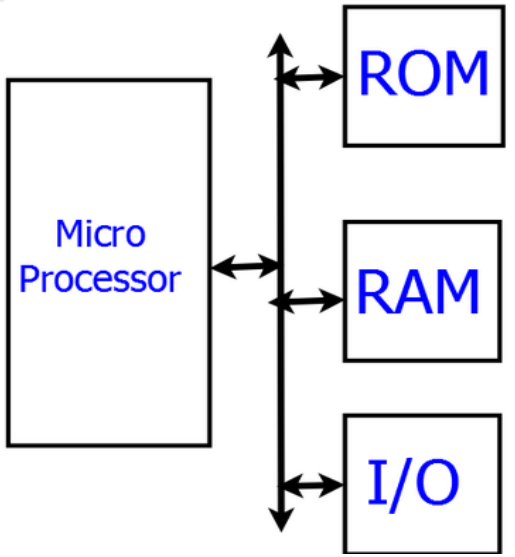
The actual actions which occur during the execute cycle of an instruction

Introduction to Microprocessors



Introduction to Microprocessors

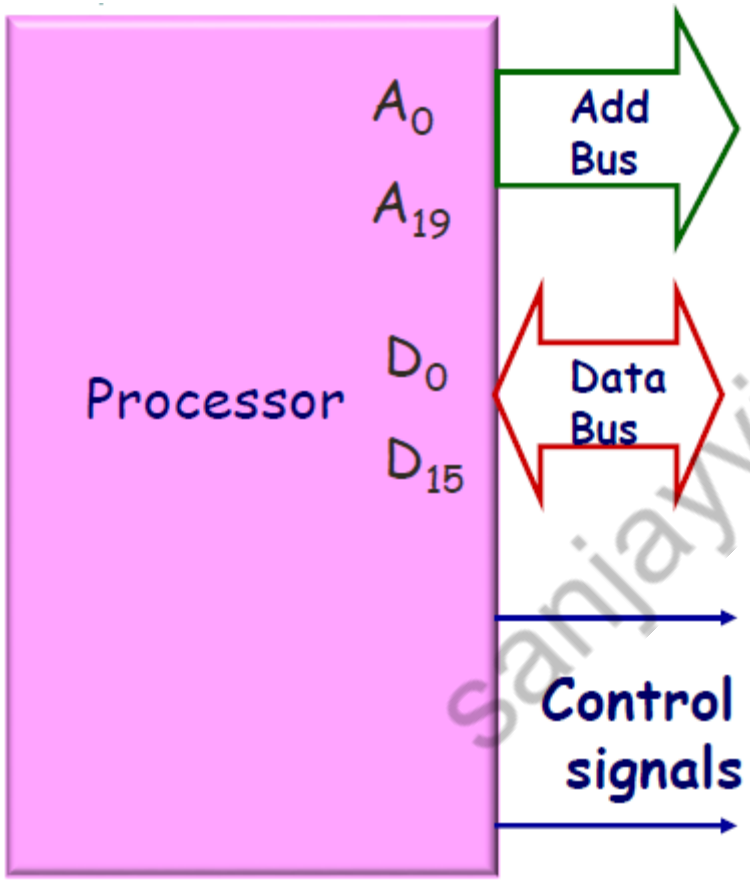




Block Diagram of a Microprocessor

Microprocessor Bus

PROCESSOR BUS



ADDRESS BUS:

No of Address lines

- 20 lines –A19–A0
- 1 M Byte of memory can be addressed

DATA BUS:

No of Data lines

- 16 lines –D15–D0

CONTROL LINES:

-Active low signals

- MEMR
- MEMW
- IOR
- IOW

Memory of Microprocessors

PROCESSOR MEMORY

- **ROM**
  - Non-Volatile
  - Read Only
- **RAM**
  - Volatile
  - Random Access Memory

Processors

- **CISC (Complex Instruction Set Computer)**

Operands for Arithmetic/Logic operation can be in Register/ Memory

- **RISC (Reduced Instruction Set Computer)**

Operands for Arithmetic/Logic operation only in Registers

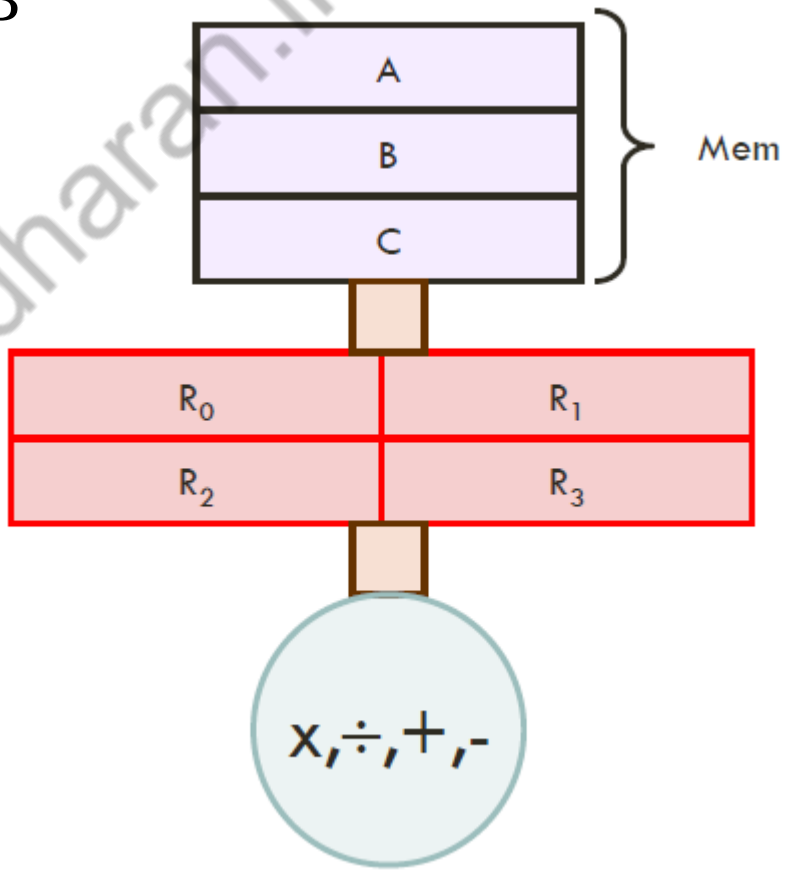
Register –Register Architecture

RISC vs CISC

Goal: Multiply data in mem A with B and put it back in A

CISC:
MUL A,B

RISC:
LDA R_0,A
LDA R_1,B
MUL R_0,R_1
STR A,R_0



RISC vs CISC

RISC vs CISC

$$\frac{\text{Time}}{\text{Program}} = \frac{\text{Time}}{\text{cycle}} \times \frac{\text{Cycles}}{\text{Inst}} \times \frac{\text{Instructions}}{\text{Program}}$$

RISC

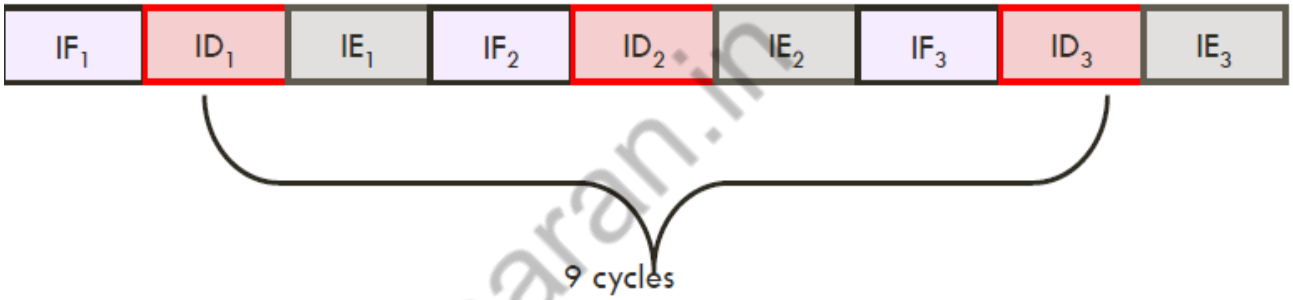
CISC

CPU-SPEEDUP

1 Instruction Per Cycle (1 IPC)

Basic Parallel Techniques

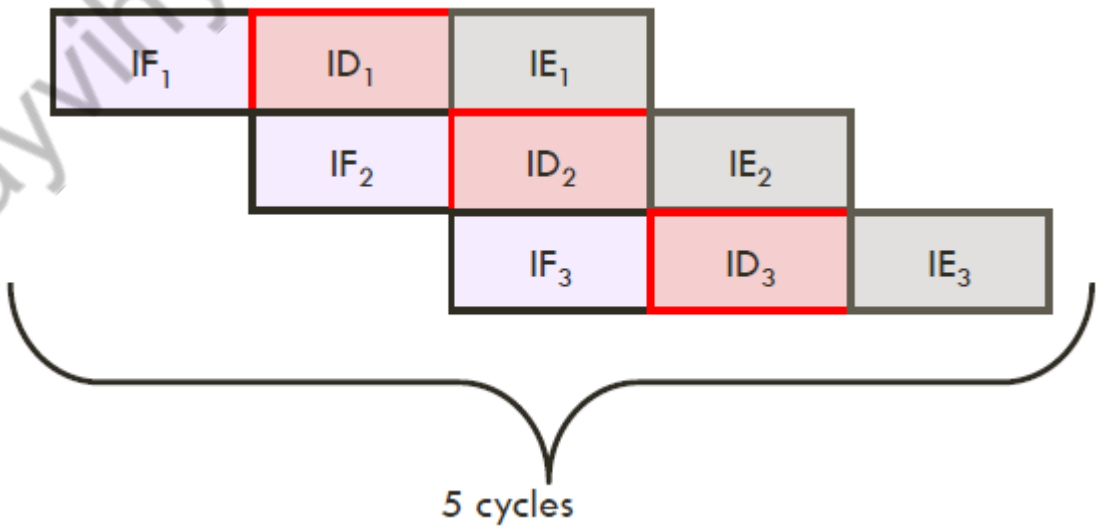
- Pipelining
- Replication



INSTRUCTION PIPELINES

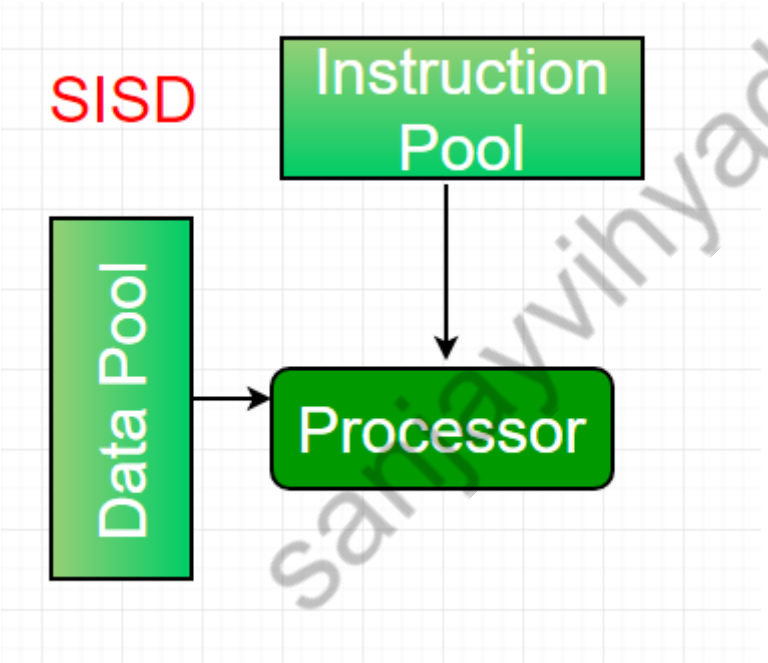
Instruction:

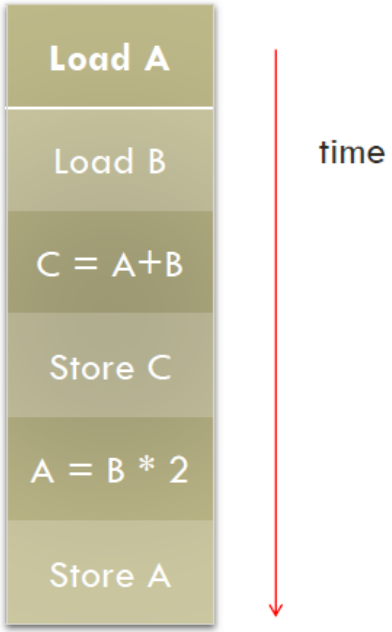
- Fetch
- Decode
- Execute



FLYNN'S TAXNOMY

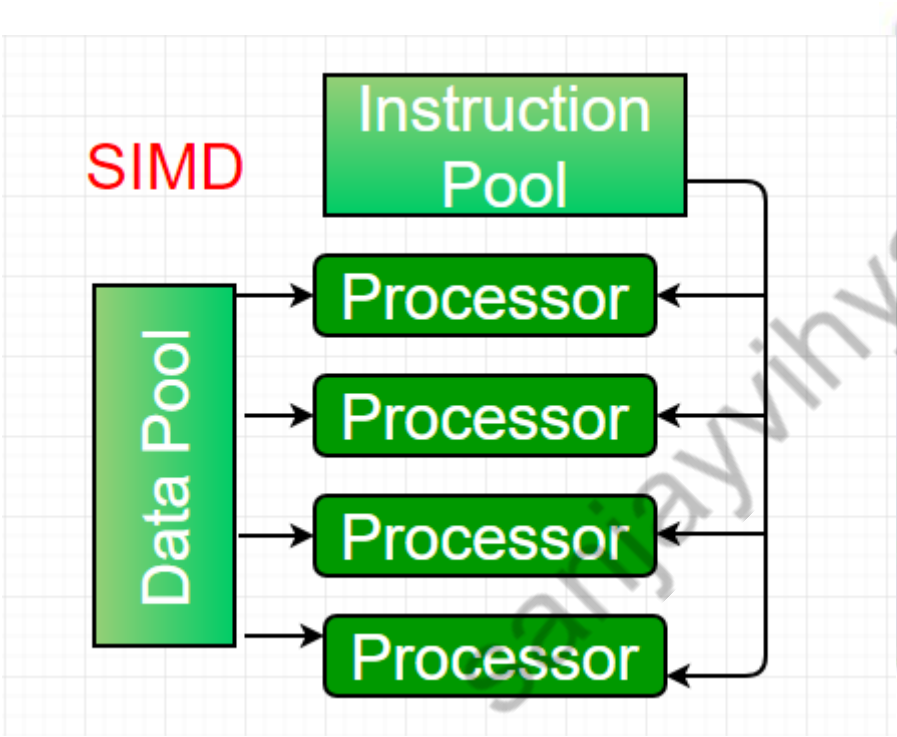
1. SISD: Single Instruction, Single-Data Systems

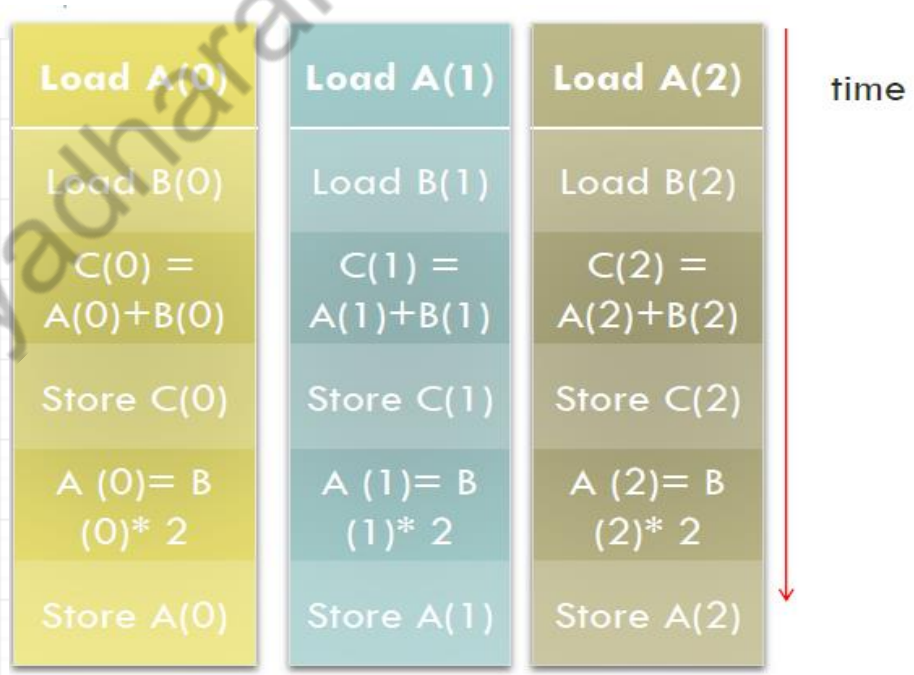




FLYNN'S TAXNOMY

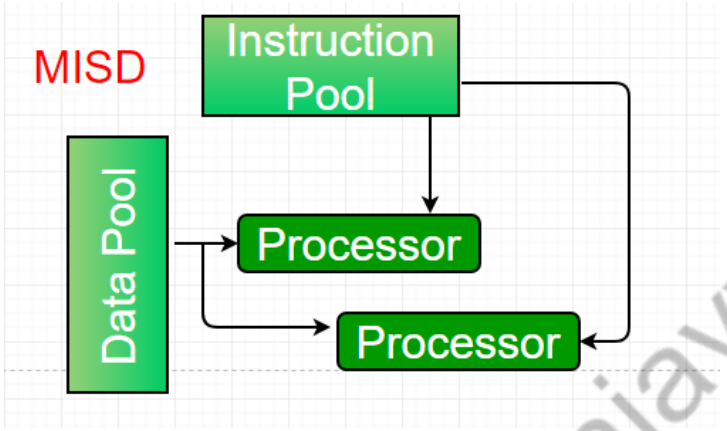
2. SIMD : Single-Instruction, Multiple-Data Systems

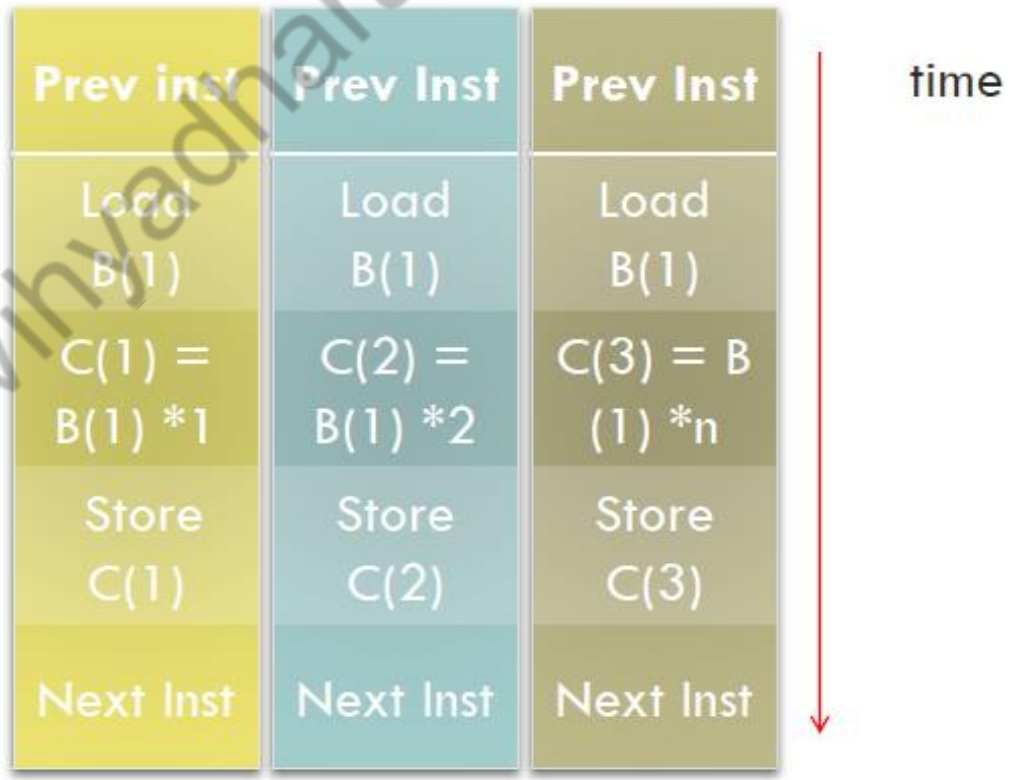




FLYNN'S TAXNOMY

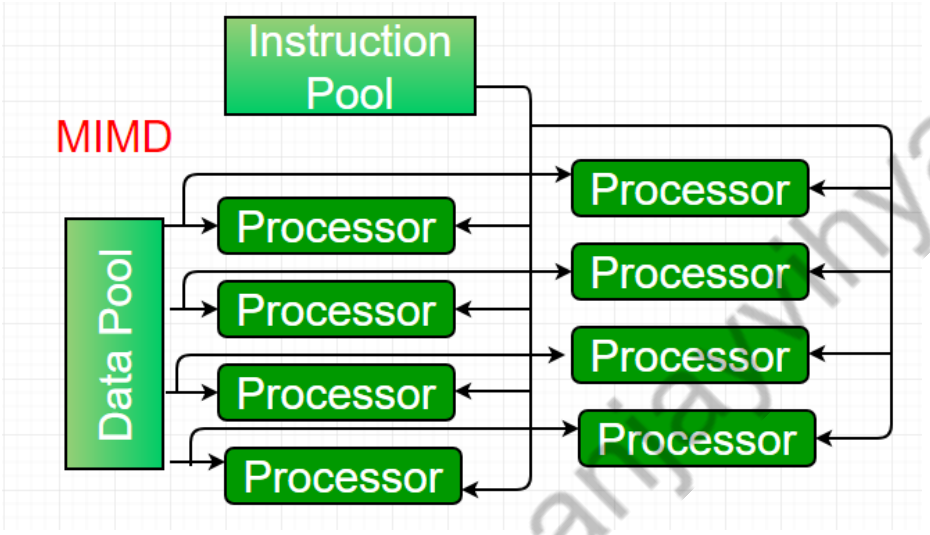
3. MISD : Multiple-Instruction, Single-Data Systems

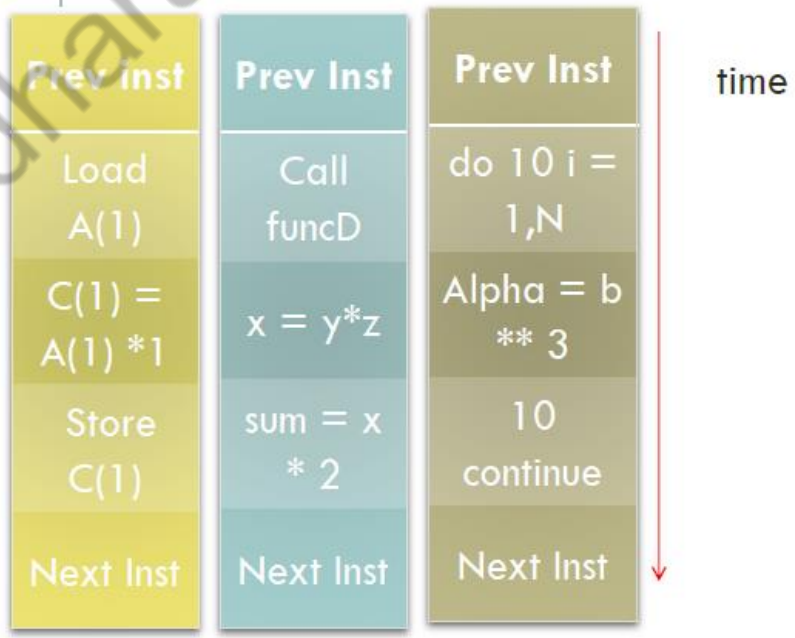




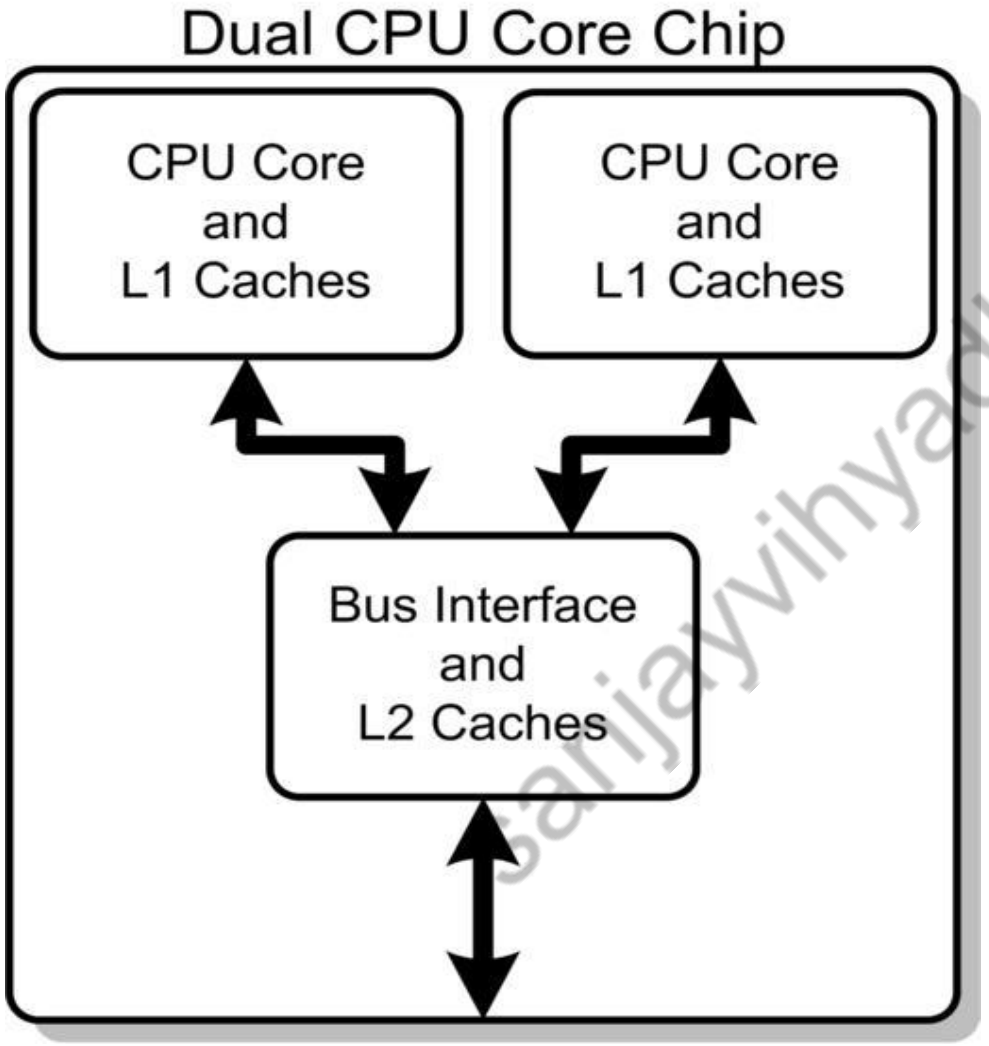
FLYNN'S TAXNOMY

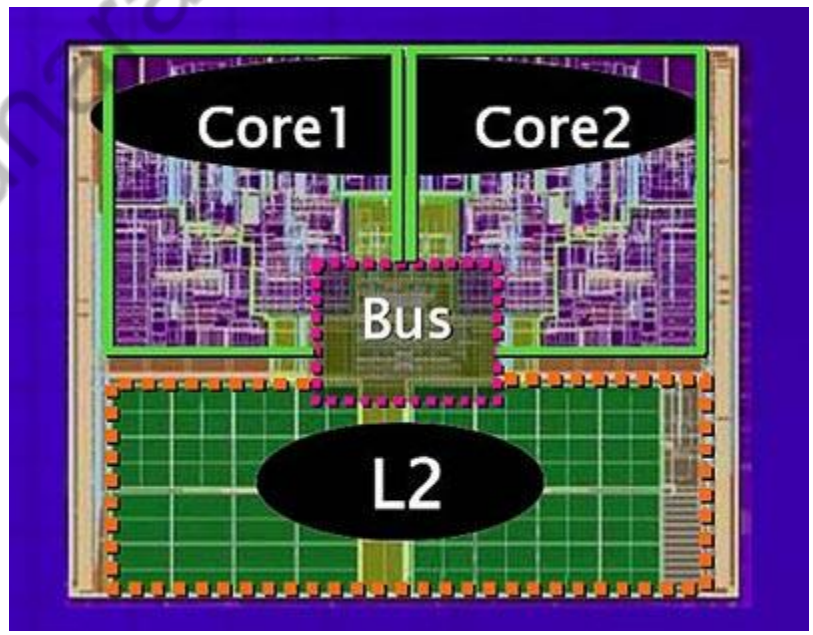
4. MIMD: Multiple-Instruction, Multiple-Data Systems



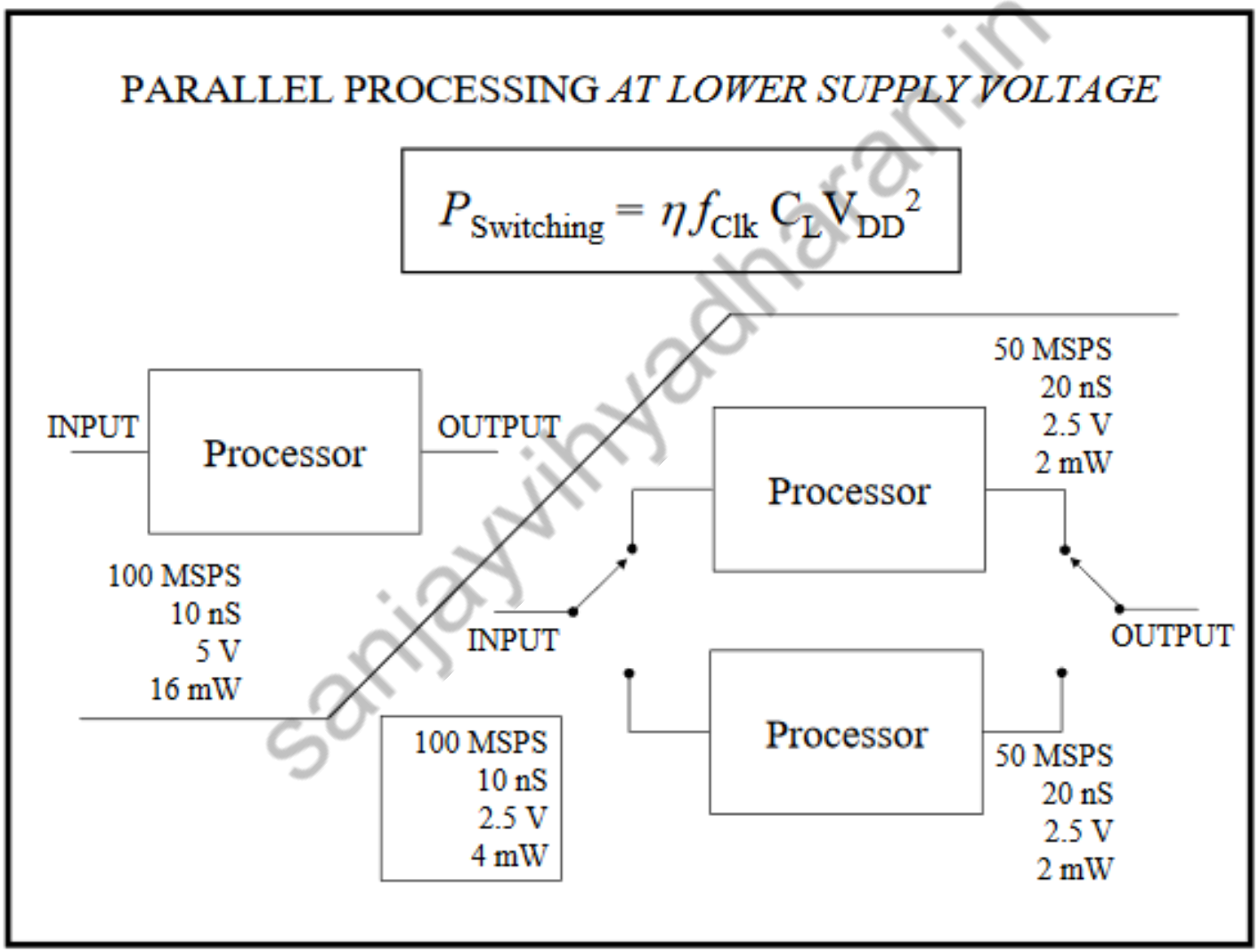


Multi-Core Processors

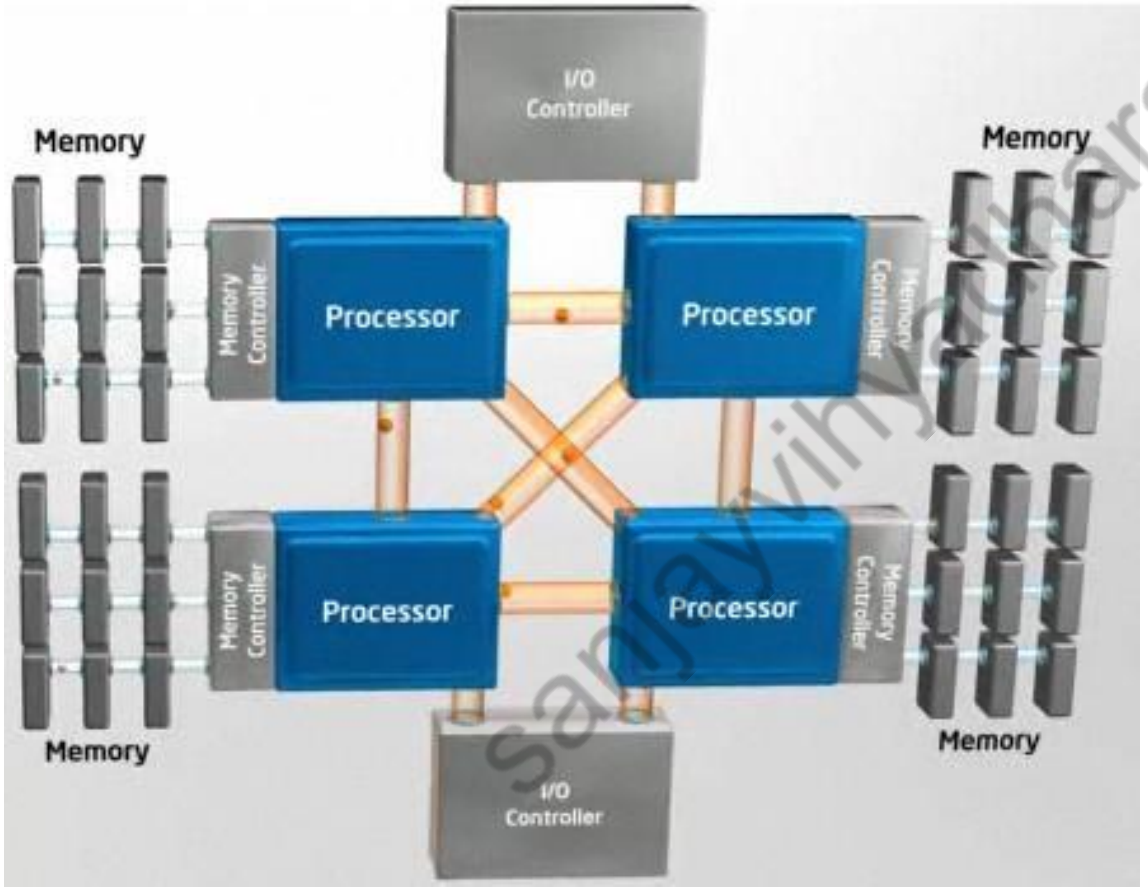




Multi-Core Processors



Multi-Core Processors



Quad- core microprocessor

EVOLUTION OF MICROPROCESSOR

Name	Date	Transistors	Clock speed	Data width
8080	1974	6K	2MHz	8
8086	1978	29K	5MHz	16
80286	1982	134K	12 MHz	16
80386	1985	275K	16-33 MHz	32
80486	1989	1.2 M	20 -100 MHz	32
Pentium	1993	3.1M	60-200 MHz	32 /64
Pentium II	1997	7.5 M	233-450 MHz	32/ 64
Pentium III	1999	9.5M	450 -933 MHz	32 /64
Pentium 4	2000	42 M	1.5 GHz	32/ 64

Thankyou