

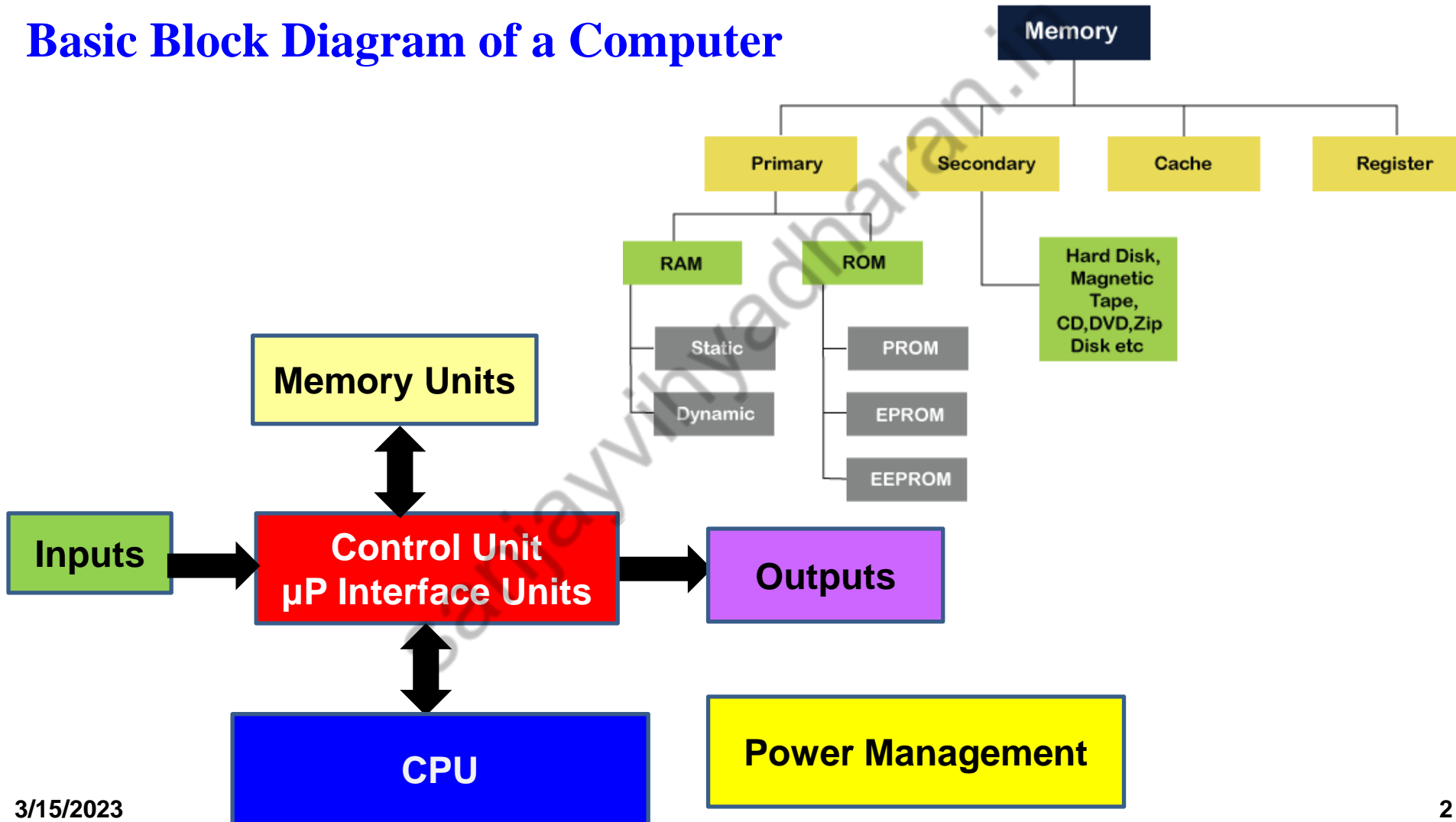
Microprocessor Programming and Interfacing

Lecture-2 : Introduction to Microprocessors

Dr. Sanjay Vidhyadharan

Introduction to Microprocessors

Basic Block Diagram of a Computer



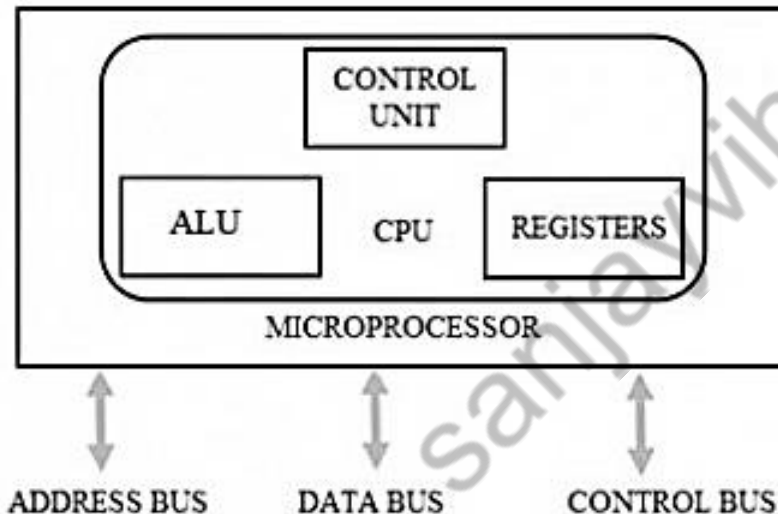
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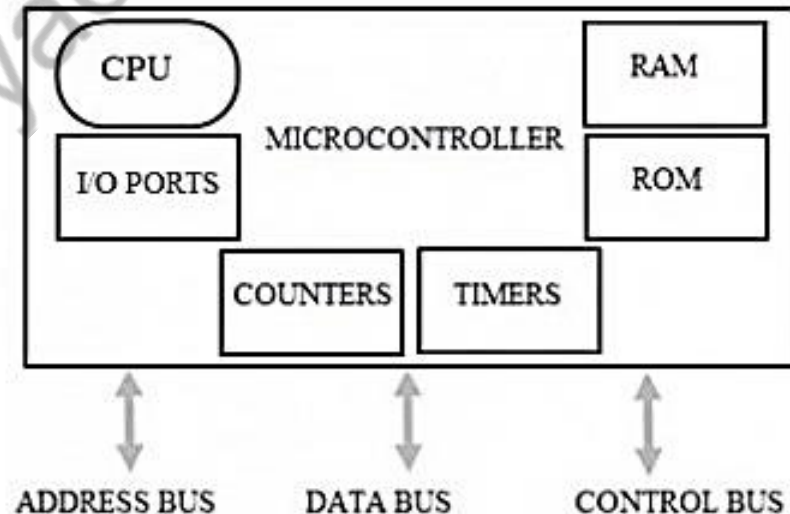
Introduction to Microprocessors

Microprocessor vs. Microcontroller

Microprocessor



Microcontroller



Introduction to Microprocessors

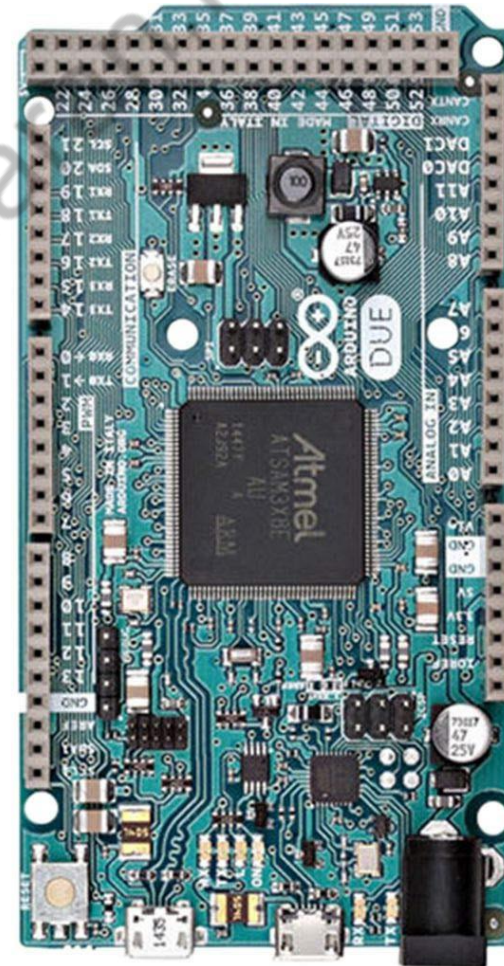


Introduction to Microprocessors

Microprocessor



Microcontroller



Instructions in Microprocessor

WHAT IS INSTRUCTIONS?

Tells the μ p what action to perform

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Instructions in Microprocessor

HOW DOES A MICROPROCESSOR HANDLE AN INSTRUCTION?

Fetch Cycle

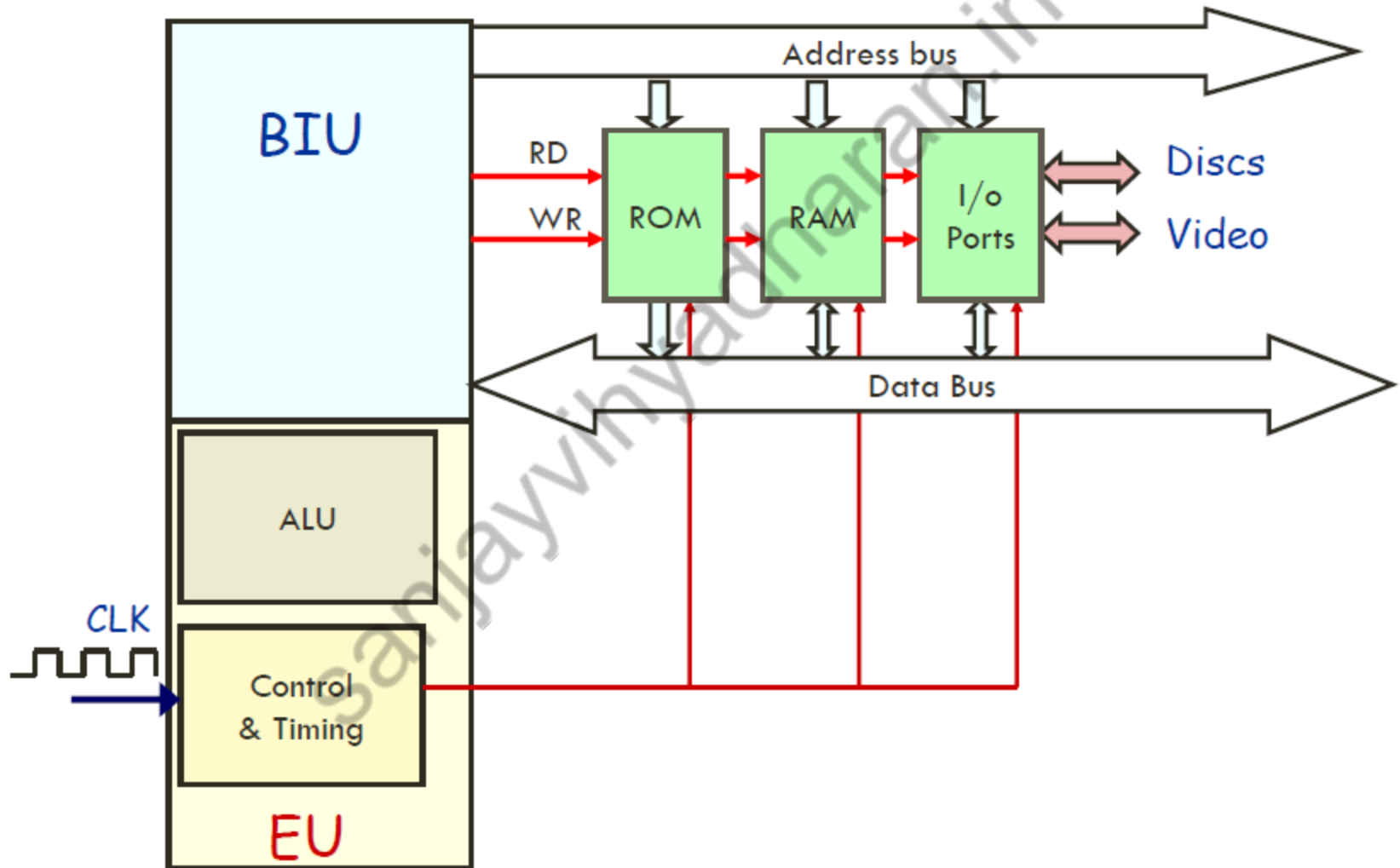
The fetch cycle takes the instruction required from memory, stores it in the instruction register

Execute Cycle

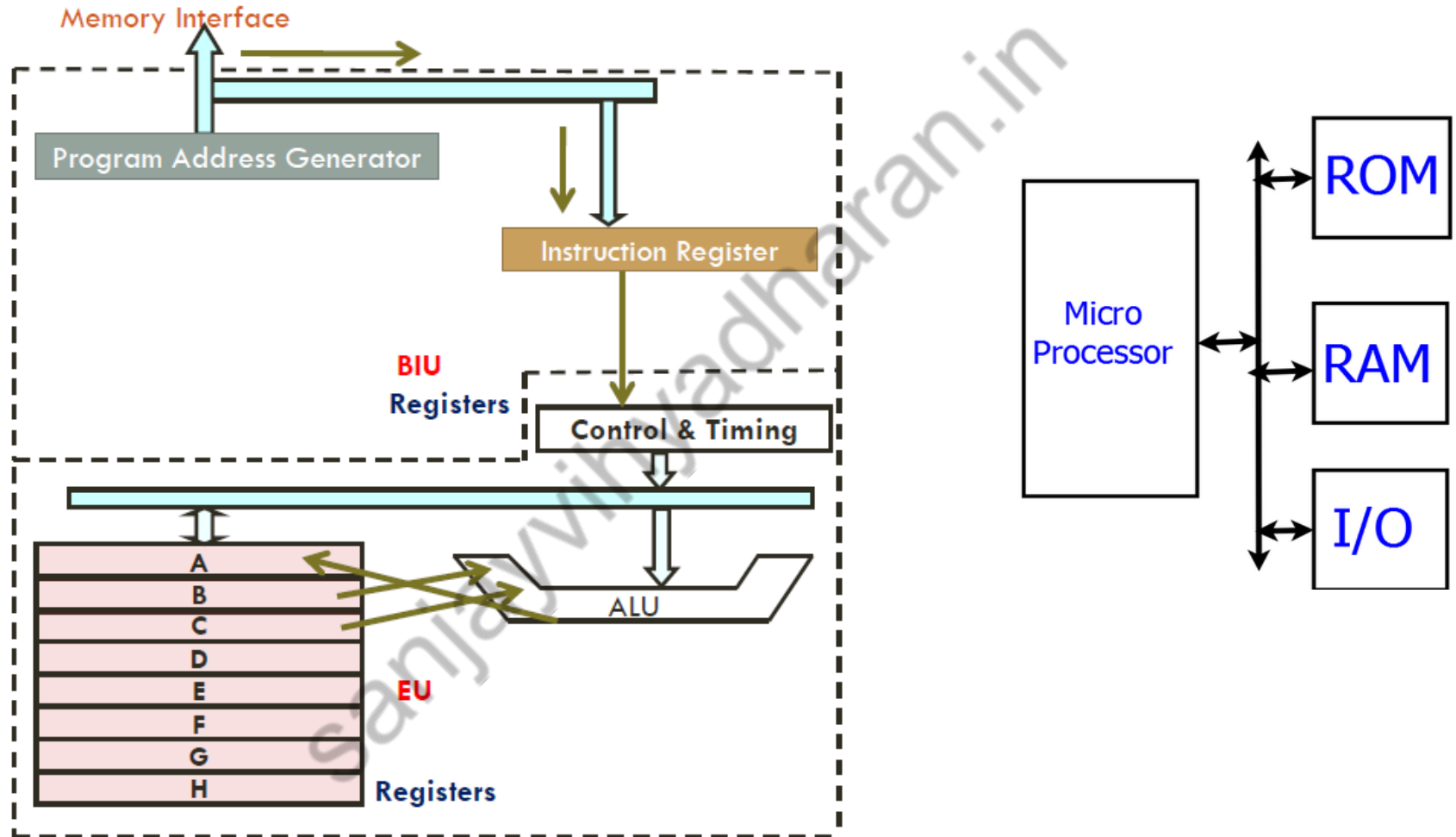
The actual actions which occur during the execute cycle of an instruction

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Introduction to Microprocessors



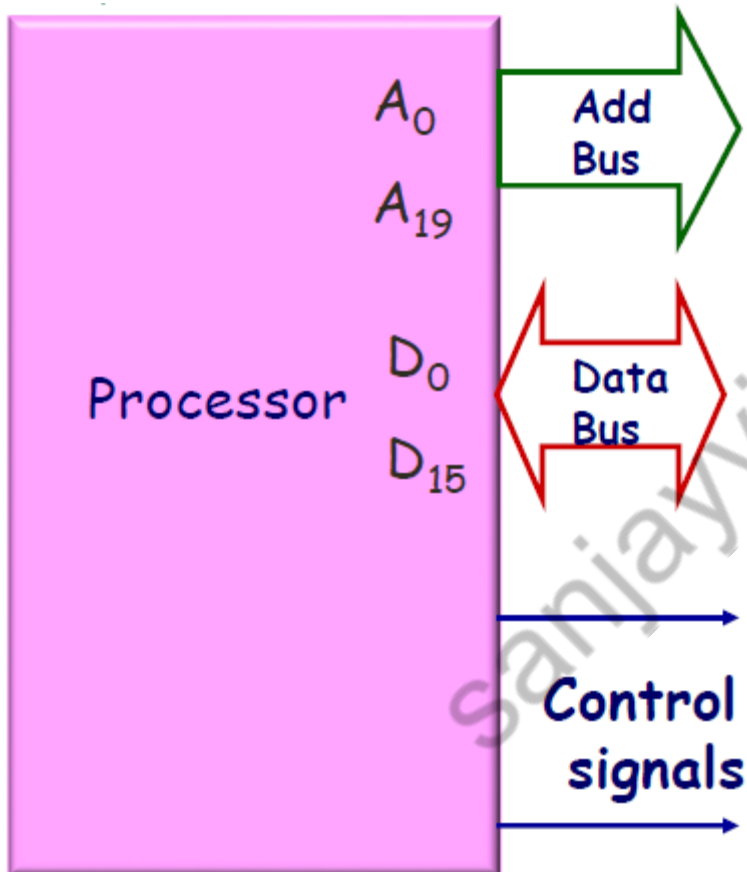
Introduction to Microprocessors



Block Diagram of a Microprocessor

Microprocessor Bus

PROCESSOR BUS



ADDRESS BUS:

No of Address lines

- 20 lines – A_{19} – A_0
- 1 M Byte of memory can be addressed

DATA BUS:

No of Data lines

- 16 lines – D_{15} – D_0

CONTROL LINES:

-Active low signals

- MEMR
- MEMW
- IOR
- IOW

Memory of Microprocessors

PROCESSOR MEMORY

- **ROM**
 - Non-Volatile
 - Read Only
- **RAM**
 - Volatile
 - Random Access Memory

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Processors

- **CISC (Complex Instruction Set Computer)**

Operands for Arithmetic/Logic operation can be in Register/ Memory

- **RISC (Reduced Instruction Set Computer)**

Operands for Arithmetic/Logic operation only in Registers

Register –Register Architecture

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RISC vs CISC

Goal: Multiply data in mem A with B
and put it back in A

CISC:

MUL A,B

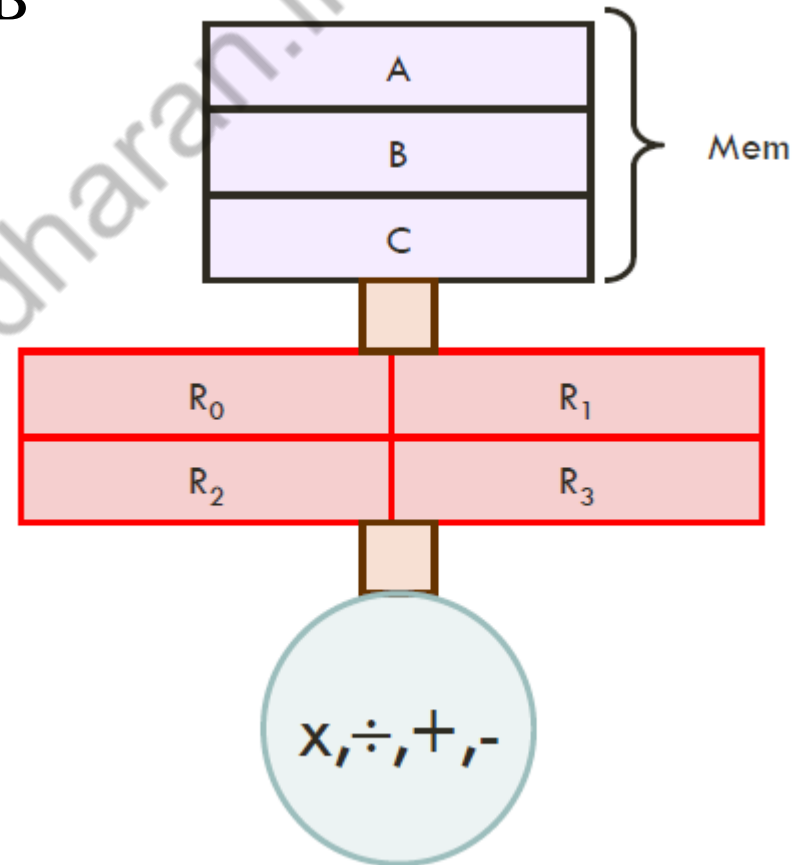
RISC:

LDA R₀,A

LDA R₁,B

MUL R₀,R₁

STR A,R₀



RISC vs CISC

Comparison of Instruction Sets



CISC



RISC



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RISC vs CISC

$$\frac{\text{Time Program}}{\text{Time cycle}} = \text{Cycles Inst} \times \frac{\text{Instructions Program}}{\text{Cycles Inst}}$$

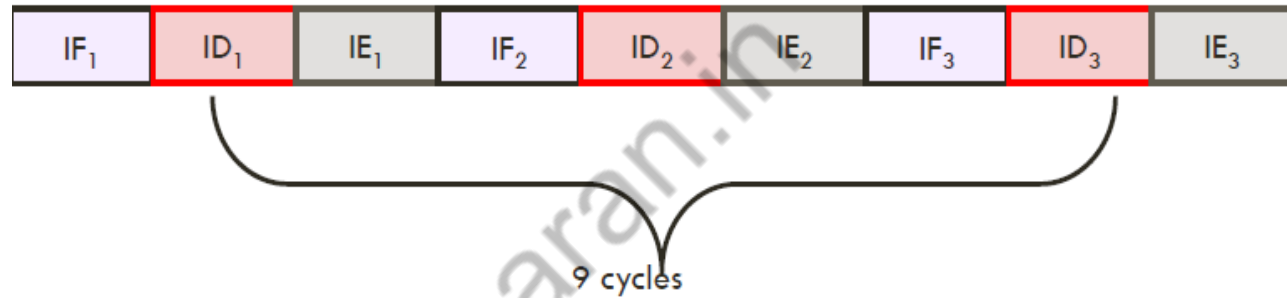
The diagram illustrates the relationship between RISC and CISC architectures in the context of the equation above. An upward arrow labeled "RISC" points from the "Cycles Inst" term to the "Cycles Inst" term in the denominator of the fraction on the right. Another upward arrow labeled "CISC" points from the "Cycles Inst" term to the "Instructions Program" term in the numerator of the fraction on the right.

CPU-SPEEDUP

1 Instruction Per Cycle (1 IPC)

Basic Parallel Techniques

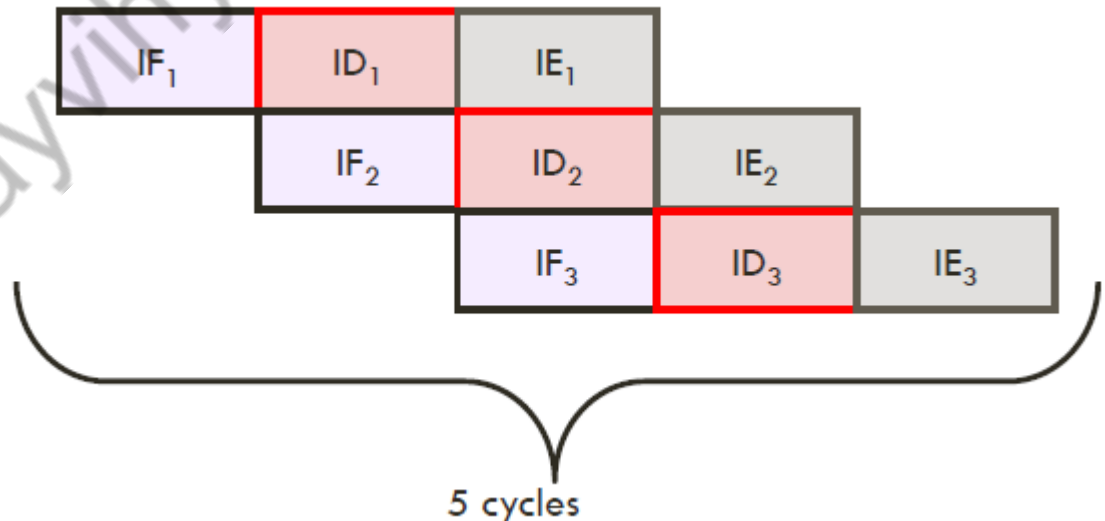
- Pipelining
- Replication



INSTRUCTION PIPELINES

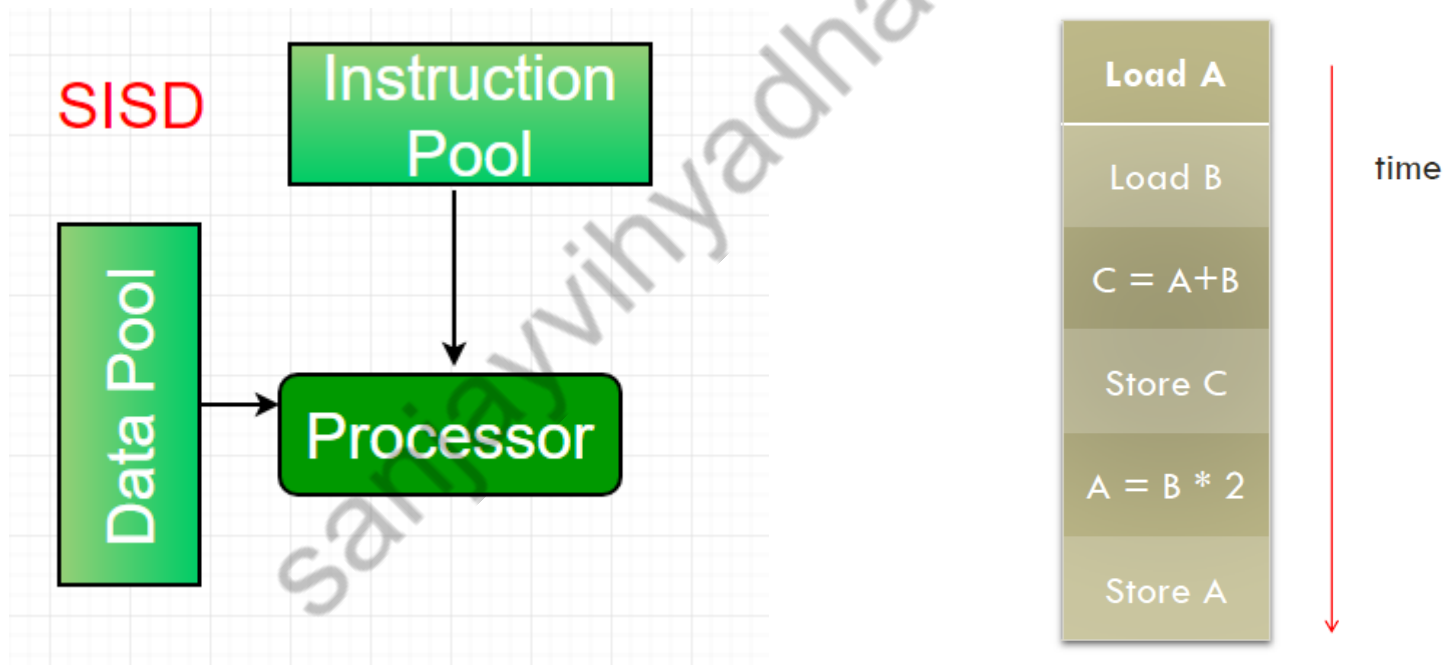
Instruction:

- Fetch
- Decode
- Execute



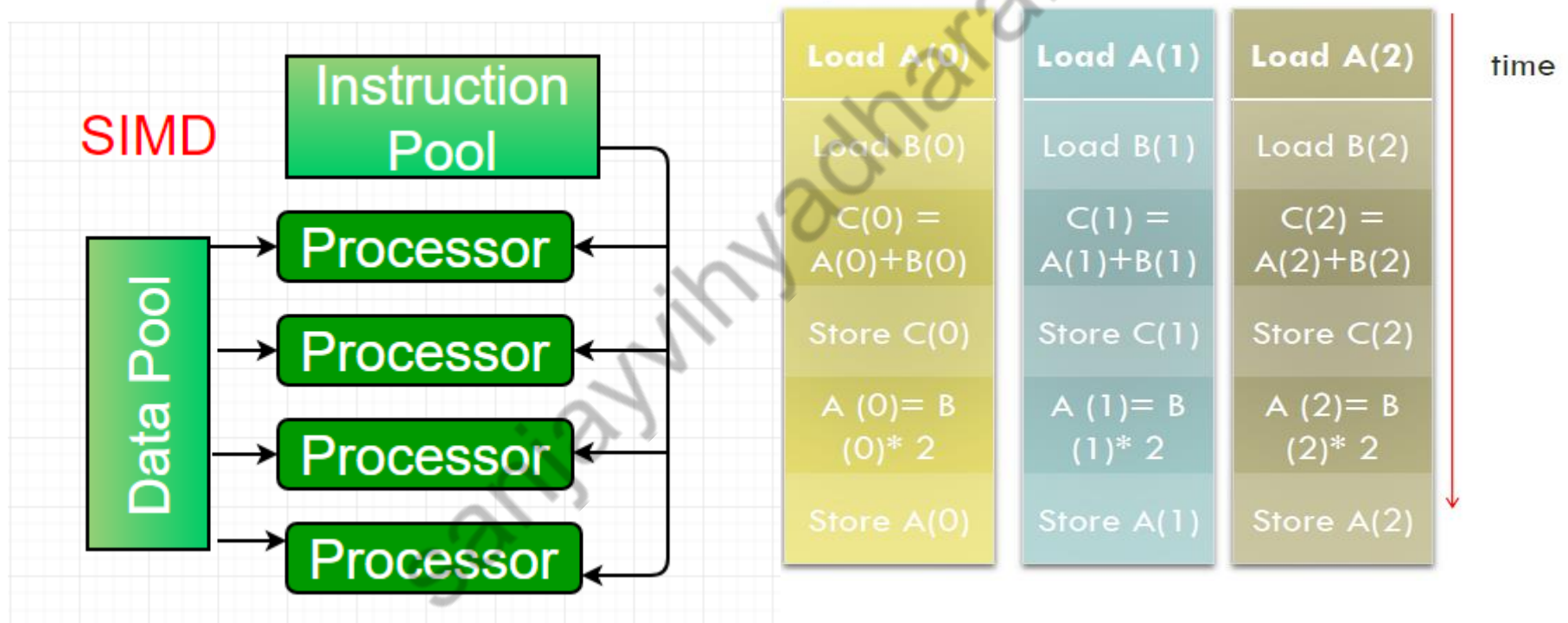
FLYNN'S TAXNOMY

1. SISD: Single Instruction, Single-Data Systems



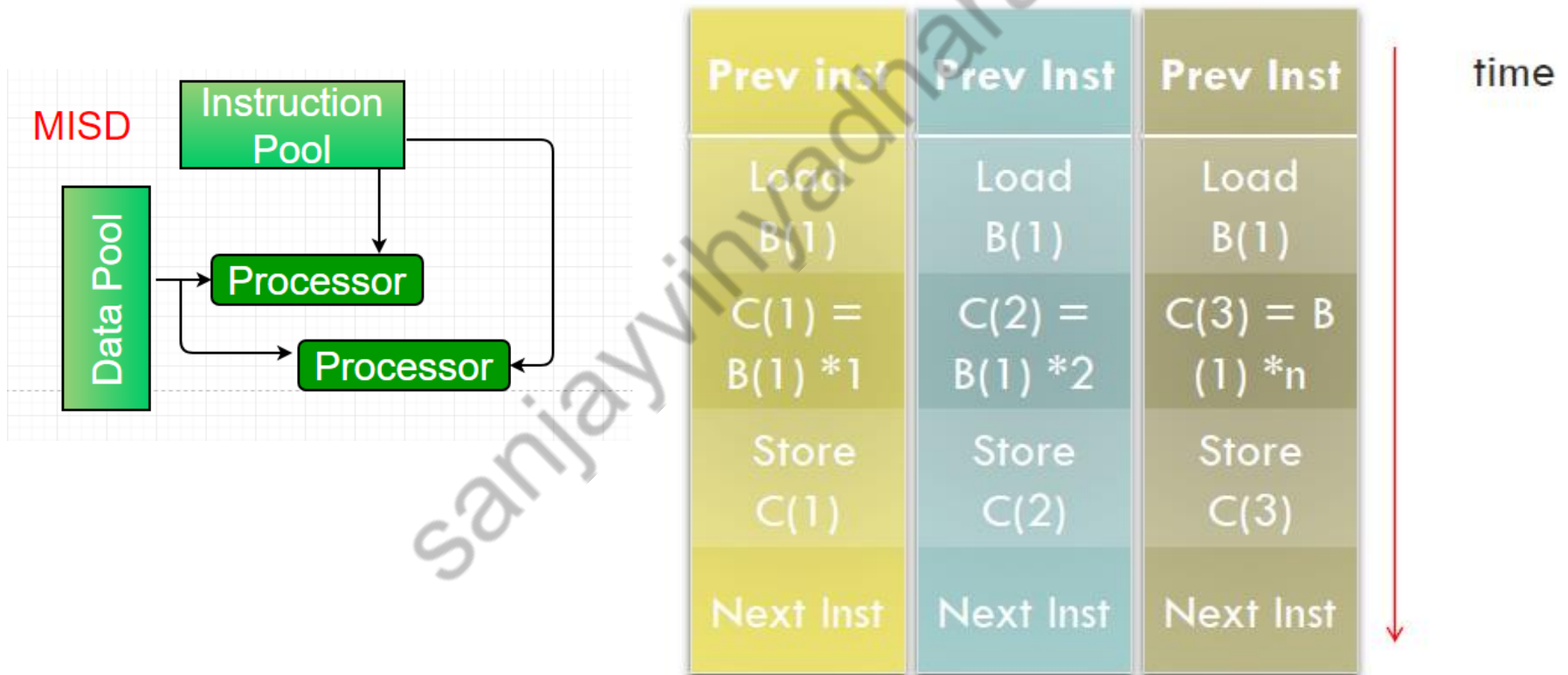
FLYNN'S TAXNOMY

2. SIMD : Single-Instruction, Multiple-Data Systems



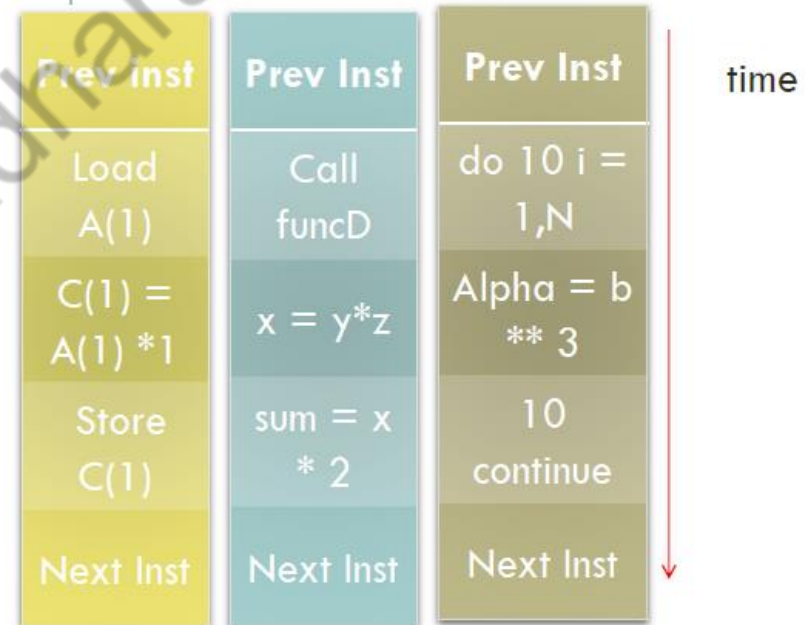
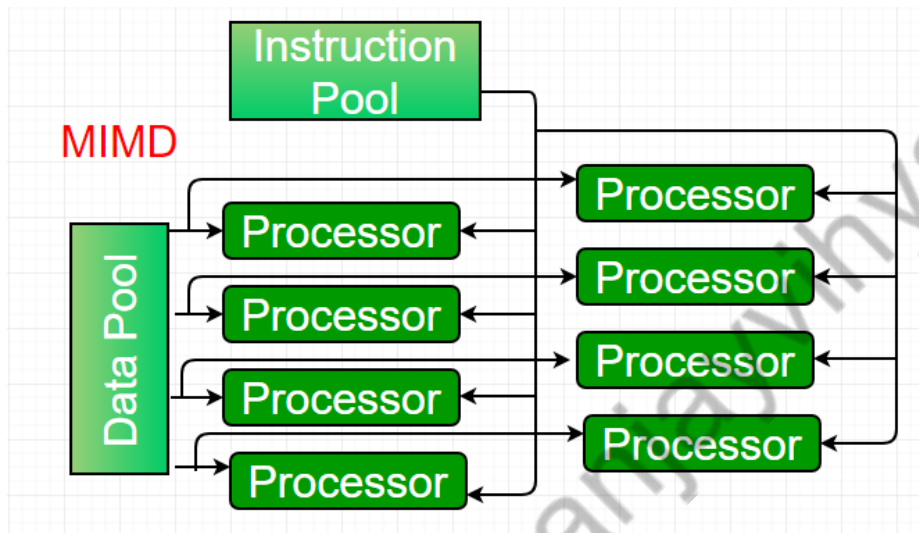
FLYNN'S TAXNOMY

3. MISD : Multiple-Instruction, Single-Data Systems



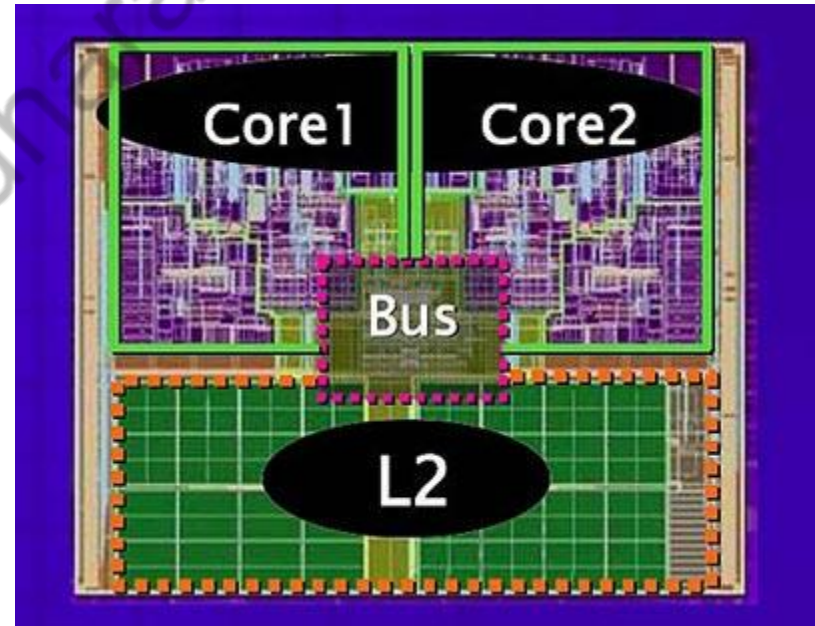
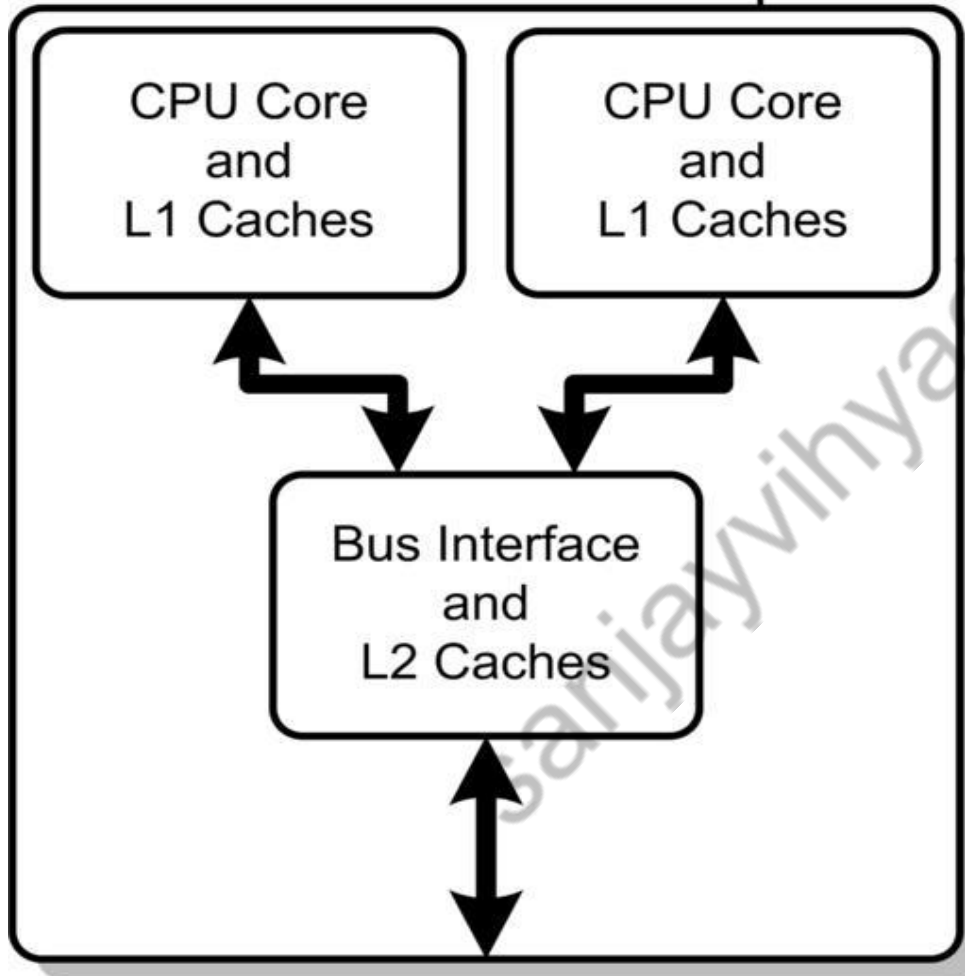
FLYNN'S TAXNOMY

4. MIMD: Multiple-Instruction, Multiple-Data Systems



Multi-Core Processors

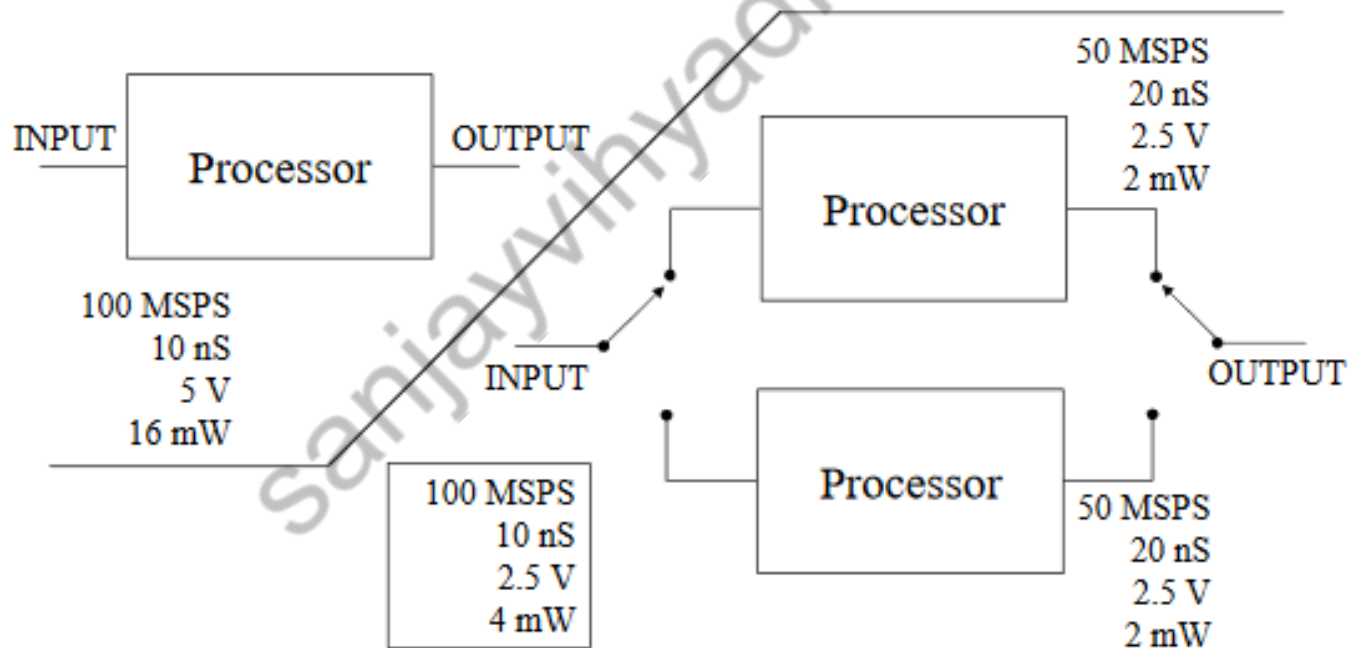
Dual CPU Core Chip



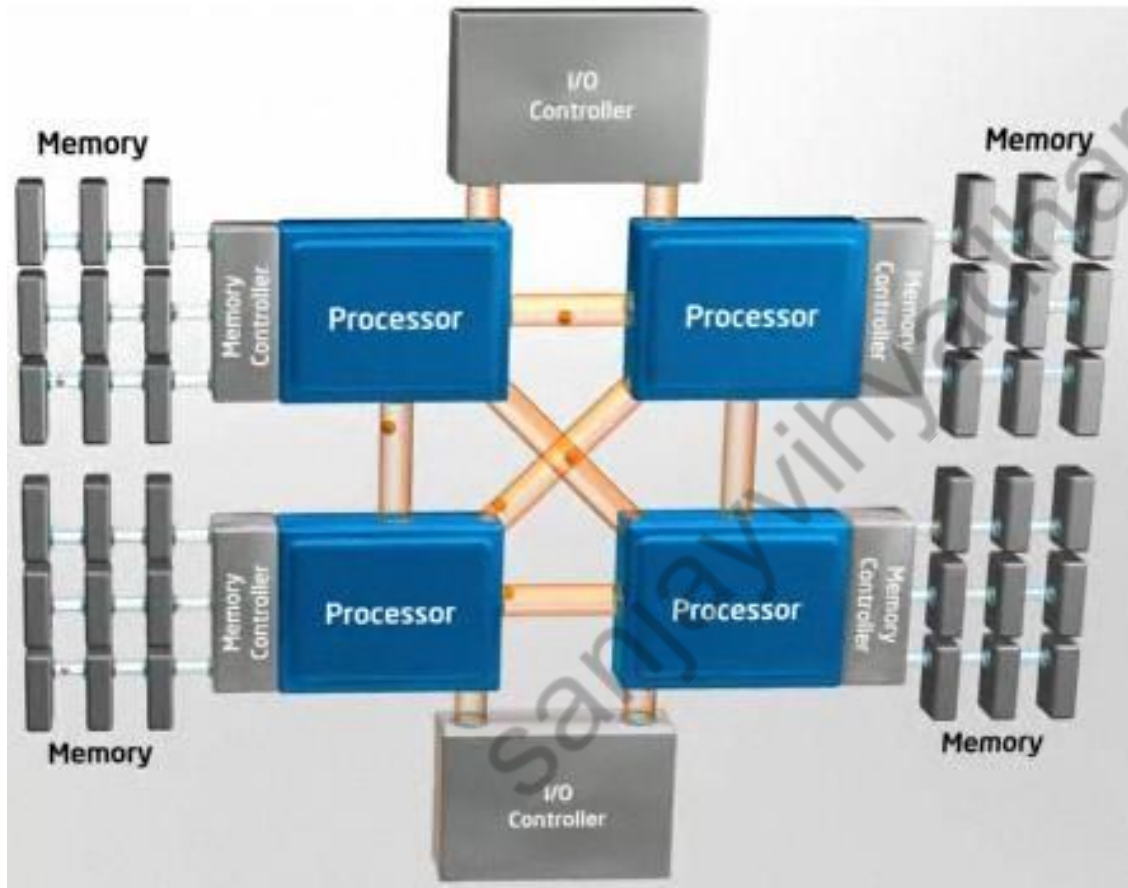
Multi-Core Processors

PARALLEL PROCESSING AT LOWER SUPPLY VOLTAGE

$$P_{\text{Switching}} = \eta f_{\text{Clk}} C_L V_{\text{DD}}^2$$



Multi-Core Processors



Quad- core
microprocessor

EVOLUTION OF MICROPROCESSOR

Name	Date	Transistors	Clock speed	Data width
8080	1974	6K	2MHz	8
8086	1978	29K	5MHz	16
80286	1982	134K	12 MHz	16
80386	1985	275K	16-33 MHz	32
80486	1989	1.2 M	20 -100 MHz	32
Pentium	1993	3.1M	60-200 MHz	32 /64
Pentium II	1997	7.5 M	233-450 MHz	32/ 64
Pentium III	1999	9.5M	450 -933 MHz	32 /64
Pentium 4	2000	42 M	1.5 GHz	32/ 64

Thankyou

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