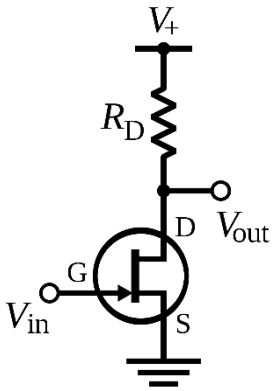
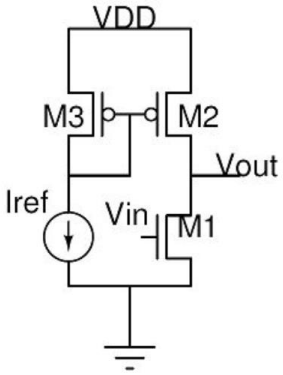
Analog IC Design : 2022-23
Lecture 13
Gain Boosting and Output Amplifiers

By Dr. Sanjay Vidhyadharan

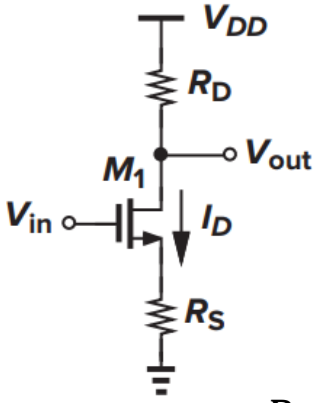
Gain Boosting



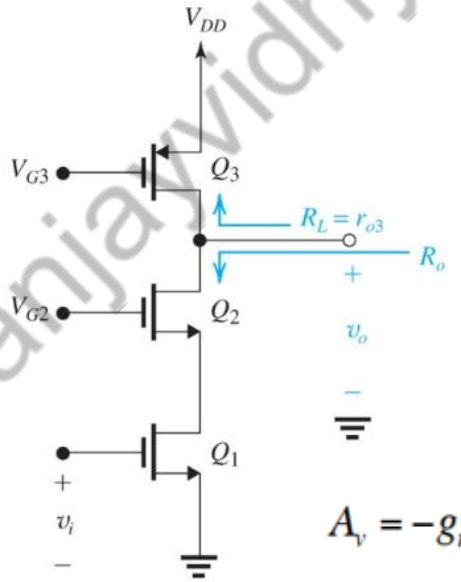
$$Gain = -g_m * (R_D || r_0)$$



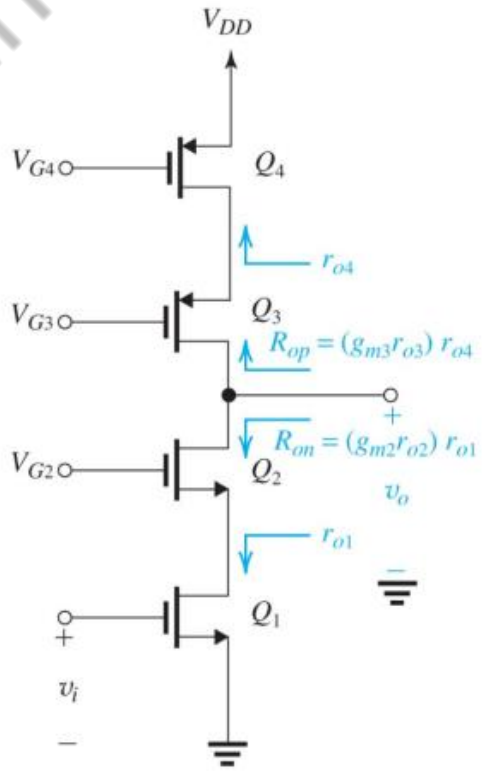
$$Gain = -g_m * (r_{01} || r_{02})$$



$$Gain \sim -\frac{R_D}{R_S}$$

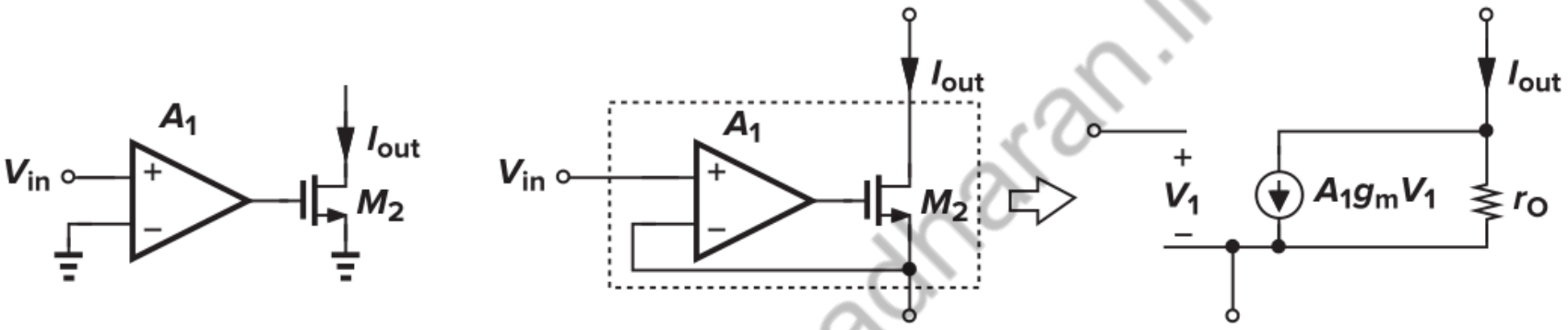


$$A_v = -g_{m1} r_{o3}$$



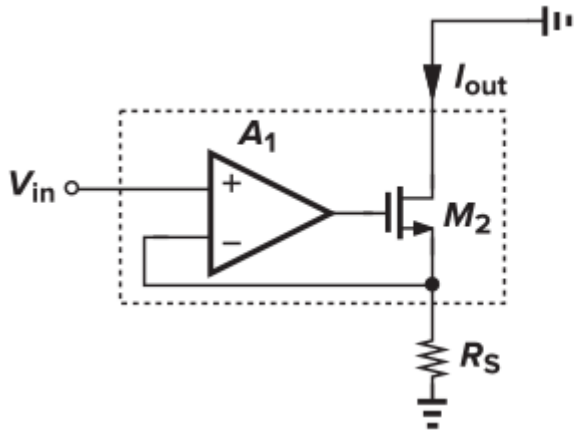
$$A_v = -\frac{1}{2}(g_m r_o)^2$$

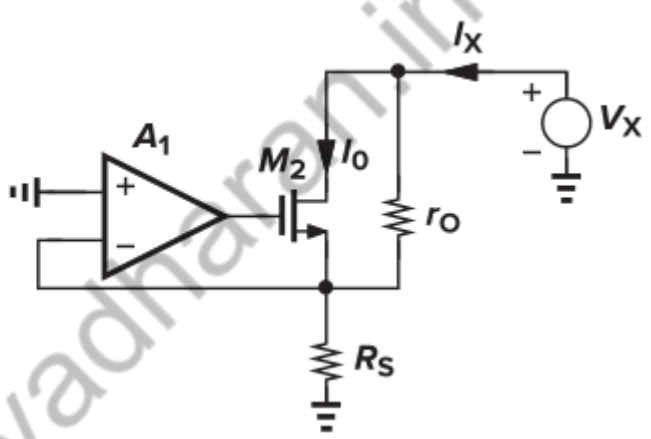
Gain Boosting



The idea behind gain boosting is to further increase the output impedance without adding more cascode devices.

Gain Boosting





$$V_d = V_{in} - I_{out}R_s$$

$$V_G = (V_{in} - I_{out}R_s)A_1$$

$$V_{GS} = (V_{in} - I_{out}R_s)A_1 - I_{out}R_s$$

$$I_{out} = g_m[(V_{in} - I_{out}R_s)A_1 - I_{out}R_s]$$

$$\frac{I_{out}}{V_{in}} = \frac{A_1 g_m}{1 + (A_1 + 1)g_m R_S}$$

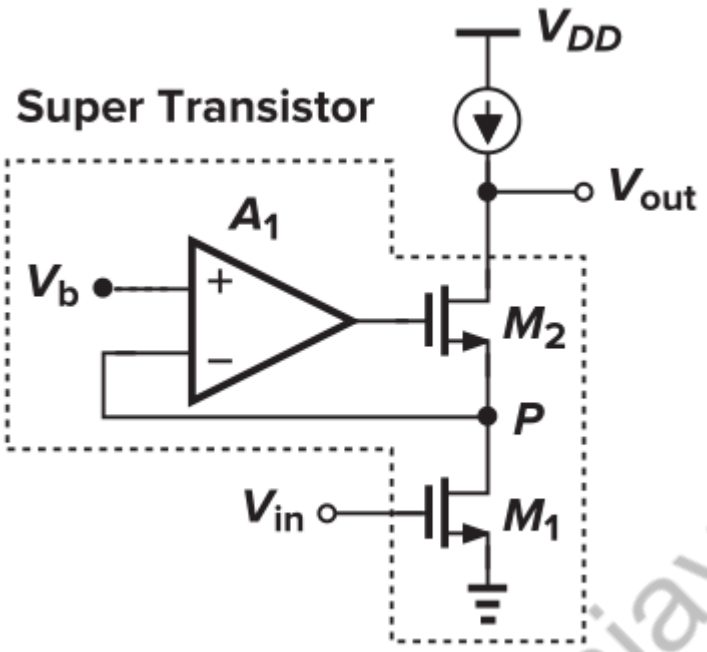
$$I_X = (-A_1 R_S - R_S)g_m I_X + \frac{V_X - R_S I_X}{r_O}$$

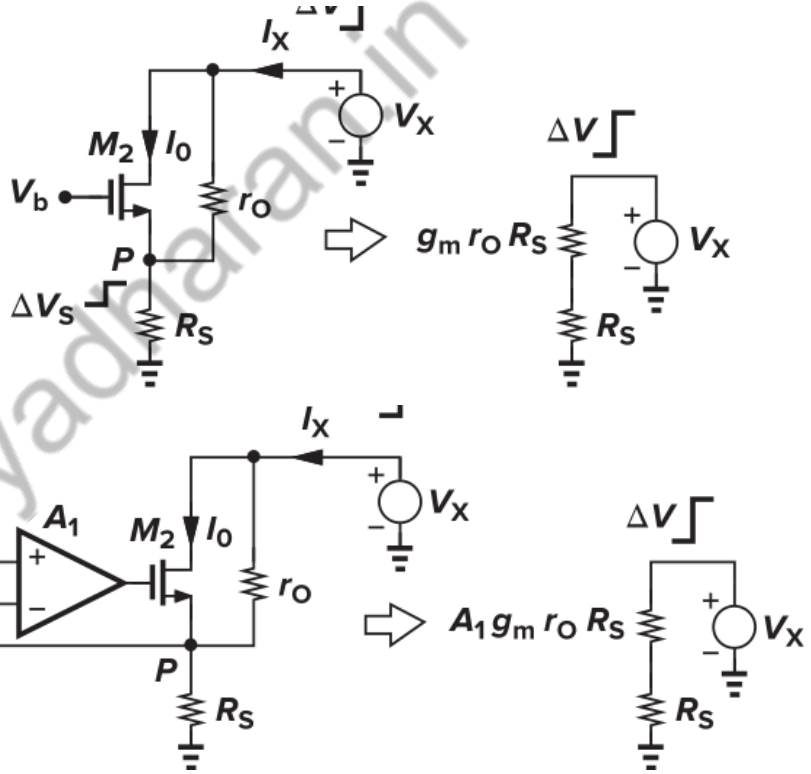
$$R_{out} = r_O + (A_1 + 1)g_m r_O R_S + R_S$$

$$Gain\ A_v \approx A_1\ g_m\ r_0$$

Gain Boosting

The Regulated Cascode





$V_p \approx V_{in} \ \ (g_{m1} \approx g_{m2})$

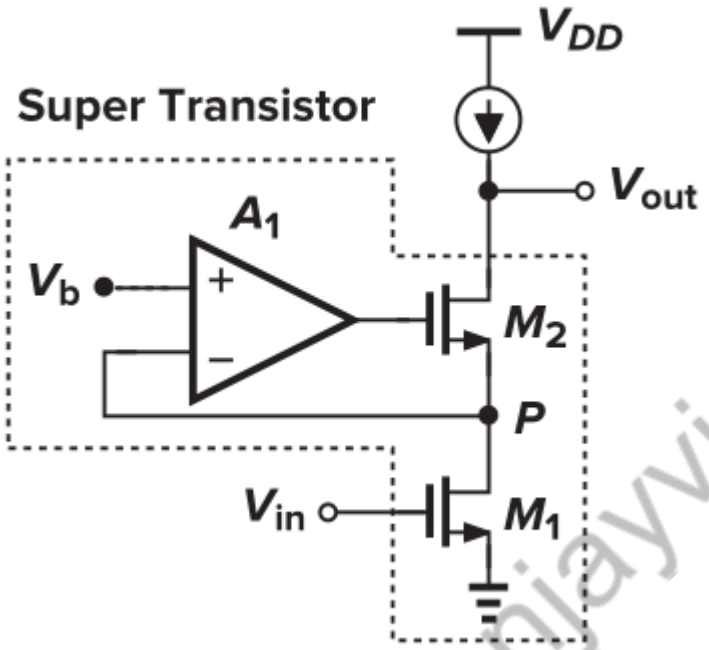
$G_m \approx \ (1 + A_1)\ g_{m1}$

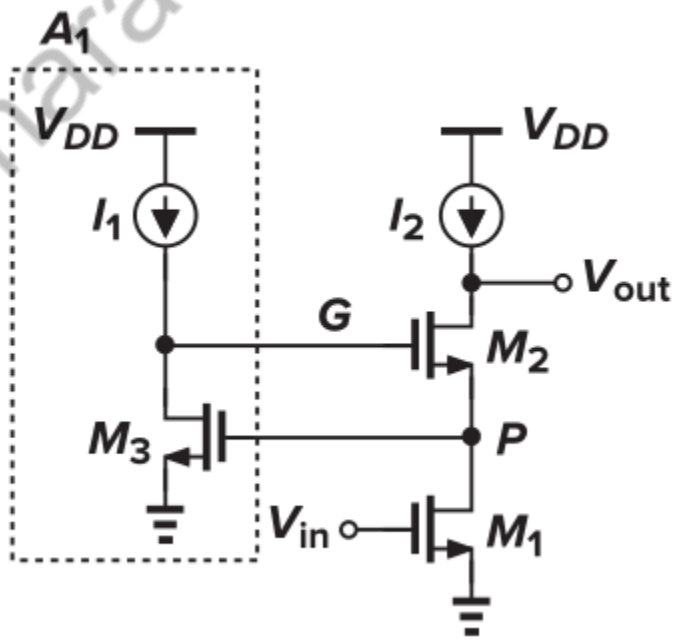
$$|A_v| \approx g_{m1}[r_{O2} + (A_1 + 1)g_{m2}r_{O2}r_{O1} + r_{O1}]$$

$$\approx g_{m1}g_{m2}r_{O1}r_{O2}(A_1 + 1)$$

Gain Boosting

Circuit Implementation

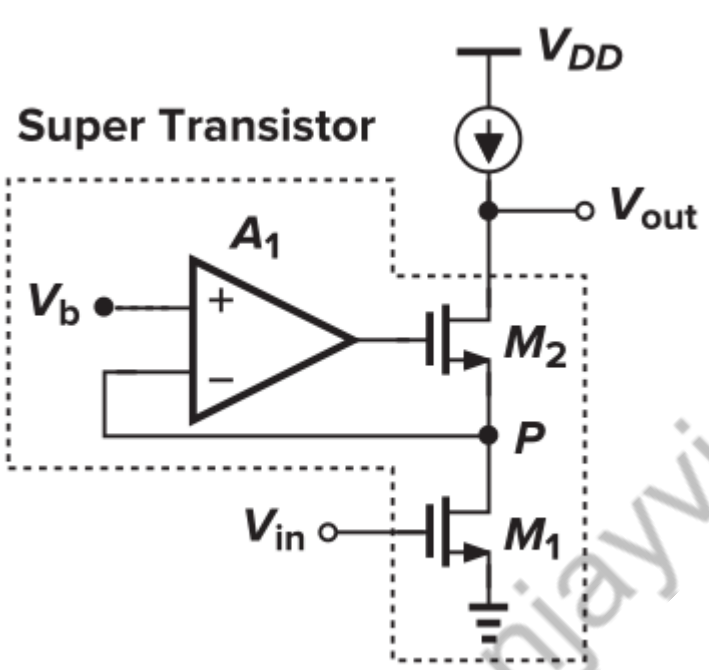


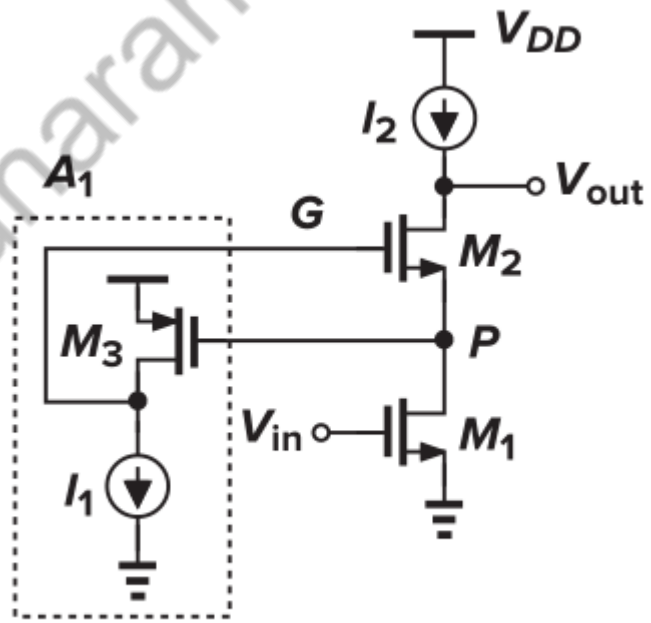


NMOS CS stage

Gain Boosting

Circuit Implementation

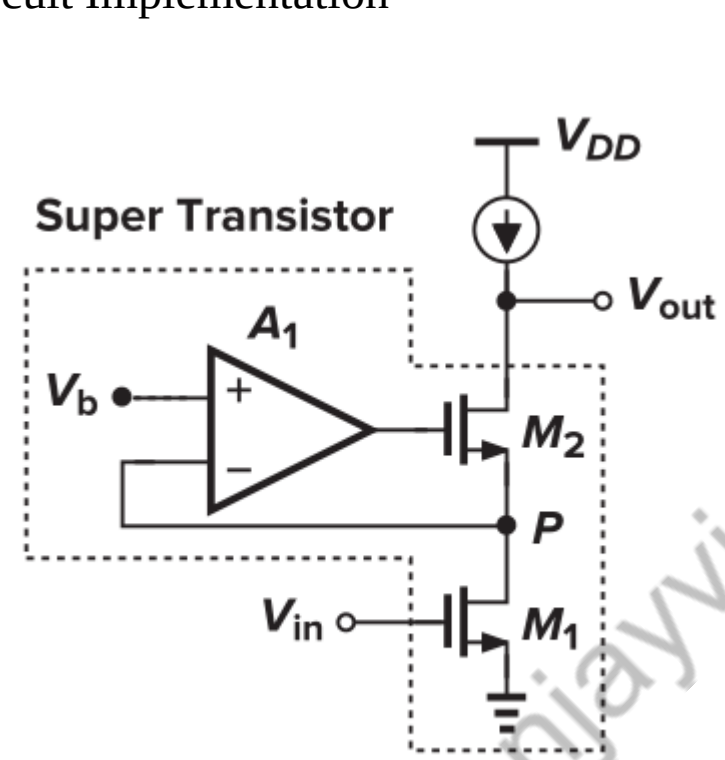


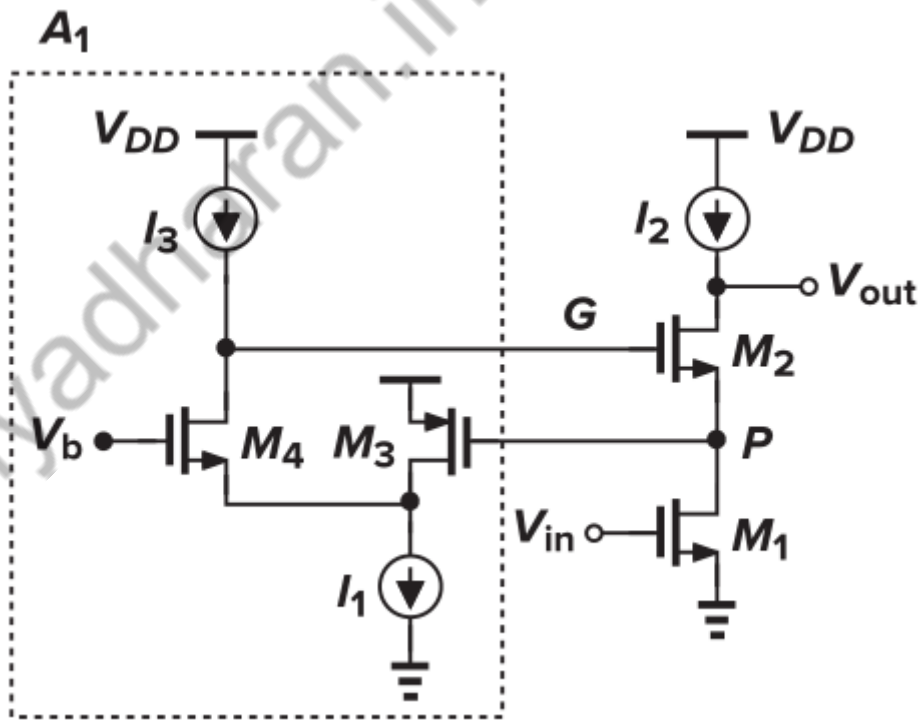


PMOS CS stage

Gain Boosting

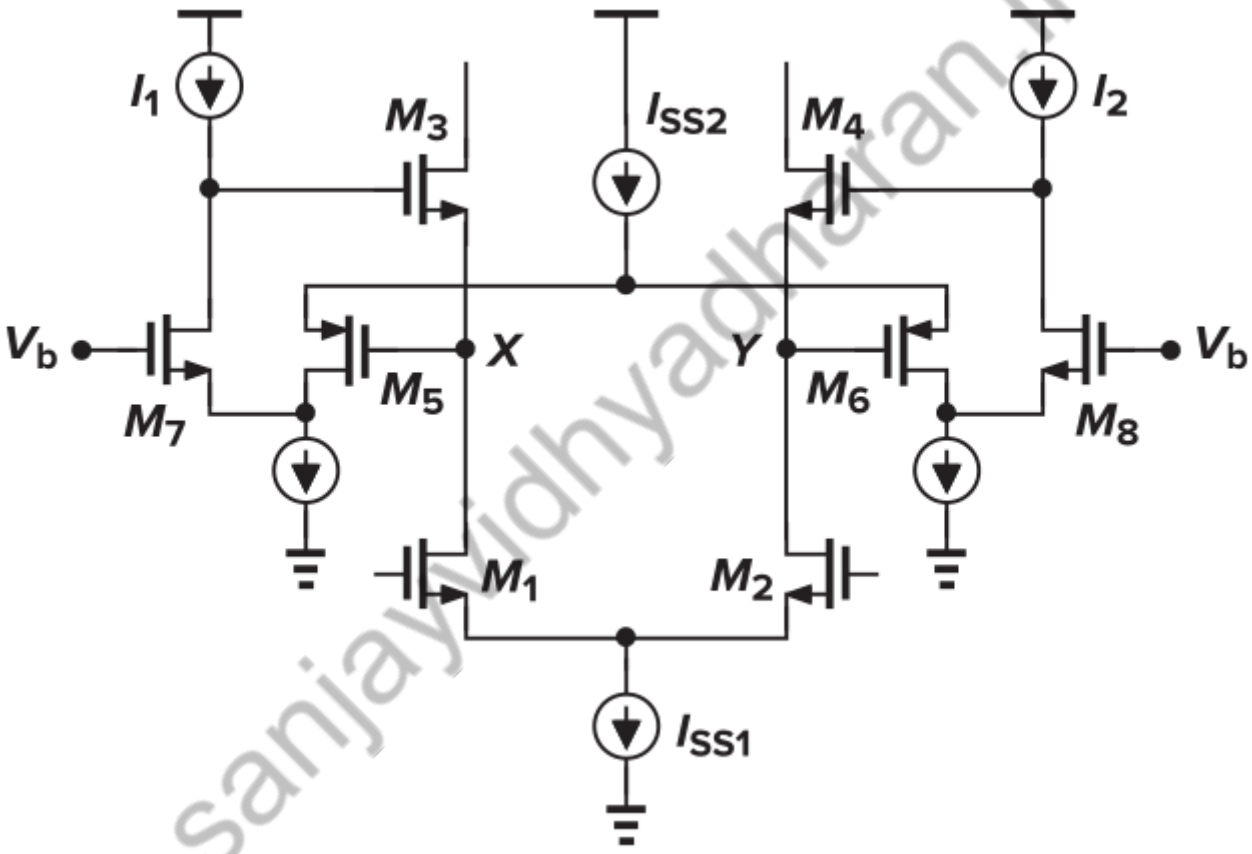
Circuit Implementation





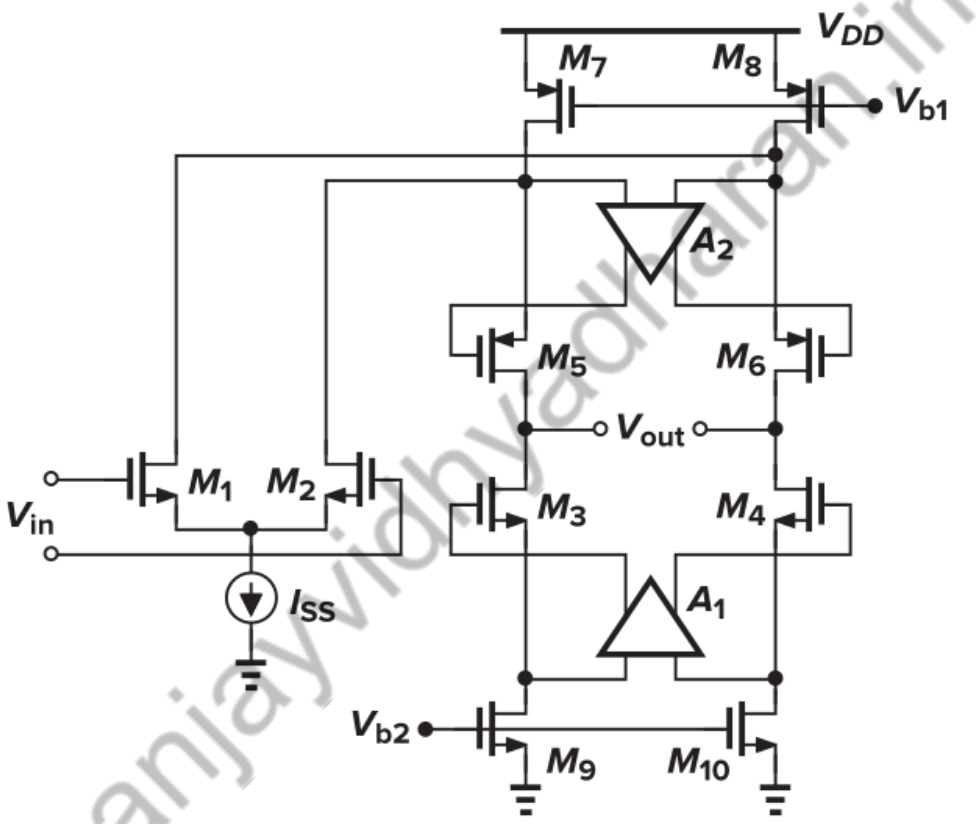
Folded-cascode stage

Gain Boosting



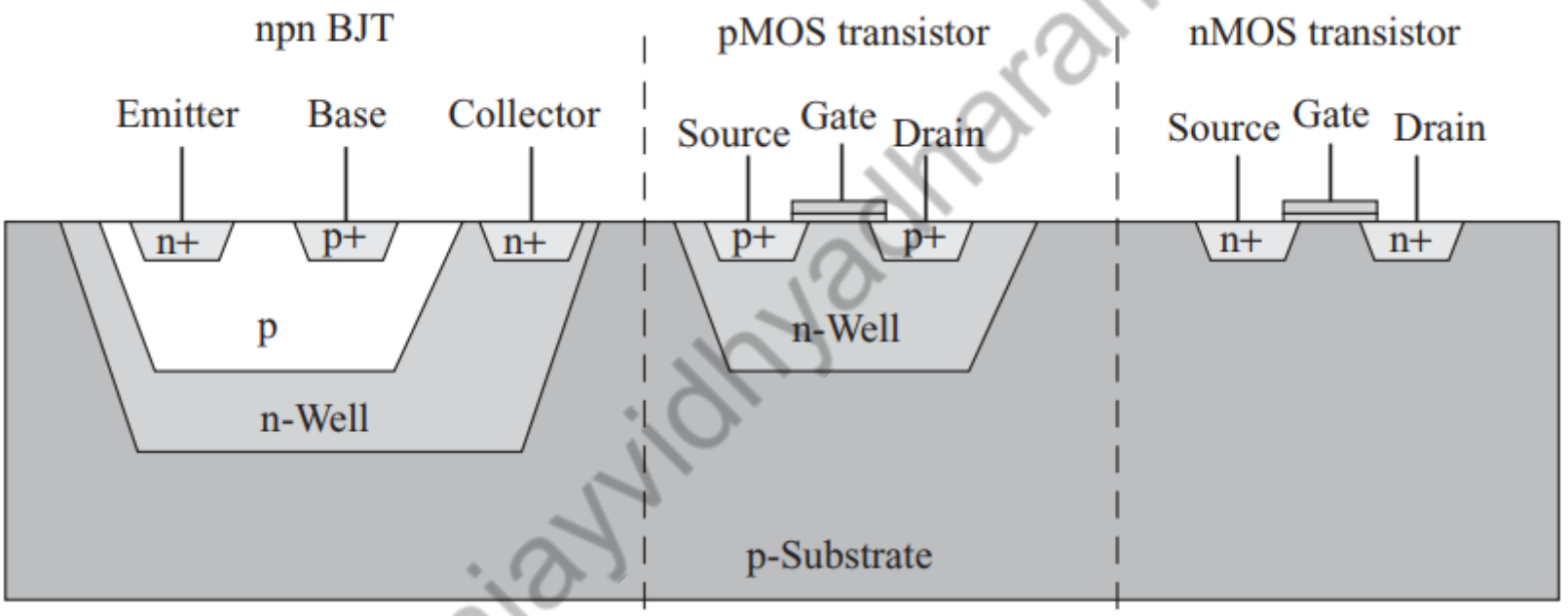
Folded-cascode Differential circuit

Gain Boosting



Gain boosting applied to both signal path and load devices.

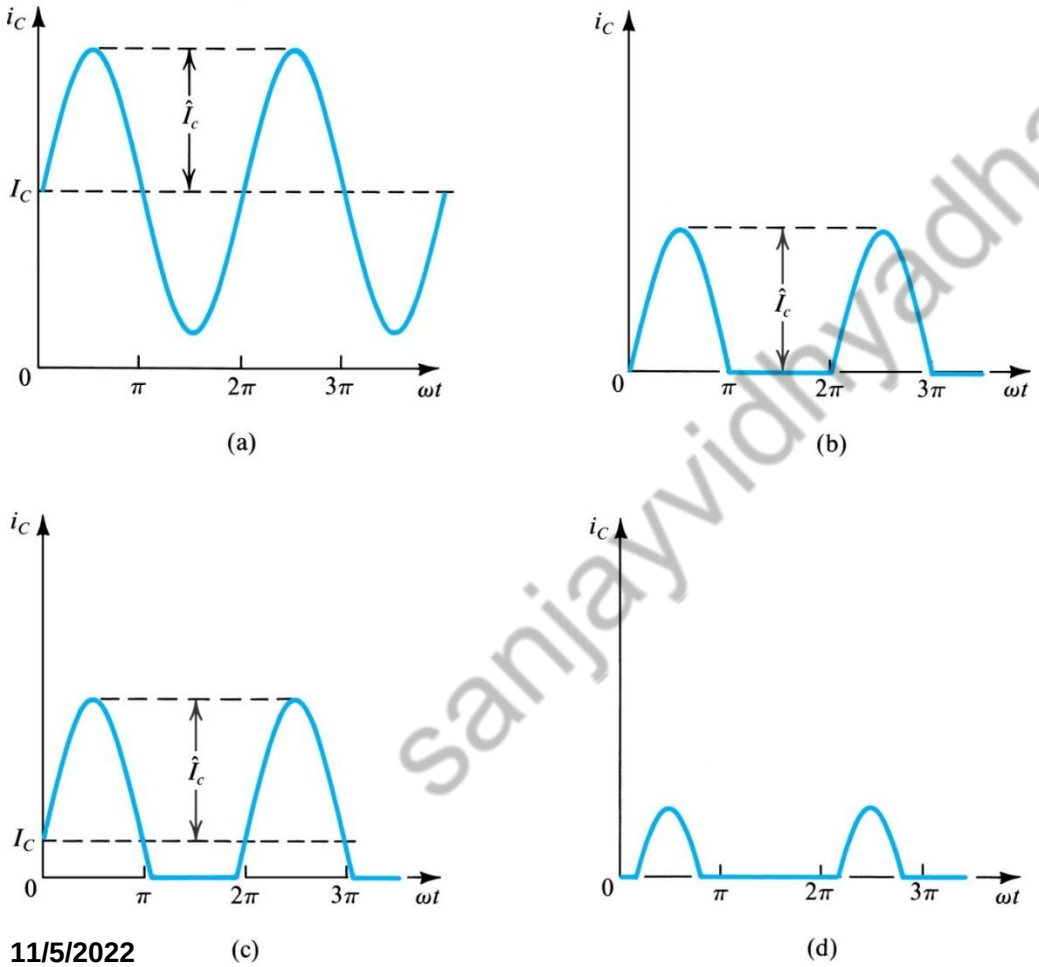
BiCMOS



Advantages of BJT
Higher switching speed
Higher current drive per unit area, higher gain

Output Amplifiers

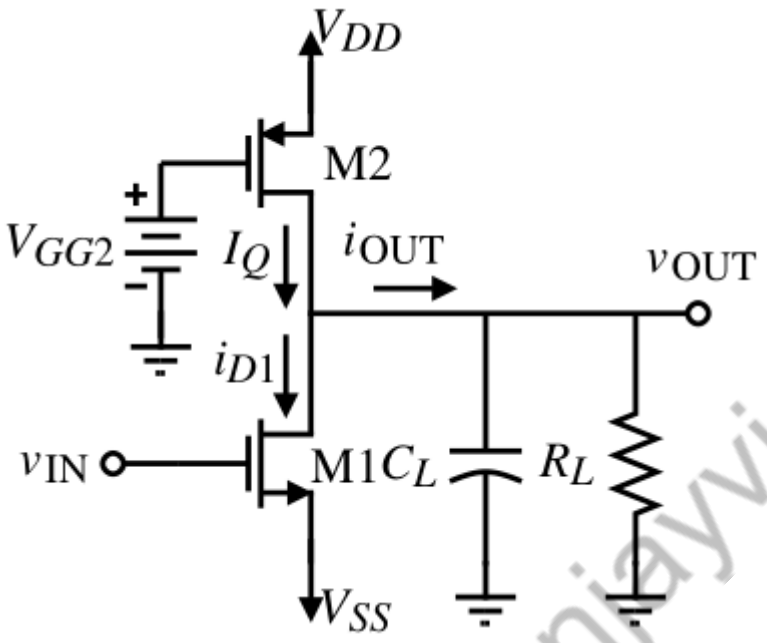
Classification of Output Stages



Collector current waveforms for transistors operating in
(a) class A,
(b) class B,
(c) class AB, and
(d) class C amplifier stages.

Output Amplifiers

CS Amplifier with High I_Q.



$$r_{out} = \frac{1}{g_{ds1} + g_{ds2}} = \frac{1}{(\lambda_1 + \lambda_2)I_D}$$

$$I_{OUT}^{-} = \frac{K_1' W_1}{2L_1}(V_{DD} - V_{SS} - V_{T1})^2 - I_Q$$

$$I_{OUT}^{+} = \frac{K_2' W_2}{2L_2}(V_{DD} - V_{GG2} - |V_{T2}|)^2 \leq I_Q$$

Output Amplifiers

CLASS A AMPLIFIERS

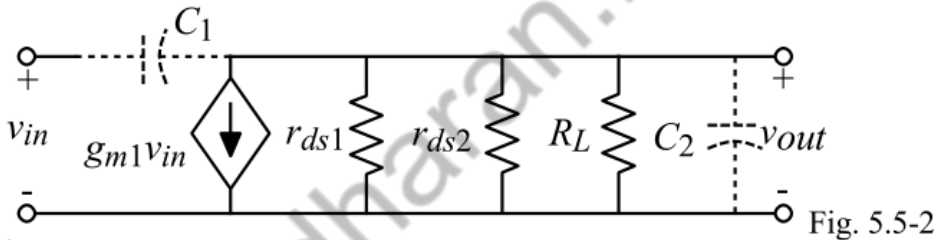


Fig. 5.5-2

The small-signal voltage gain is:

$$\frac{v_{out}}{v_{in}} = \frac{-g_{m1}}{g_{ds1}+g_{ds2}+G_L}$$

The small-signal frequency response includes:

A zero at

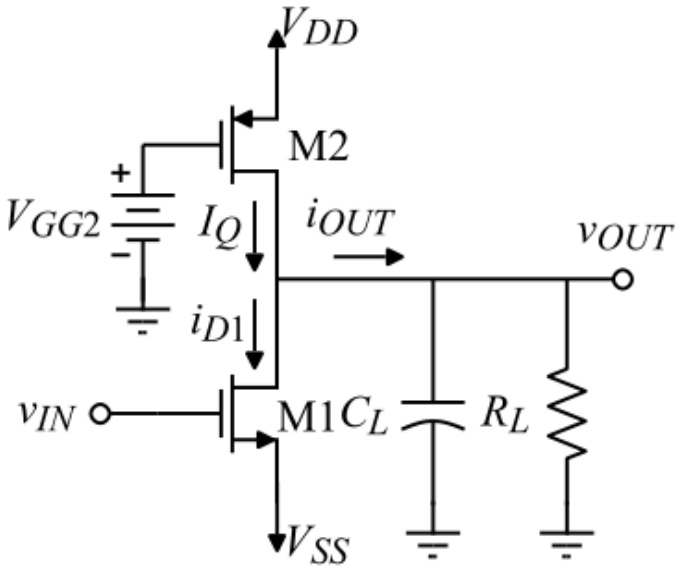
$$z = \frac{g_{m1}}{C_{gd1}}$$

and a pole at

$$p = \frac{-(g_{ds1}+g_{ds2}+G_L)}{C_{gd1}+C_{gd2}+C_{bd1}+C_{bd2}+C_L}$$

Output Amplifiers

CLASS A AMPLIFIERS



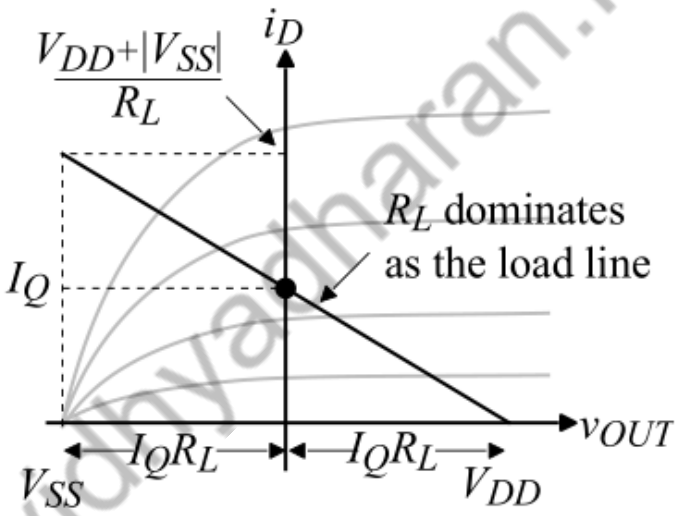
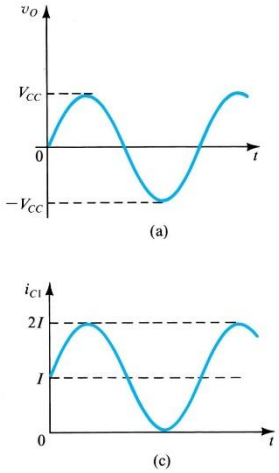


Fig. 5.5-1

$$\frac{I_{Lmin}}{2} = \frac{-V_{ss}}{R_L}$$

$$\frac{I_{Lmax}}{2} = \frac{V_{DD}}{R_L}$$



$$\text{Efficiency} = \frac{P_{RL}}{P_{Supply}} = \frac{\frac{v_{OUT}(\text{peak})^2}{2R_L}}{(V_{DD}-V_{SS})I_Q} = \frac{\frac{v_{OUT}(\text{peak})^2}{2R_L}}{(V_{DD}-V_{SS})\left(\frac{(V_{DD}-V_{SS})}{2R_L}\right)} = \left(\frac{v_{OUT}(\text{peak})}{V_{DD}-V_{SS}}\right)^2$$

Maximum efficiency occurs when $v_{OUT}(\text{peak}) = V_{DD} = |V_{SS}|$ which gives 25%.

Example-1

Design of CLASS A AMPLIFIERS

Assume that $K_N'=2K_P'=100\mu A/V^2$, $V_{TN}=0.5V$ and $V_{TP}=-0.5V$. Design the W/L ratios of M1 and M2 so that a voltage swing of $\pm 1V$ and a slew rate of $\cong 1\ V/\mu s$ is achieved if $R_L = 1\ k\Omega$ and $C_L = 1000\ pF$. Assume $V_{DD} = |V_{SS}| = 2V$ and $V_{GG2} = 0V$. Let $L = 1\ \mu m$ and assume that $C_{gd1} = 100fF$. Find the voltage gain and roots of this output amplifier.

Solution

Let us first consider the effects of R_L and C_L.

$$i_{OUT}(\text{peak}) = \pm 1V/1k\Omega = \pm 1000\mu A \quad \text{and} \quad C_L \cdot SR = 10^{-9} \cdot 10^{6} = 1000\mu A$$

Since the current for C_L and R_L occur at different times, choose a bias current of 1mA.

$$\frac{W_1}{L_1} = \frac{2(I_{OUT}^{-}+I_Q)}{K_N'(V_{DD}+|V_{SS}| - V_{TN})^2} = \frac{4000}{100\cdot(3.5)^2} \approx \frac{3\mu m}{1\mu m}$$

and

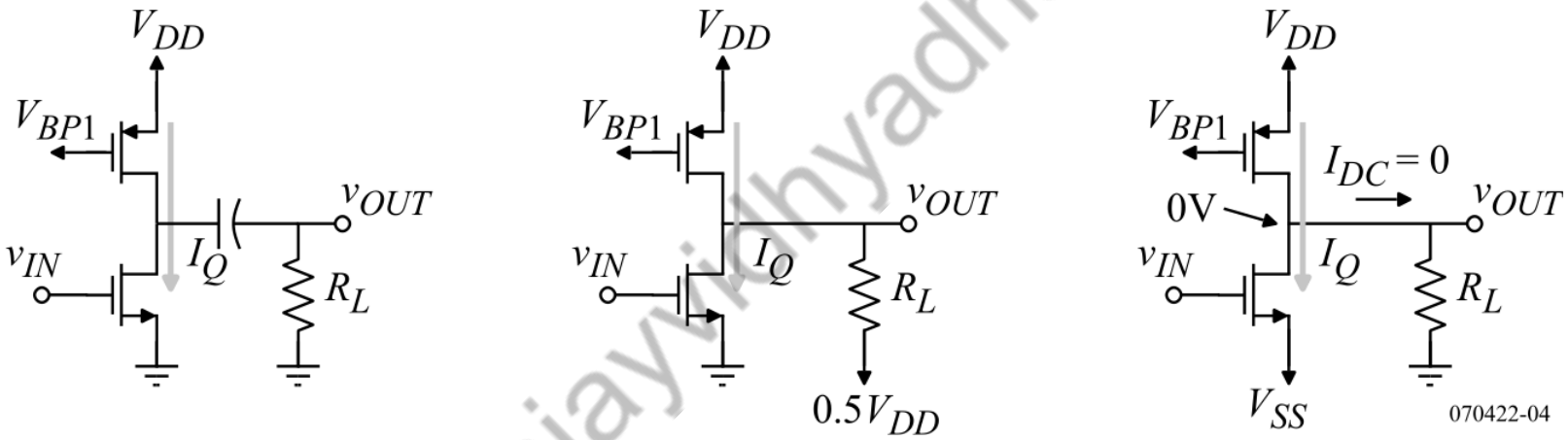
$$\frac{W_2}{L_2} = \frac{2I_{OUT}^{+}}{K_P'(V_{DD}-V_{GG2}-|V_{TP}|)^2} = \frac{2000}{50\cdot(1.5)^2} \approx \frac{18\mu m}{1\mu m}$$

The small-signal performance is $A_v = -0.775\ V/V$.

The roots are, zero $= g_{m1}/C_{gd1} \Rightarrow 1.23GHz$ and pole $\approx 1/(R_L C_L) \Rightarrow -159.15\ kHz$

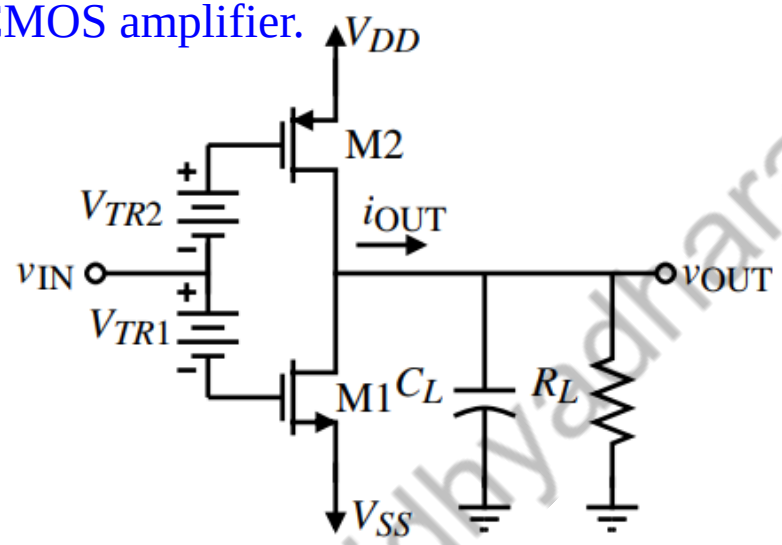
Output Amplifiers

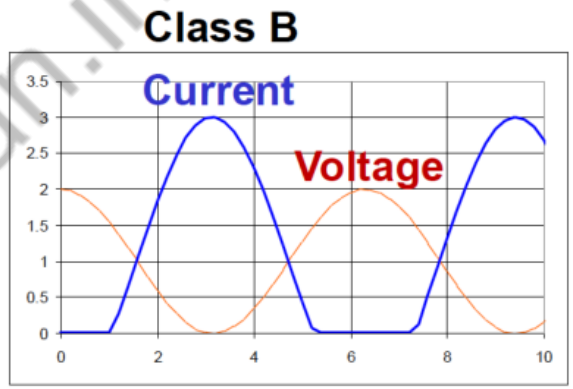
CS Amplfier with High I_Q.
Separation of the Amplifier Bias from the Load Resistance



Output Amplifiers

Push–pull inverting CMOS amplifier.





- Class B - one transistor has current flow for only 180° of the sinusoid (half period)

$$\therefore \text{ Efficiency} = \frac{P_{RL}}{P_{VDD}} = \frac{\dfrac{v_{OUT}(\text{peak})^2}{2R_L}}{(V_{DD} - V_{SS})\left(\dfrac{1}{2}\right)\left(\dfrac{2v_{OUT}(\text{peak})}{\pi R_L}\right)} = \frac{\pi}{2}\frac{v_{OUT}(\text{peak})}{V_{DD} - V_{SS}}$$

Maximum efficiency occurs when $v_{OUT}(\text{peak}) = V_{DD}$ and is 78.5%

- Class AB - each transistor has current flow for more than 180° of the sinusoid.

Maximum efficiency is between 25% and 78.5%

Thankyou