Advanced VLSI Design: 2022-23
Lecture 9
Logic Families Other than CMOS

By Dr. Sanjay Vidhyadharan

CMOS Differential Logic

They use both the variable and its complement as an input pair.

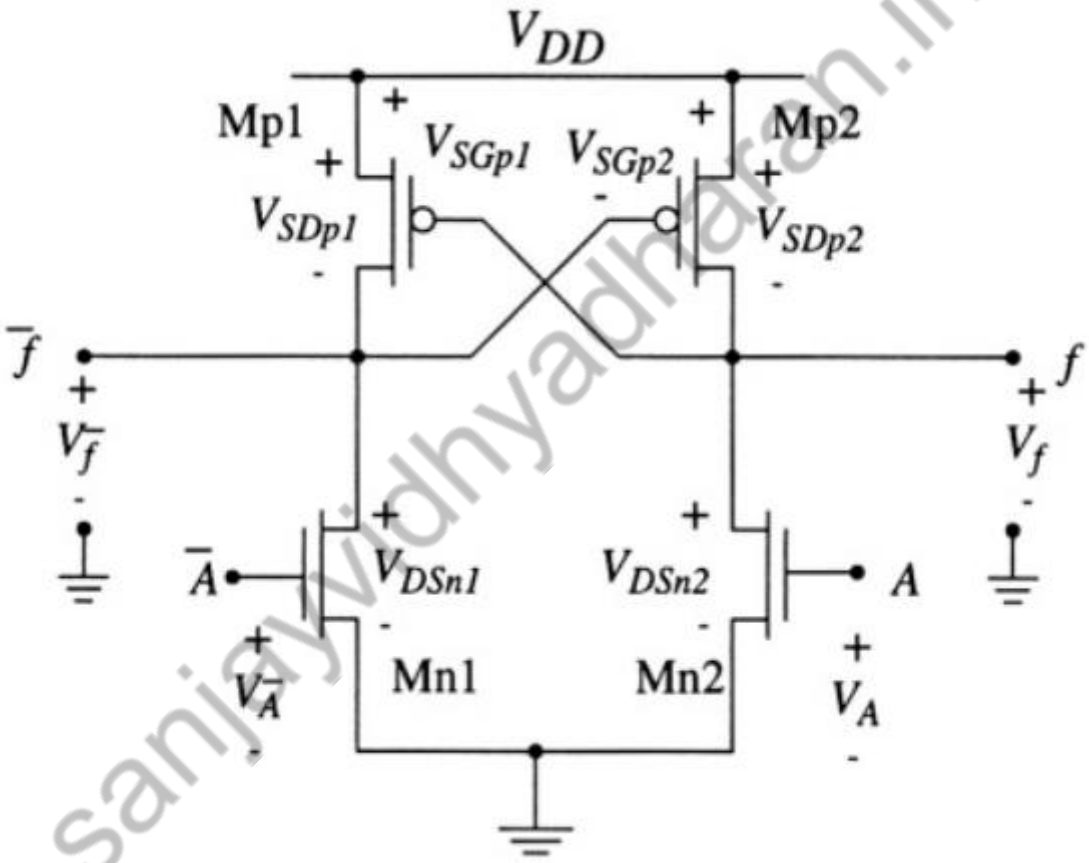
The dual rail logic interprets the **difference** as the logic variable instead of just one or the other. Some circuits can be made to react to small differences, giving us the term **differential logic.**

Viewed at the level of Boolean algebra, the use of both the variable and its complement is superfluous.

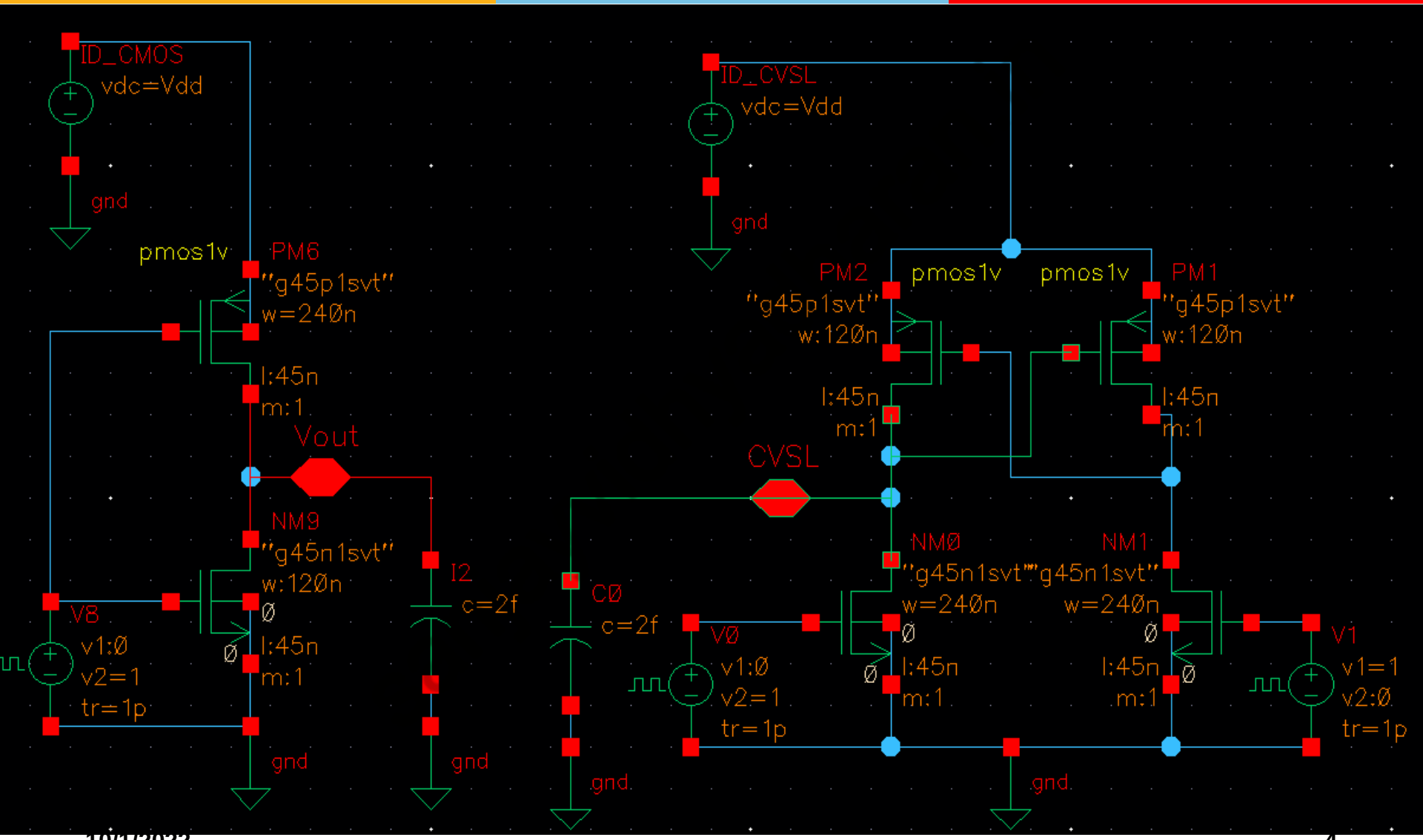
Dual rail networks are inherently more complicated to wire since interconnect lines must be allocated for twice as many signals.

The real advantage to using dual rail logic lies in the fact that an **electronic** dual rail circuit can be faster than an **electronic** single rail circuit.

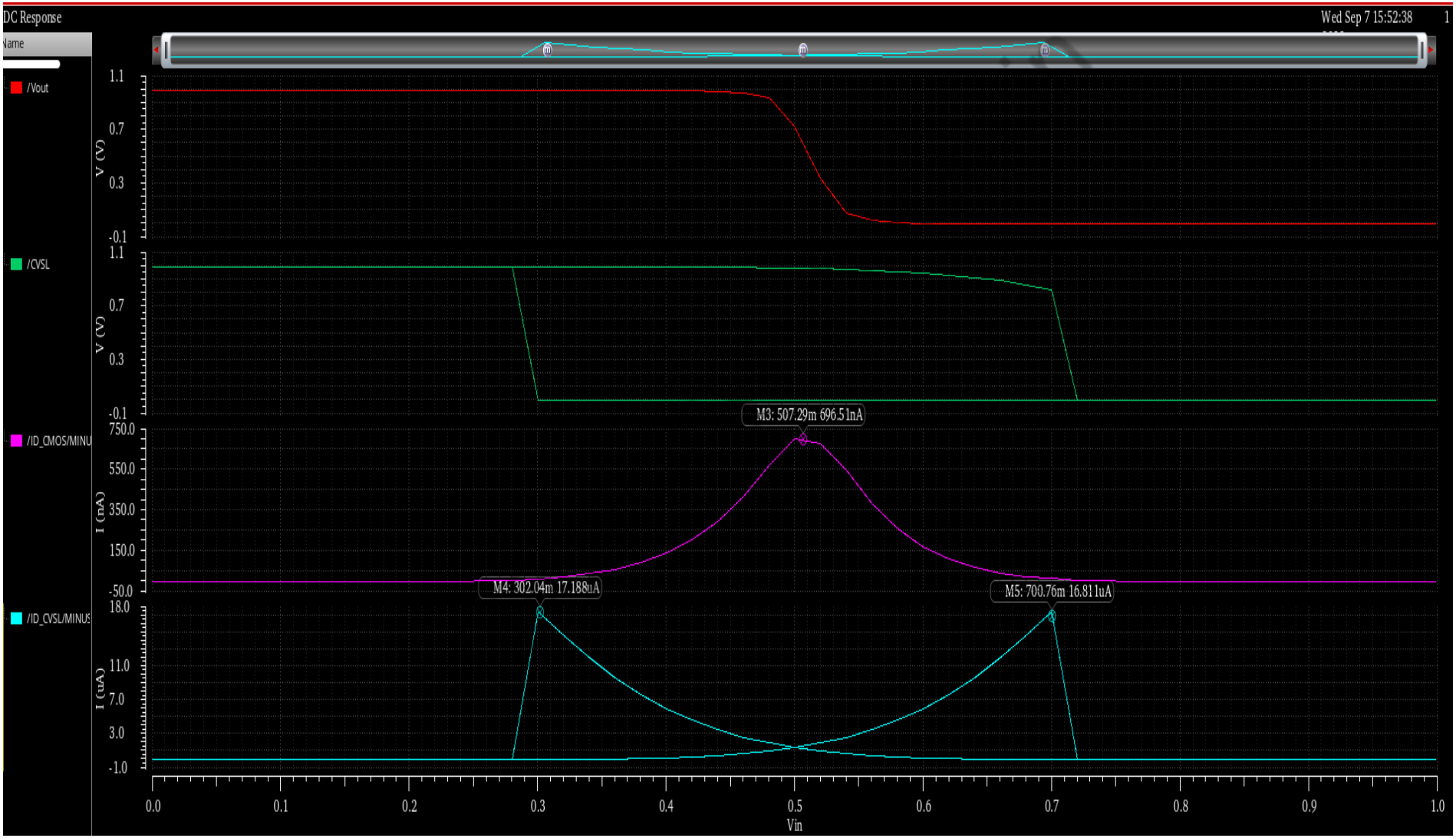
Cascode Voltage Switch Logic (CVSL)



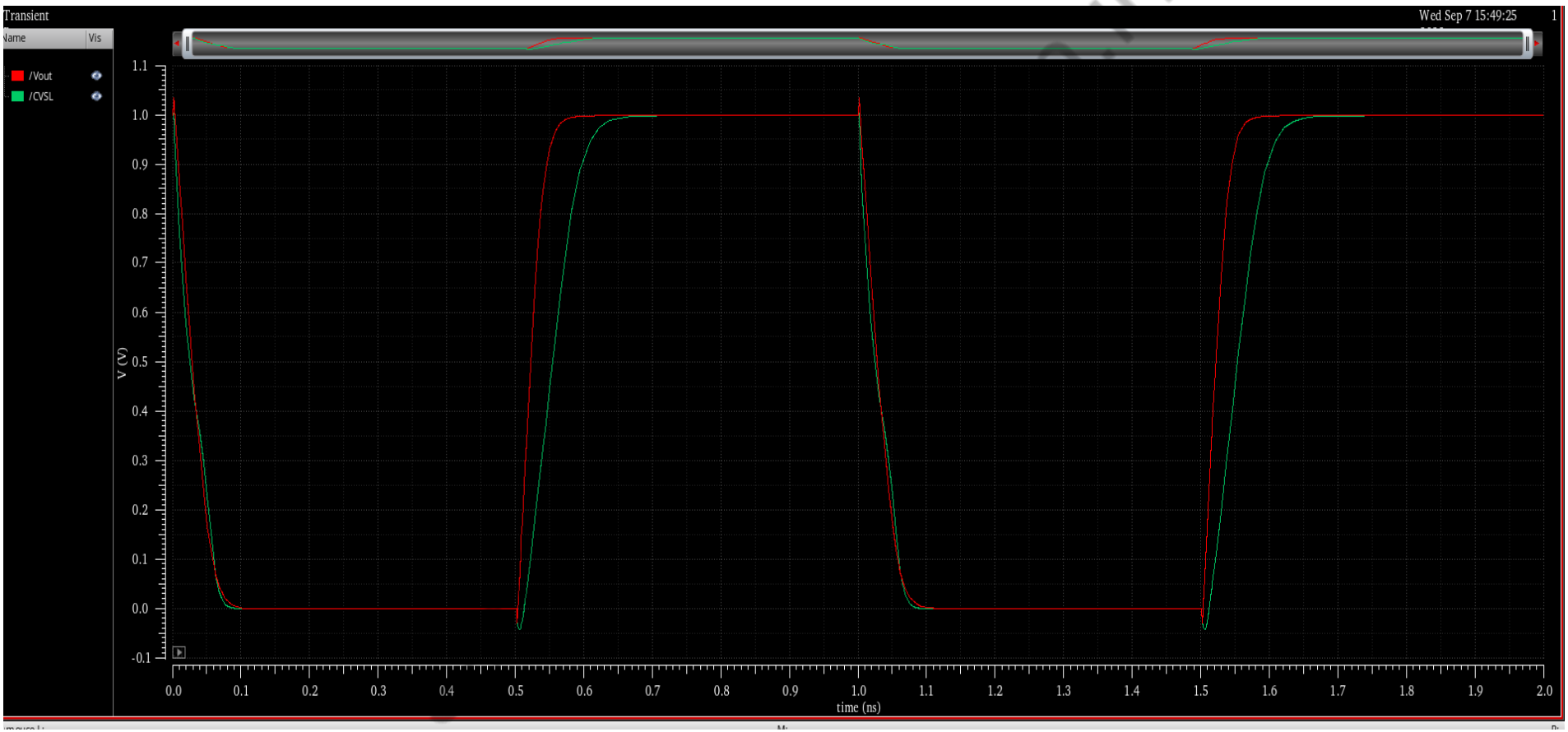
Cascode Voltage Switch Logic (CVSL)



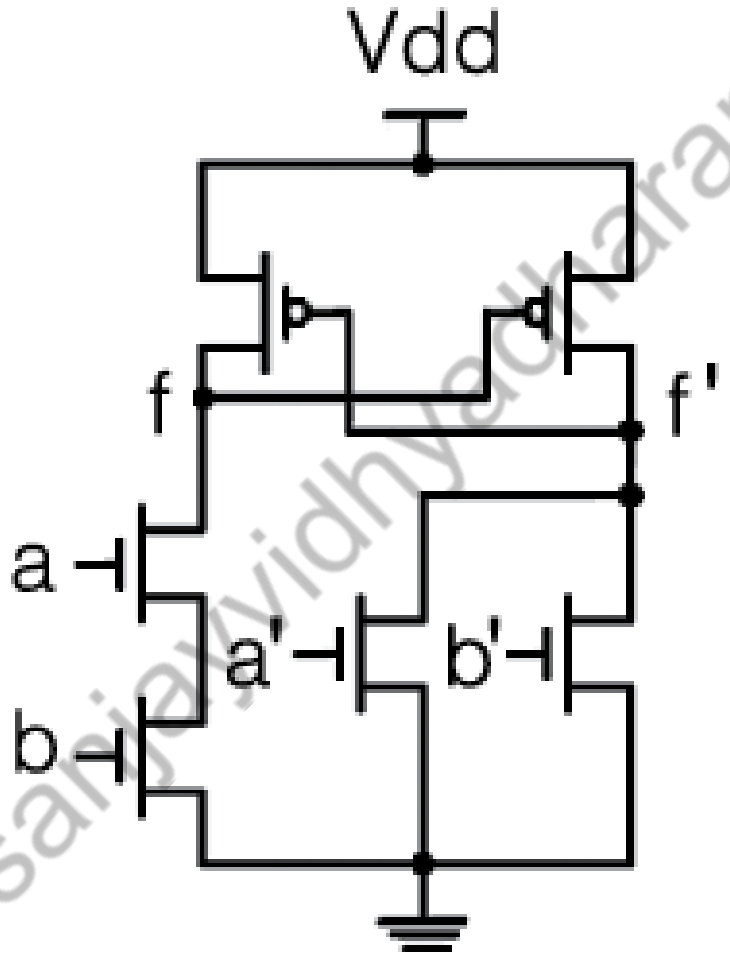
Cascode Voltage Switch Logic (CVSL)



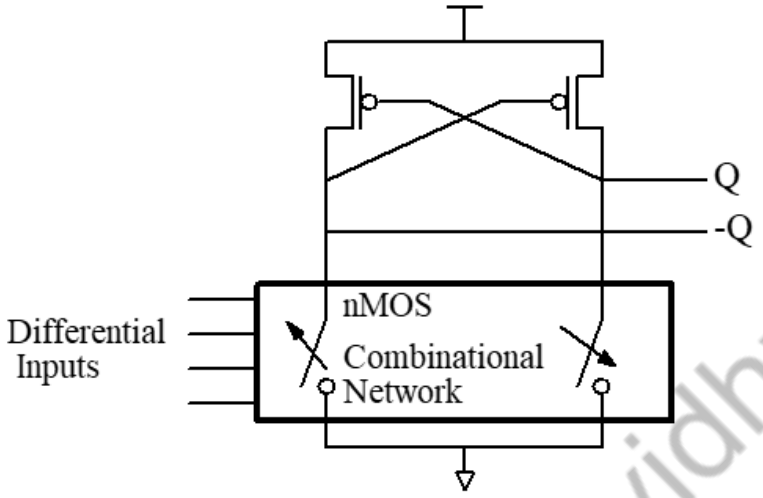
Cascode Voltage Switch Logic (CVSL)



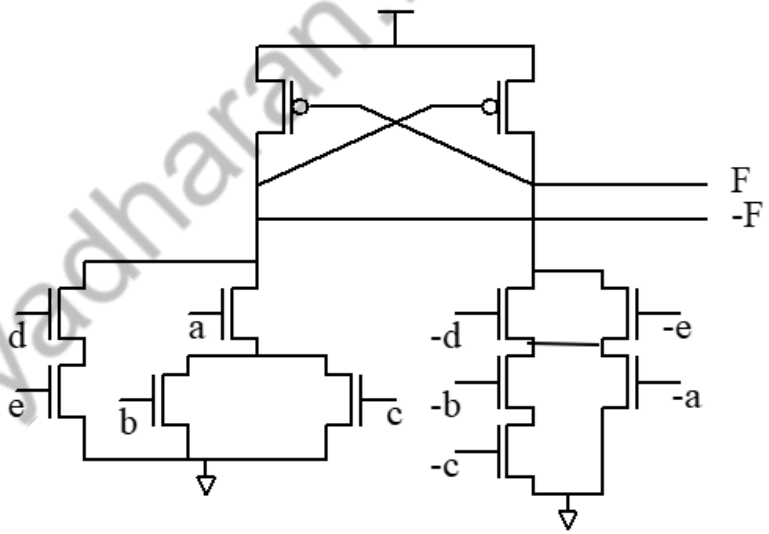
Cascode Voltage Switch Logic (CVSL)



Cascode Voltage Switch Logic (CVSL)



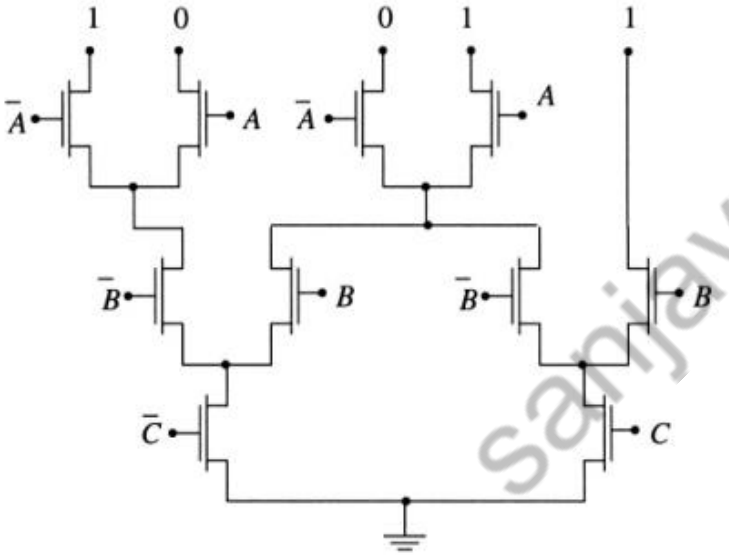
Basic version

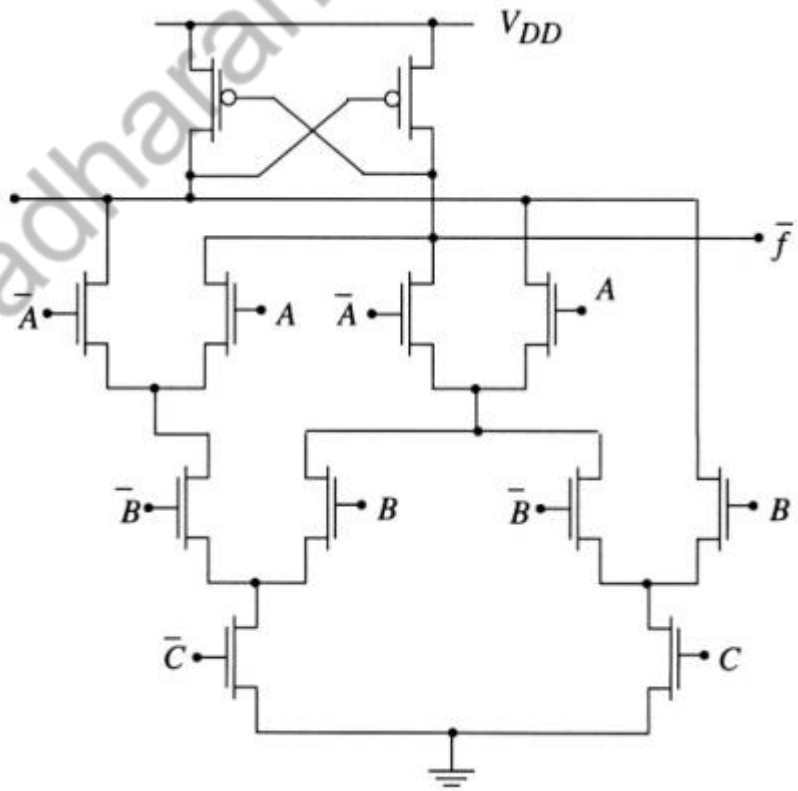


A particular function

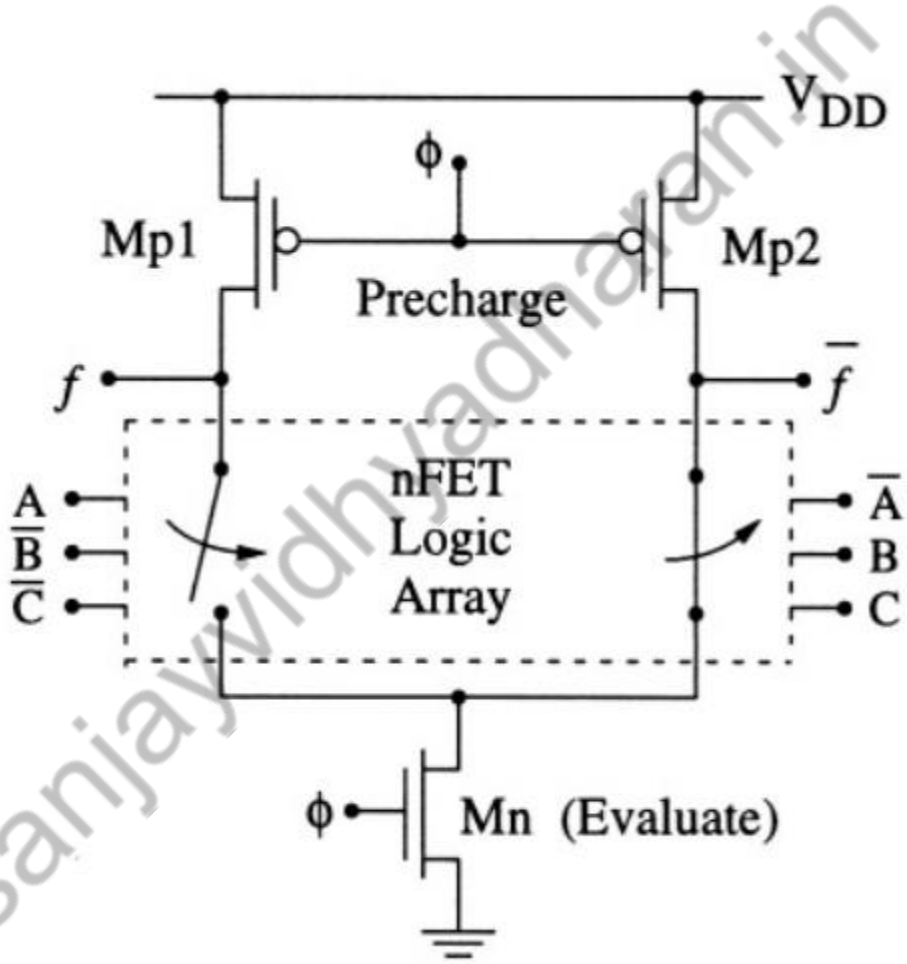
Cascode Voltage Switch Logic (CVSL)

f	1	0	0	1	0	1	1	1
A	0	1	0	1	0	1	0	1
B	0	0	1	1	0	0	1	1
C	0	0	0	0	1	1	1	1



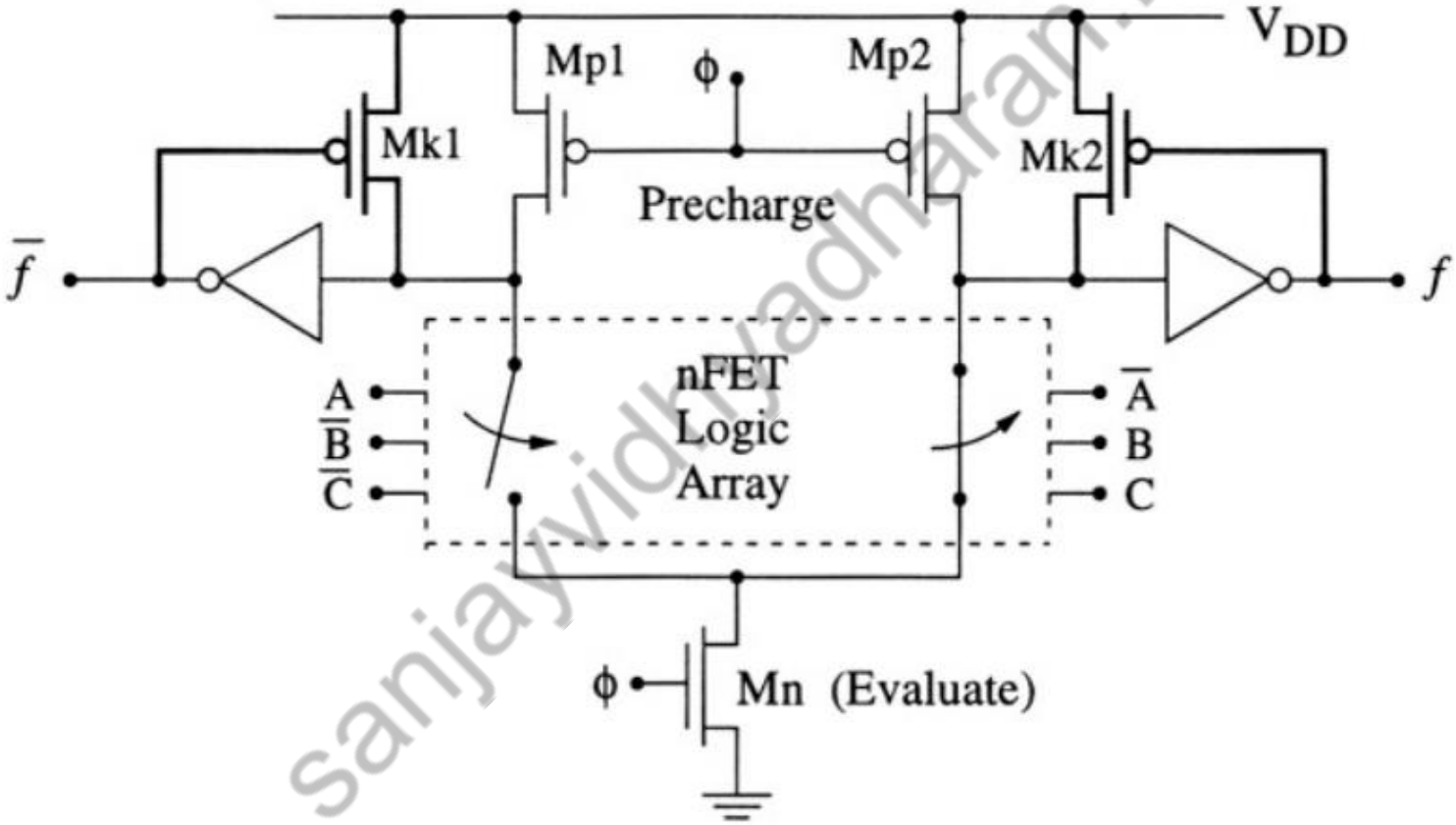


Dynamic CVSL

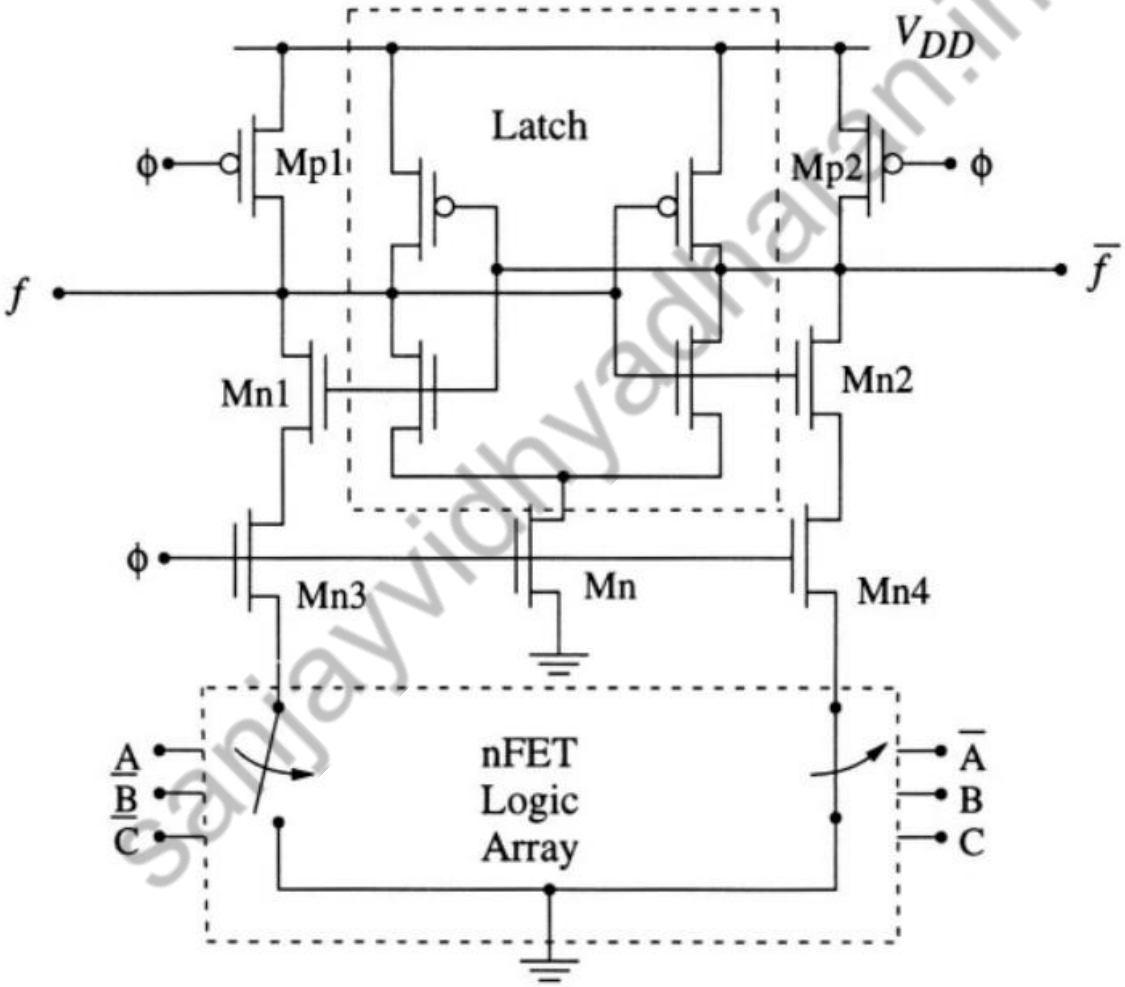


The real advantage to using dual rail logic lies in the fact that an **electronic** dual rail circuit can be faster than an **electronic** single rail circuit.

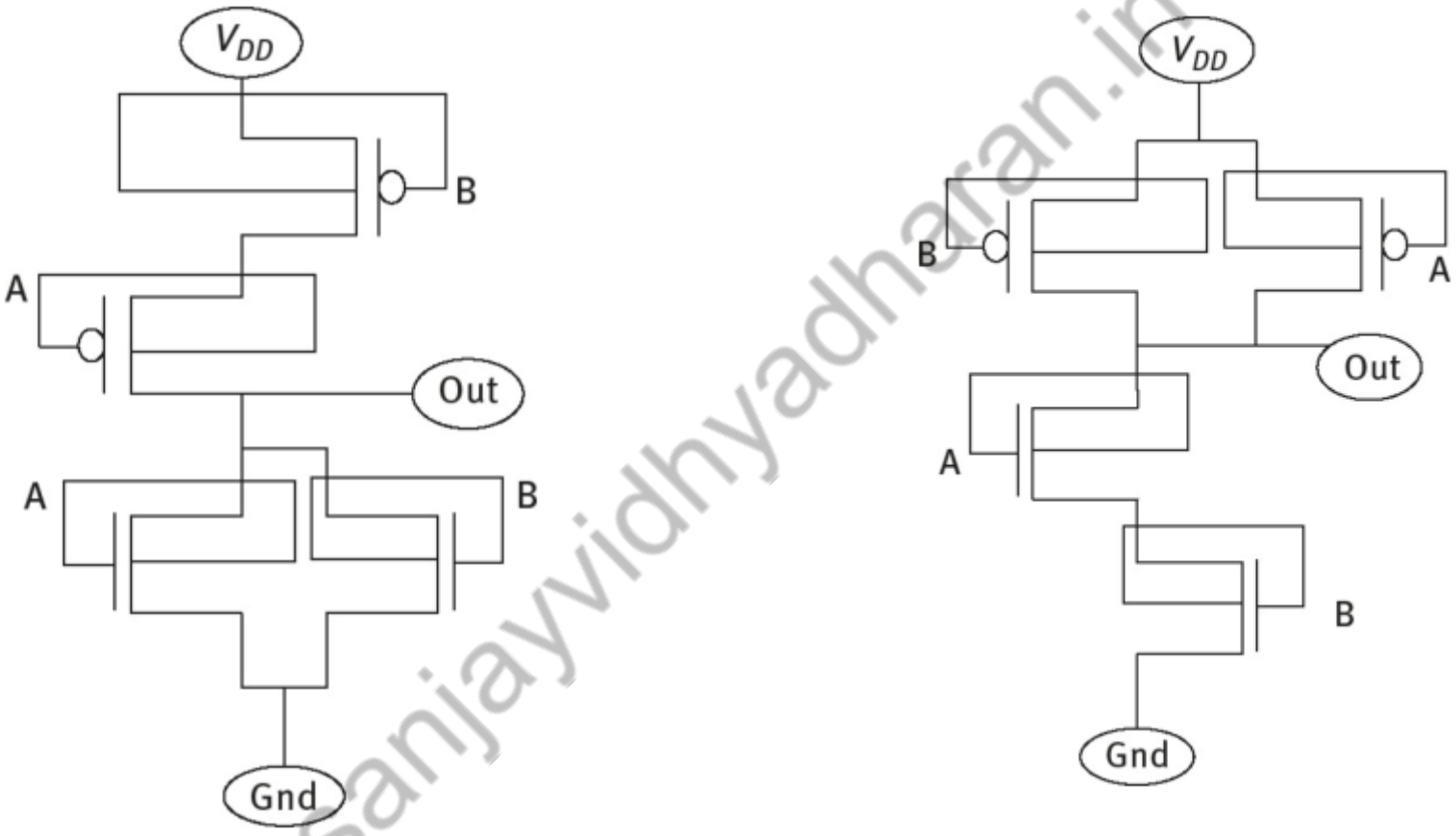
Dynamic CVSL with Charge Keepers



Differential current switch logic

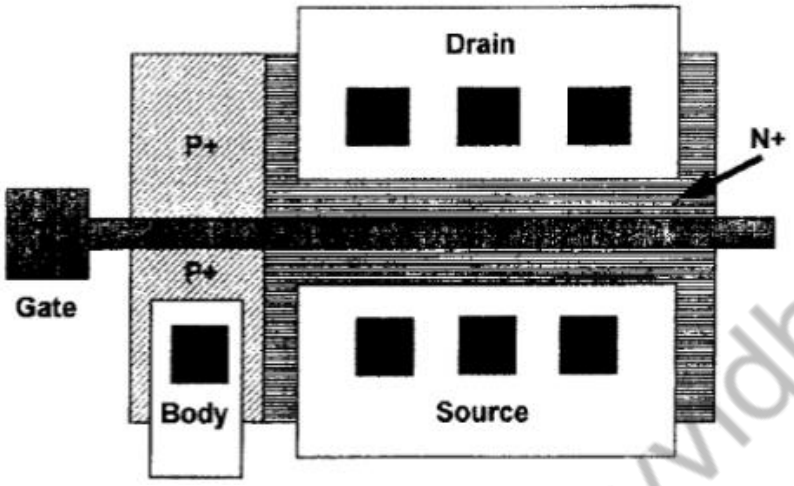


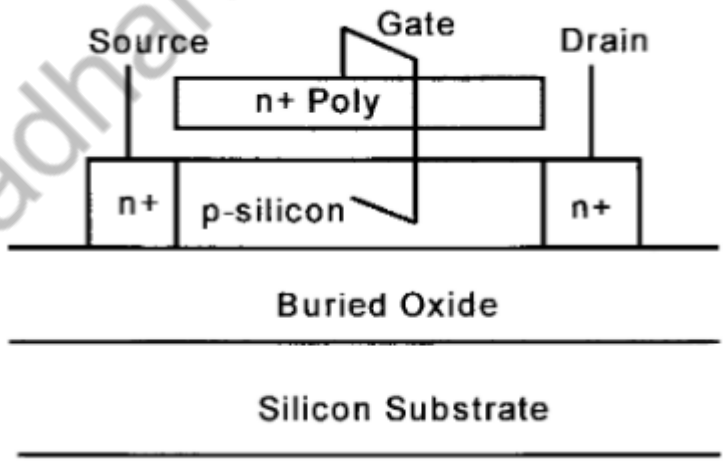
Dynamic threshold voltage MOSFET (DTMOS)



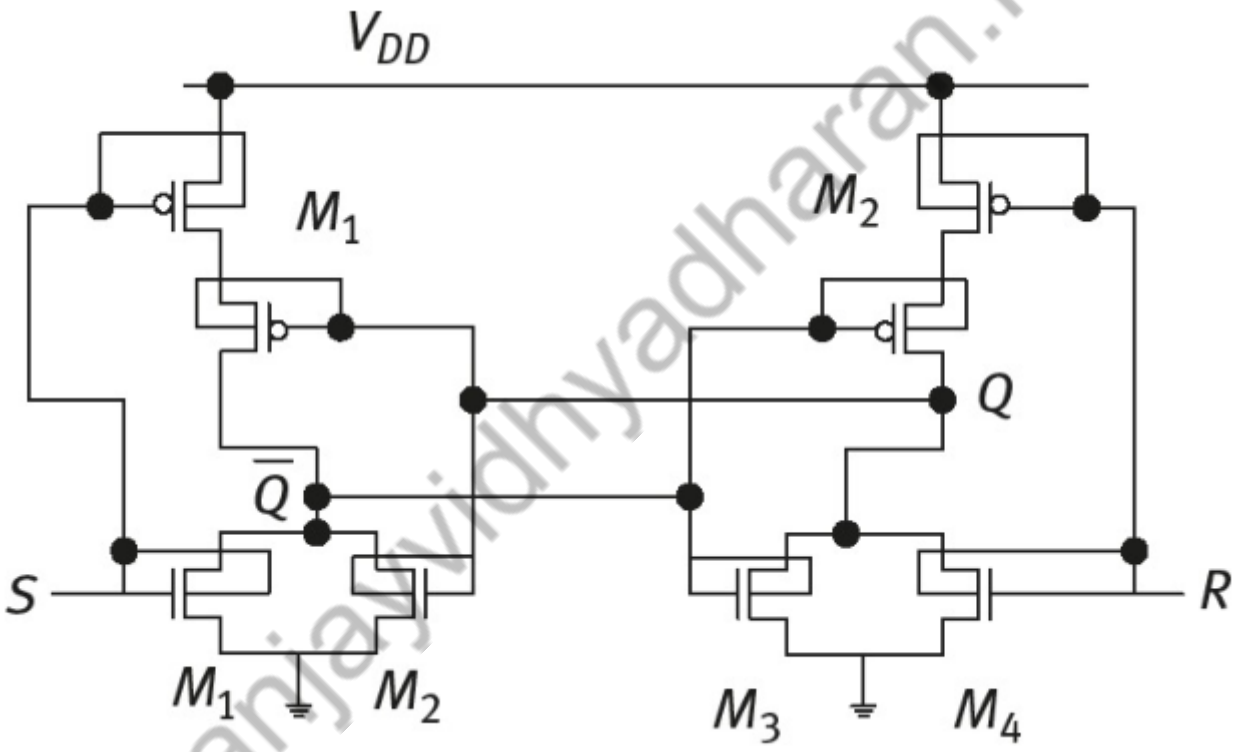
Subthreshold DTMOS logic circuit (a) NAND and (b) NOR.

Dynamic threshold voltage MOSFET (DTMOS)



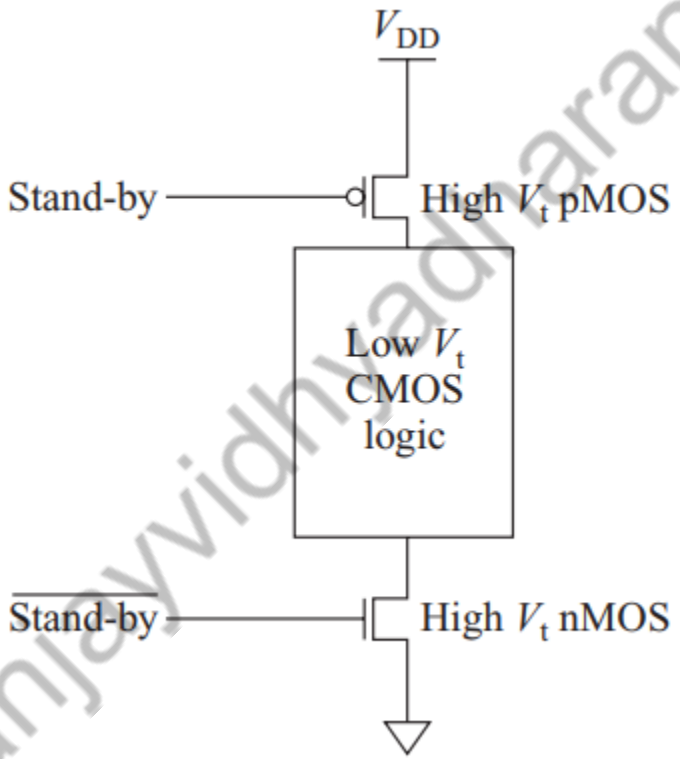


Dynamic threshold voltage MOSFET (DTMOS)



NOR-based SR flip-flop using DTMOS.

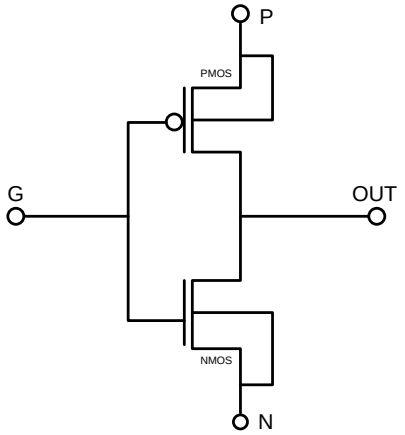
Dual Vt CMOS logic circuit



Gate Diffusion Input(GDI)

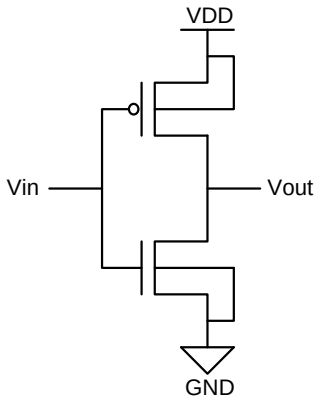
A GDI cell consists of three inputs:

1. G-common inputs to the gate of PMOS and NMOS
2. N-input to the source/drain of NMOS
3. P-input to the source/drain of



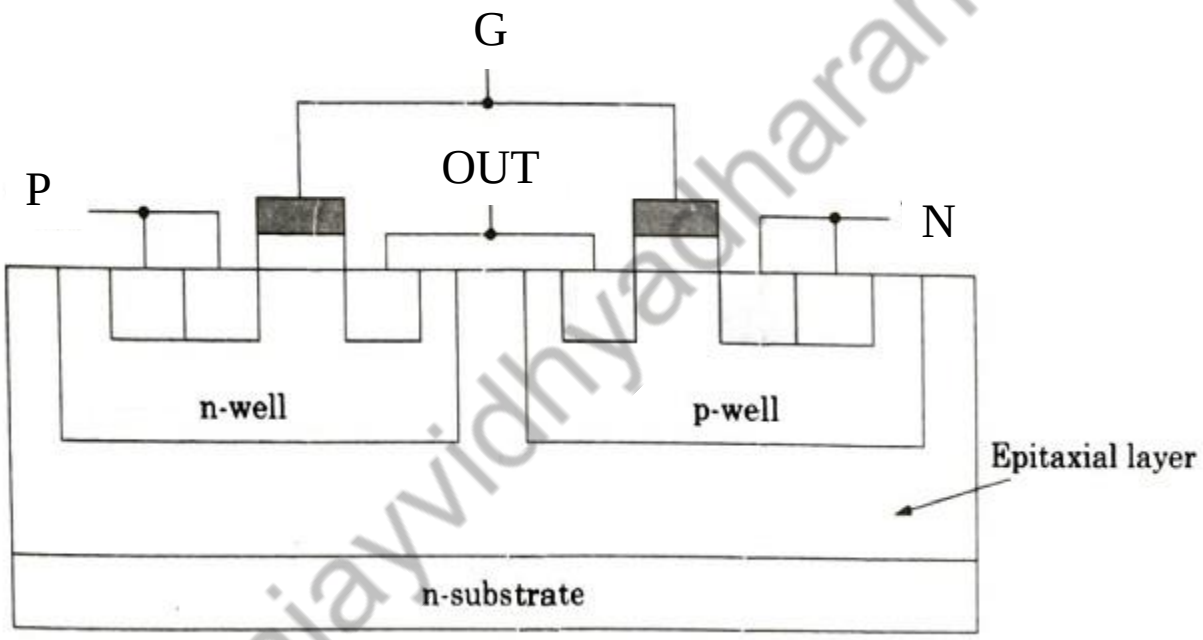
GDI Cell

❖One major difference between CMOS and GDI is that in GDI (N,P&G) terminals could be given a supply VDD or can be grounded or can be supplied with input signal depending upon the circuit to design and hence effectively minimizing the number of transistors used.



CMOS inverter

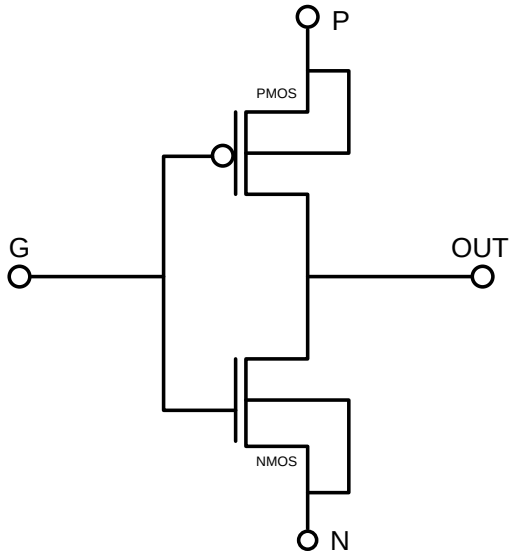
Gate Diffusion Input(GDI)



Gate Diffusion Input(GDI)

Logic function (GDI)

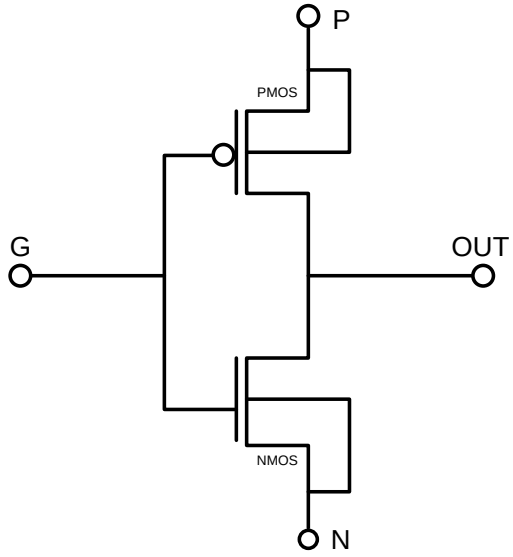
N	P	G	OUT	GATE
0	1	A	$\bar{A}$	NOT
B	0	A	AB	AND
1	B	A	A+B	OR



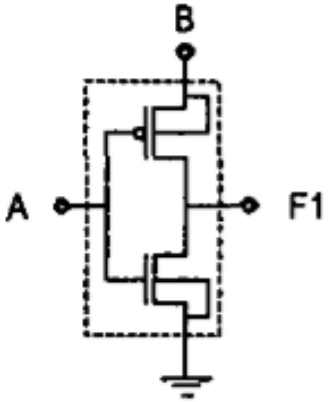
Gate Diffusion Input(GDI)

Logic function (GDI)

N	P	G	Out	Function
'0'	B	A	$\overline{A}B$	F1
B	'1'	A	$\overline{A}+B$	F2
'1'	B	A	$A+B$	OR
B	'0'	A	AB	AND
C	B	A	$\overline{A}B+AC$	MUX
'0'	'1'	A	$\overline{A}$	NOT



Gate Diffusion Input(GDI)



A	B	Functionality	F1
0	0	*pMOSTrans Gate*	V_{Tp}
0	V_{DD}	*CMOSInverter*	V_{DD}
V_{DD}	0	*nMOS Trans Gate*	0
V_{DD}	V_{DD}	*CMOSInverter*	0

Gate Diffusion Input(GDI)

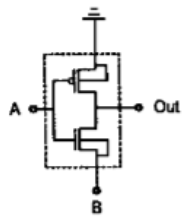
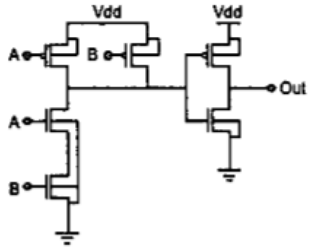
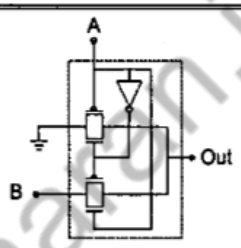
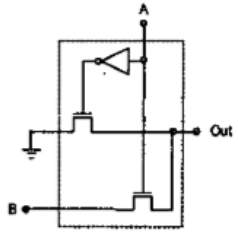
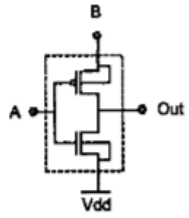
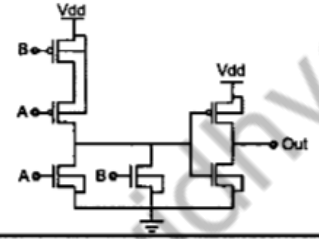
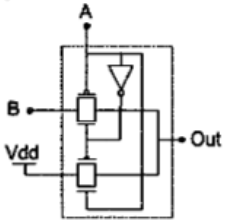
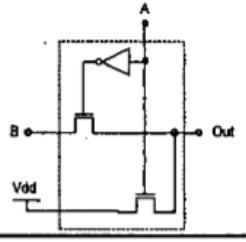
	GDI	CMOS	TG	N-PG
AND				
	2 transistors	6 transistors	6 transistors	4 transistors
OR				
	2 transistors	6 transistors	6 transistors	4 transistors

Table 3. AND and OR cells using GDI, CMOS and PTL design techniques for twin well process.

Morgenshtein, A., Fish, A., & Wagner, I. A. (n.d.). Gate-diffusion input (GDI) - a technique for low power design of digital circuits: analysis and characterization. 2002 IEEE International Symposium on Circuits and Systems. Proceedings (Cat. No.02CH37353). doi:10.1109/iscas.2002.1009881

Gate Diffusion Input(GDI)

Gate type in series	Logic expression	GDI			CMOS			TG			N-PG		
		Power (μW)	Delay (nsec)	# tr.	Power (μW)	Delay (nsec)	# tr.	Power (μW)	Delay (nsec)	# tr.	Power (μW)	Delay (nsec)	# tr.
MUX	$\overline{A}B + AC$	35.7	1.1	8	49.7	2.1	24	44.9	1.0	16	47.5	3.1	16
OR	$A + B$	26.3	1.2	8	32.9	1.7	12	36.2	1.3	16	32.6	2.7	16
AND	AB	25.7	0.9	8	34.1	1.4	12	30.8	0.8	16	30.1	2.8	16
F1	$\overline{A}B$	31.2	0.8	8	45.2	1.5	12	31.8	1.1	16	31.8	2.5	16
F2	$\overline{A} + B$	32.0	1.3	8	43.1	1.9	12	33.2	1.4	16	29.6	3.5	16

Table 4. Logic gates comparisons (GDI, CMOS, Transmission Gate and n-MOS Pass Gate). Two cells and buffers are taken into account in each number of transistors.

Morgenshtein, A., Fish, A., & Wagner, I. A. (n.d.). Gate-diffusion input (GDI) - a technique for low power design of digital circuits: analysis and characterization. 2002 IEEE International Symposium on Circuits and Systems. Proceedings (Cat. No.02CH37353). doi:10.1109/iscas.2002.1009881

BiCMOS

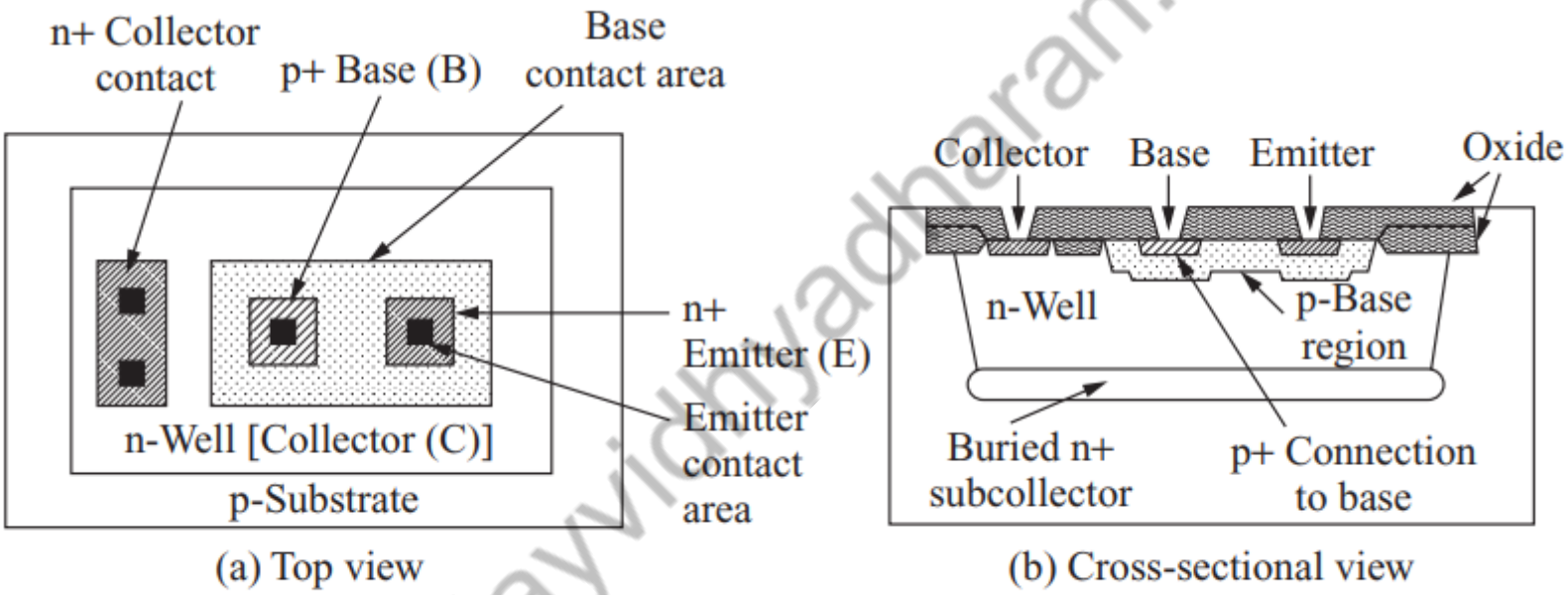
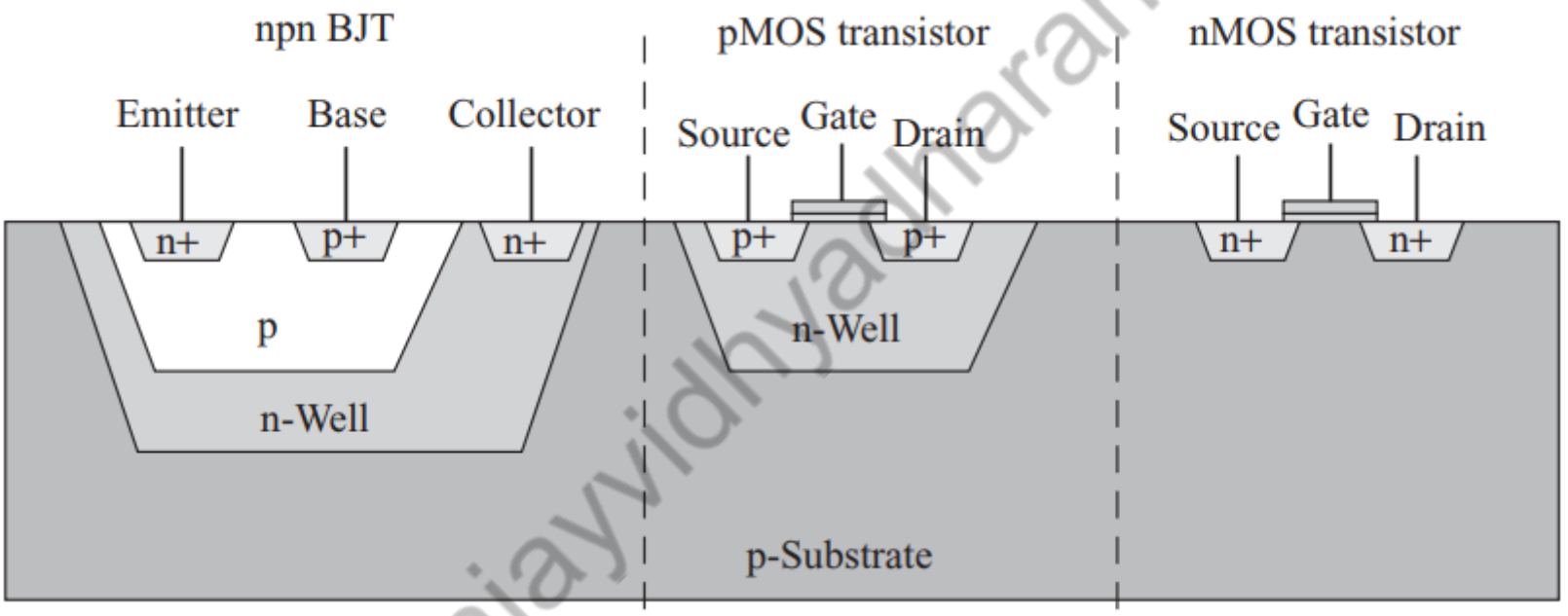


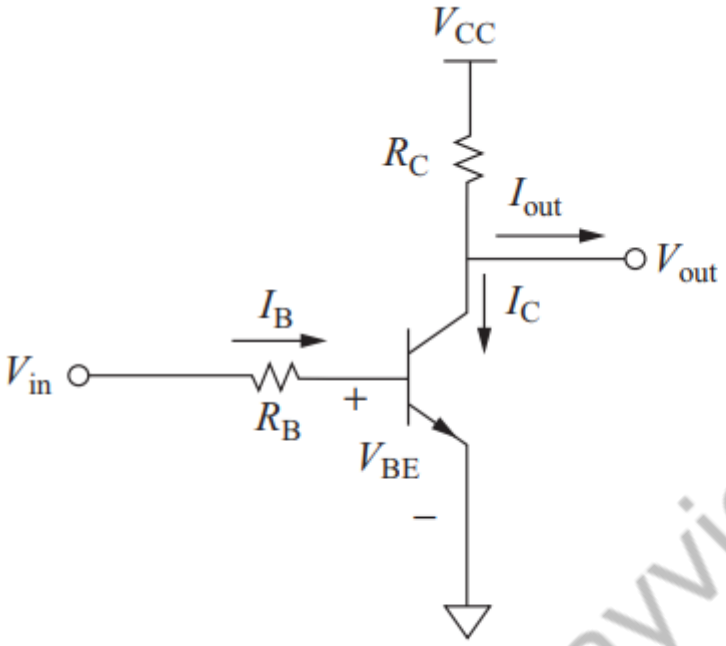
Fig. 8.1 Bipolar junction transistor: (a) top view; (b) cross-sectional view

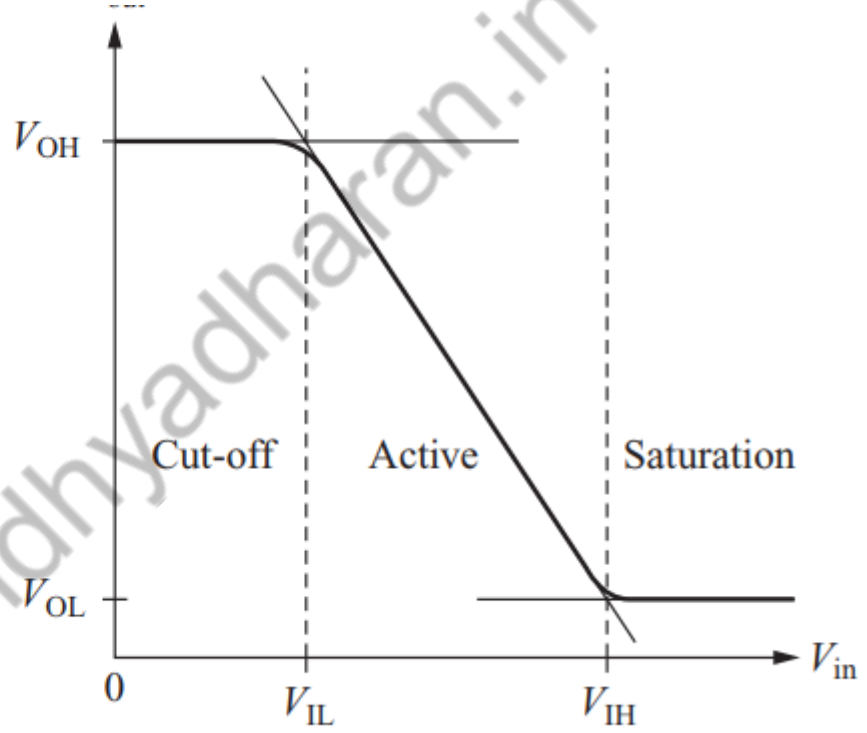
BiCMOS



Advantages of BJT
Higher switching speed
Higher current drive per unit area, higher gain

BiCMOS

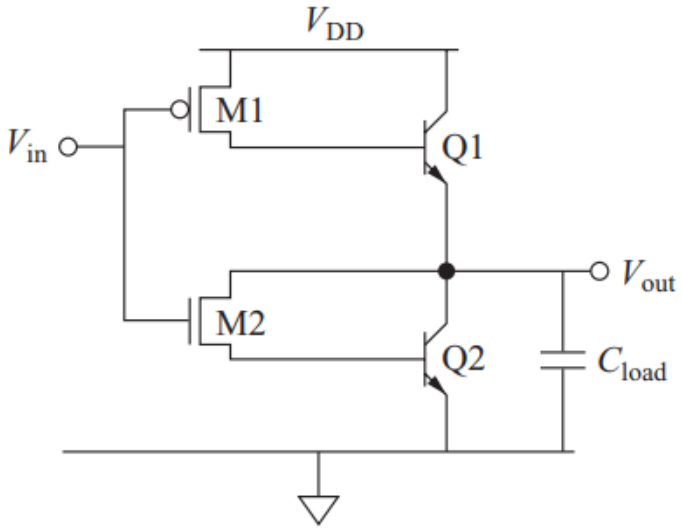




$$V_{OH} = V_{CC}$$

$$V_{OL} = V_{CE,sat}$$

BiCMOS



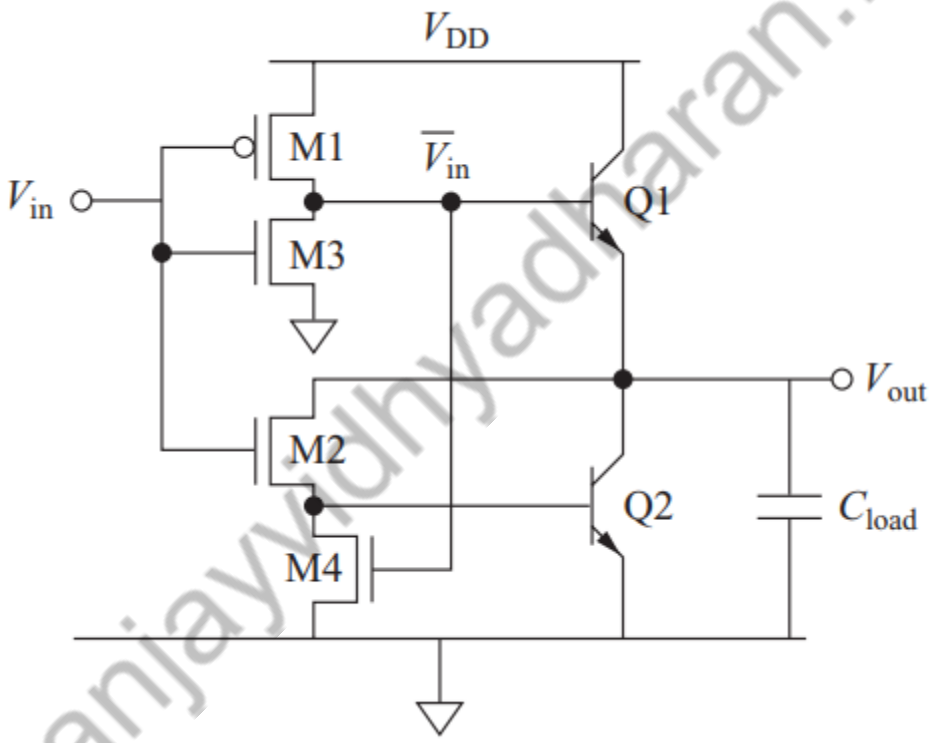
$$V_{OH} = V_{DD} - V_{BE,Q1}$$

$$V_{OL} = V_{CE,sat.Q2}$$

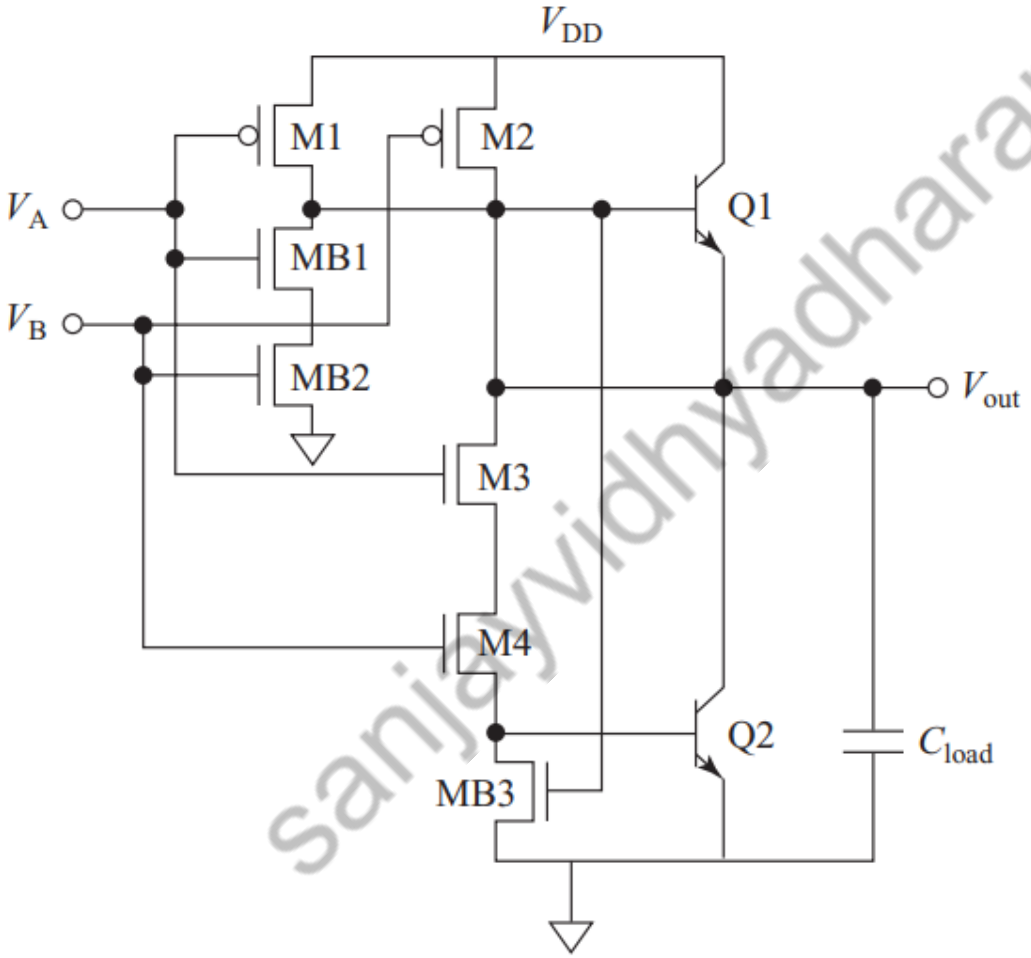
- The transistors Q1 and Q2 present low impedances when turned ON into saturation and the load capacitance will be charged or discharged rapidly
- Output logic levels will be close to rail voltages. As $V_{CE\text{-}SAT}$ is quite small Output logic levels will be close to rail voltages.
- The inverter has high input impedance due to the MOS gate input. The inverter has low output impedance.
- BiCMOS inverter noise margins will also be good.
- The inverter has high input impedance due to the MOS gate input. The inverter has low output impedance.
- The inverter has high drive capability but occupies a relatively small area

There is no discharge path for current from the base of either bipolar transistor when it is being turned OFF. Not Suitable for High-Speed operation

BiCMOS Inverter with base pull-down transistor



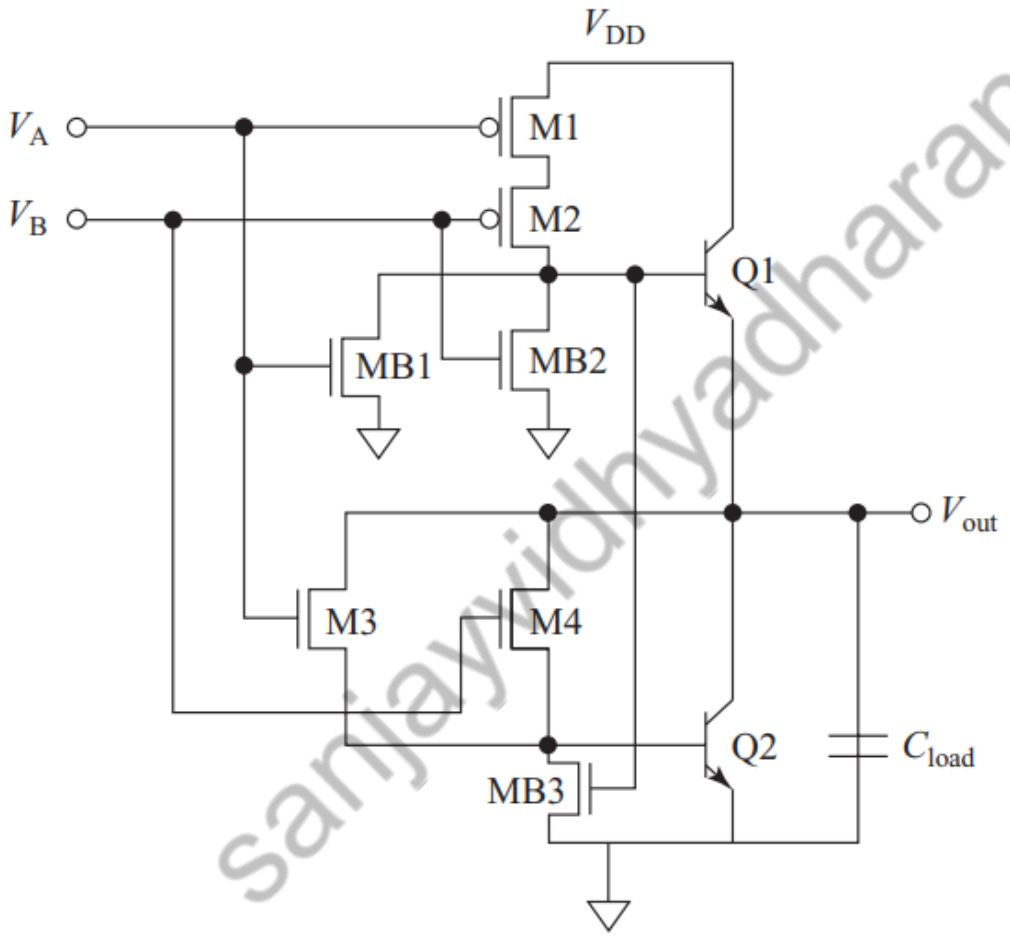
BiCMOS NAND



A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

(b)

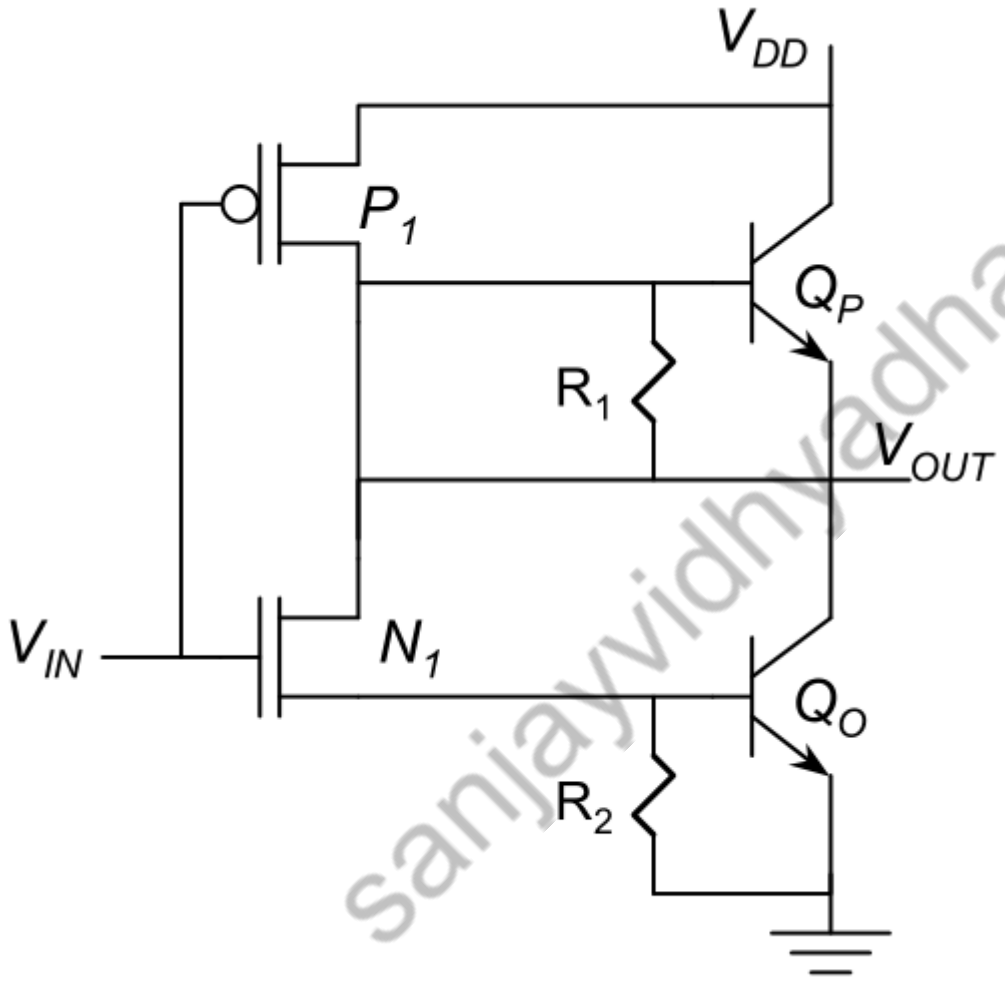
BiCMOS NOR



A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

(b)

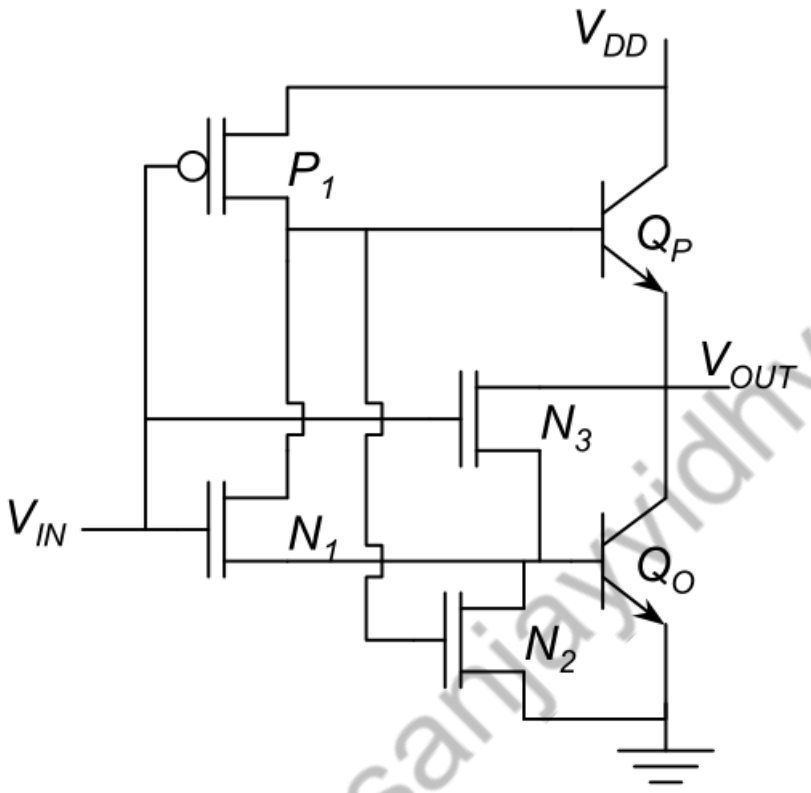
Full-Rail BiCMOS with Resistive Shunts



$V_{OH} = V_{DD}$

$V_{OL} = 0$

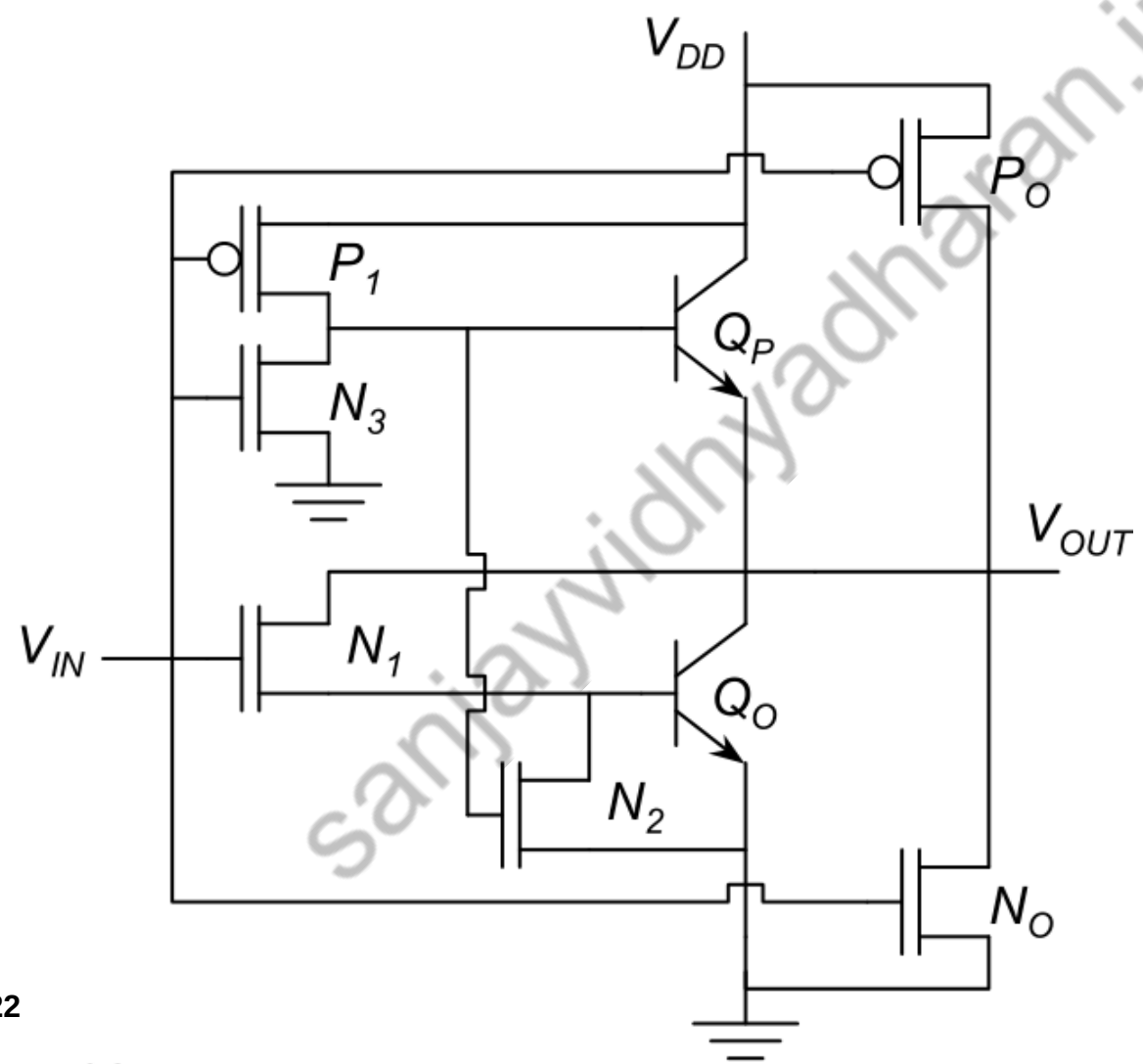
Full-Rail BiCMOS with Active Shunts



$V_{OH} = V_{DD} - V_{BEA}$

$V_{OL} = 0$

Full-Rail BiCMOS with Paralleled CMOS Inverter

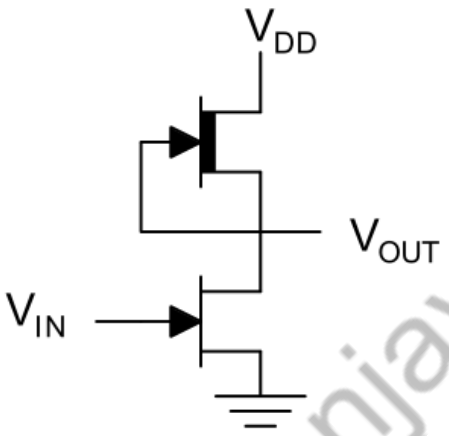


$V_{OH} = V_{DD}$

$V_{OL} = 0$

GaAs Direct-Coupled FET Logic

DCFL Inverter



- DCFL gates are similar to NMOS circuits, but are implemented with GaAs MESFET's rather than Si MOSFET's.
- The advantage of DCFL is speed - it is up to 3 times faster than CMOS.
- The disadvantages of DCFL are fabrication complexity and cost.
  - GaAs 75 mm wafer - $100
  - Si 200 mm wafer - $10
  - Si 300 mm wafers - coming soon!
  - GaAs technology is less established compared to Si technology, and the fabrication of enhancement type MESFET's is difficult.

GaAs Direct-Coupled FET Logic

DCFL Characteristics

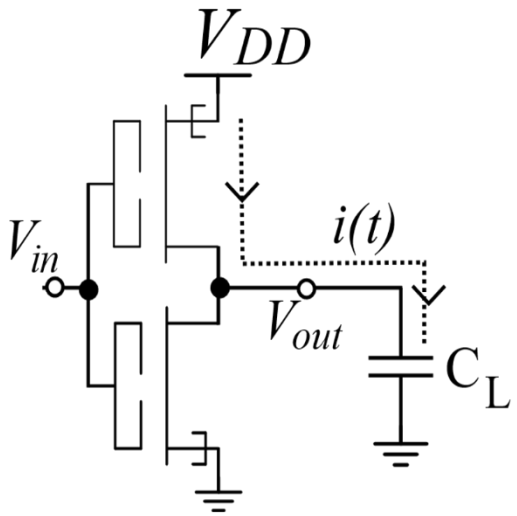
Compare the 1999 state-of-the art for GaAs DCFL and Si CMOS:

GaAs DCFL vs. Si CMOS: 0.25 μm technology		
	GaAs DCFL	Si CMOS
propagation delay	35 ps	75 ps
dissipation	30 μW (DC)	1 μW / MHz
SRAM embedded in VLSI	32 kB	128 kB

- GaAs exhibits higher electron mobility than Si.
- Due to the GaAs electron velocity characteristic, DCFL can operate at a reduced supply voltage without a penalty in switching speed.

Adiabatic Logic

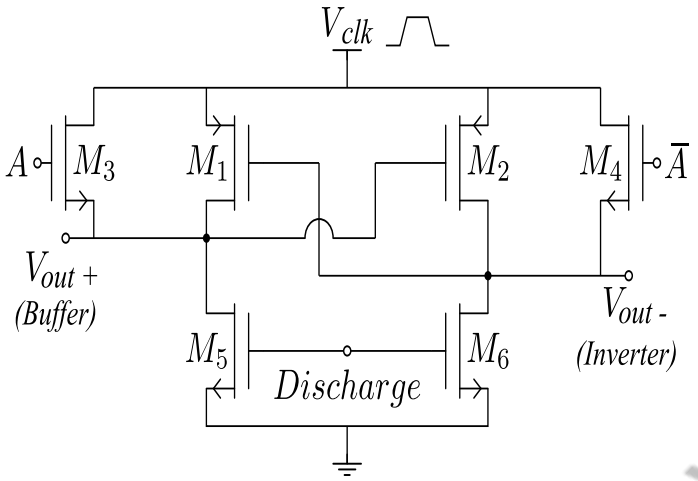
1. Adiabatic Operation

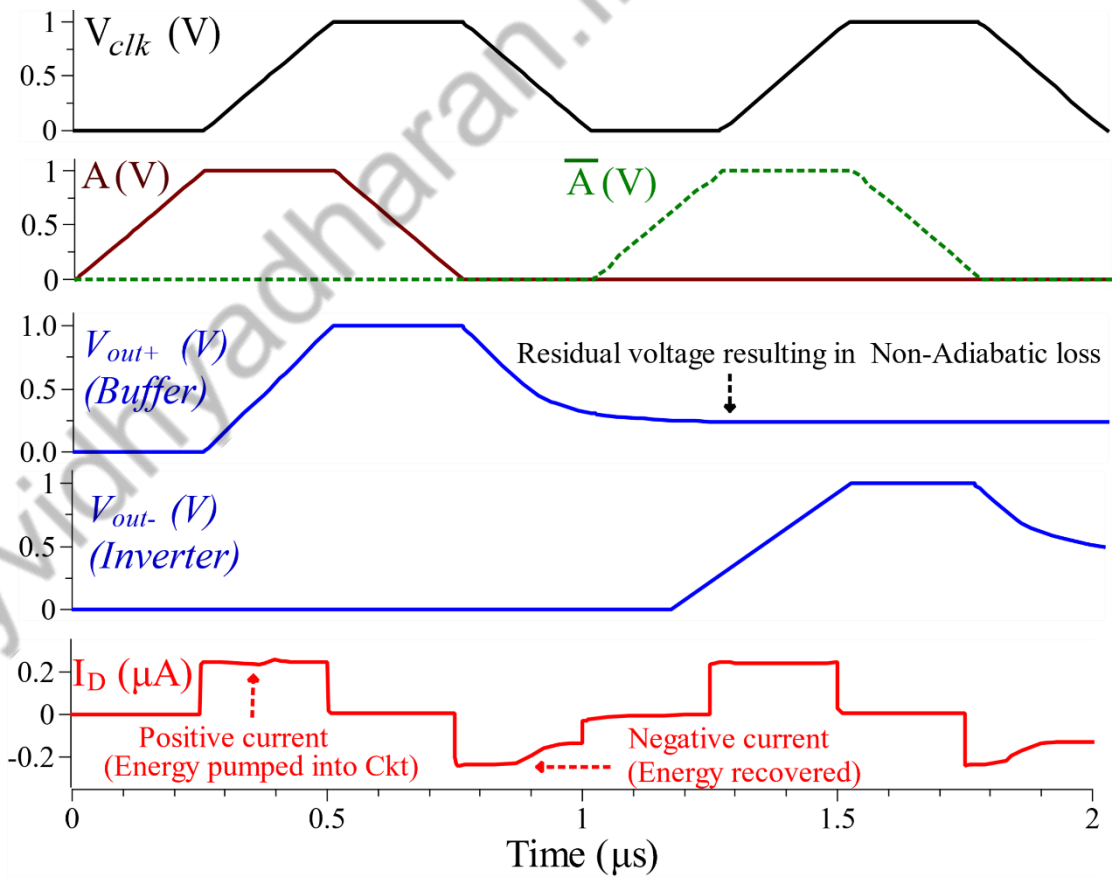


Power Supply (V_{DD})		*Energy dissipated in pGOTFET*
DC		$= \frac{V_{DD}^2 C_L}{2}$
Two Steps V_{DD}		$= \frac{V_{DD}^2 C_L}{4}$
n Steps V_{DD}		$= \frac{V_{DD}^2 C_L}{2*n}$
Slow Ramp Clk		Negligible

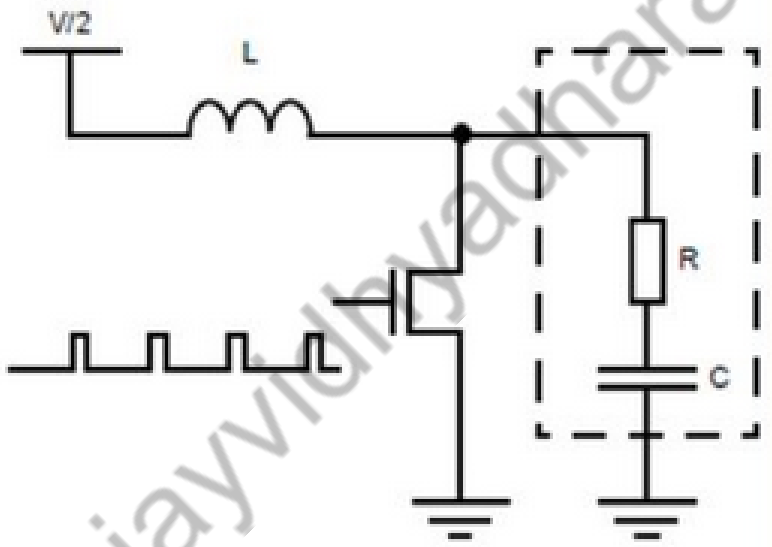
Adiabatic Logic

CMOS Symmetric Pass Gate Adiabatic Logic

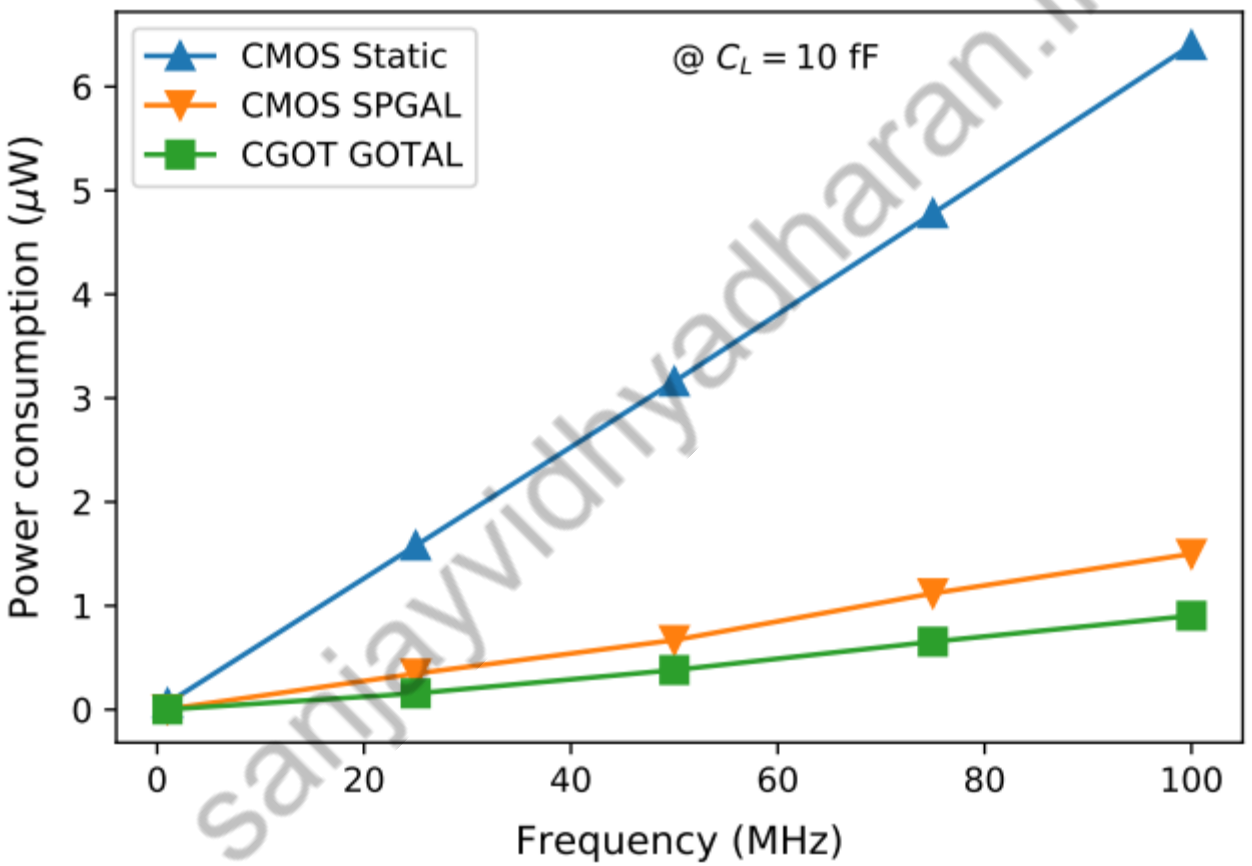




Adiabatic Logic



Adiabatic Logic vs. Static CMOS



Sanjay Vidhyadharan et all "An advanced adiabatic logic using Gate Overlap Tunnel FET (GOTFET) devices for ultra-low power VLSI sensor applications"

Thank you