Analog IC Design : 2022-23
Lecture 11
Operational Amplifiers

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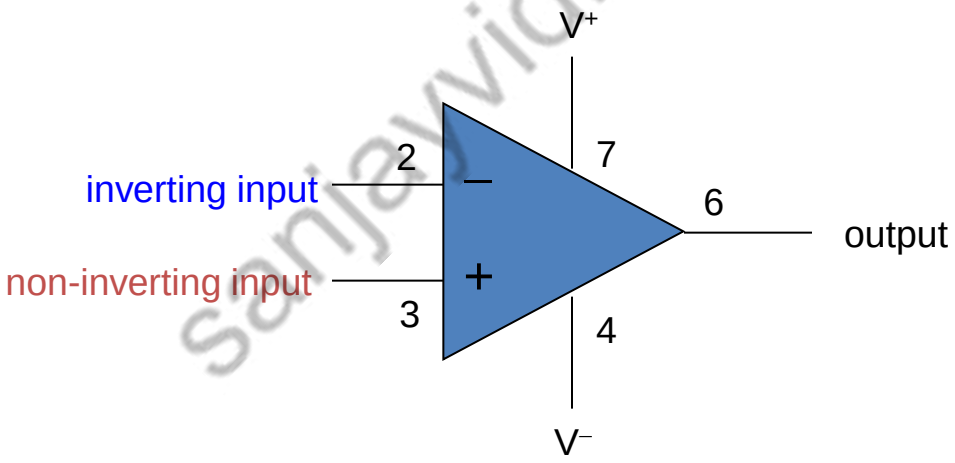
Operational Amplifiers

Op-amps (amplifiers/buffers in general) are drawn as a triangle in a circuit schematic
There are two inputs
    inverting and non-inverting
And one output
Also power connections (note no explicit ground)



The Ideal Operational Amplifiers

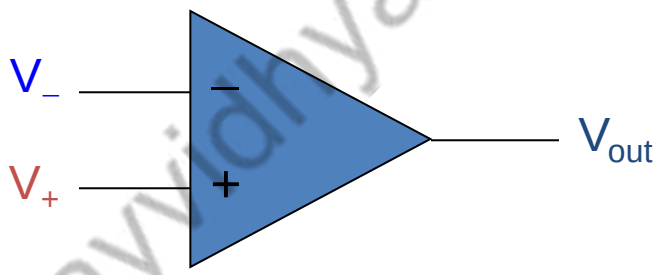
- Infinite voltage gain
  - a voltage difference at the two inputs is magnified infinitely
  - in truth, something like 200,000
  - means difference between + terminal and – terminal is amplified by 200,000!
- Infinite input impedance
  - no current flows into inputs
  - in truth, about 10^{12} Ω for FET input op-amps
- Zero output impedance
  - rock-solid independent of load
  - roughly true up to current maximum (usually 5–25 mA)
- Infinitely fast (infinite bandwidth)
  - in truth, limited to few MHz range
  - slew rate limited to 0.5–20 V/μs

Op-amp without feedback

- The internal op-amp formula is:

$$V_{out} = gain \times (V_+ - V_-)$$

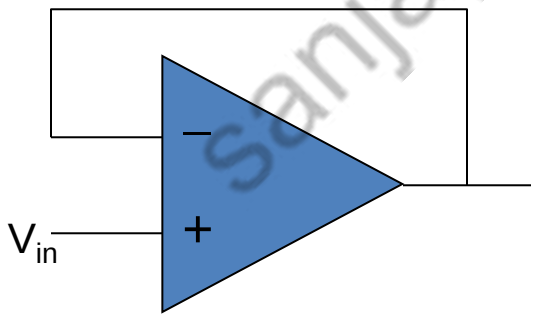
- So if V_+ is greater than V_-, the output goes positive
- If V_- is greater than V_+, the output goes negative



- A gain of 200,000 makes this device (as illustrated here) practically useless

Negative feedback

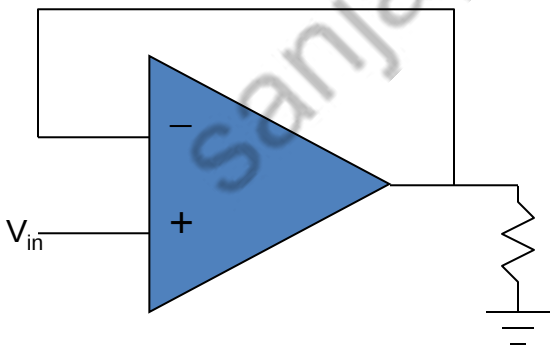
- Infinite gain would be useless except in the self-regulated negative feedback regime
  - negative feedback seems bad, and positive good—but in electronics positive feedback means runaway or oscillation, and negative feedback leads to stability
- Imagine hooking the output to the inverting terminal:
- If the output is less than V_{in}, it shoots positive
- If the output is greater than V_{in}, it shoots negative
  - result is that output quickly forces itself to be exactly V_{in}



negative feedback loop

Negative feedback

- Even if we load the output (which as pictured wants to drag the output to ground)…
  - the op-amp will do everything it can within its current limitations to drive the output until the inverting input reaches V_{in}
  - negative feedback makes it self-correcting
  - in this case, the op-amp drives (or pulls, if V_{in} is negative) a current through the load until the output equals V_{in}
  - so what we have here is a buffer: can apply V_{in} to a load without burdening the source of V_{in} with *any* current!

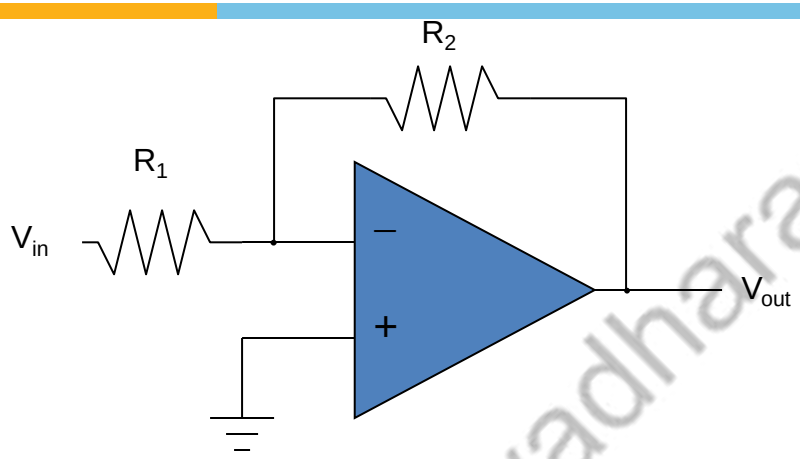


Important note: op-amp output terminal sources/sinks current at will: not like inputs that have no current flow

Op-Amp "Golden Rules"

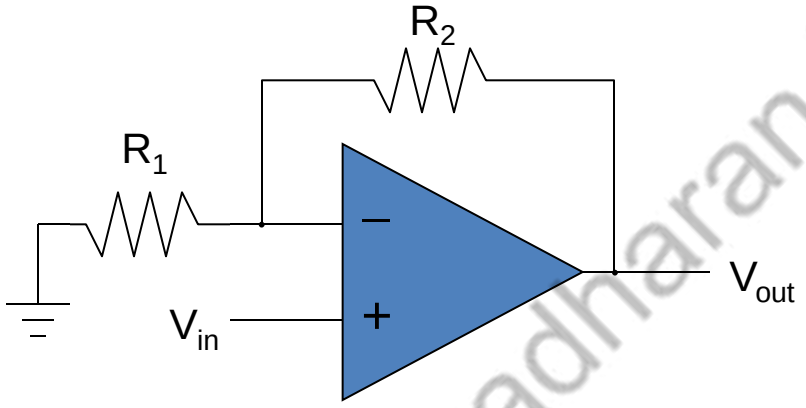
- When an op-amp is configured in *any* negative-feedback arrangement, it will obey the following two rules:
  - The inputs to the op-amp draw or source no current (true whether negative feedback or not)
  - The op-amp output will do whatever it can (within its limitations) to make the voltage difference between the two inputs zero

Inverting amplifier



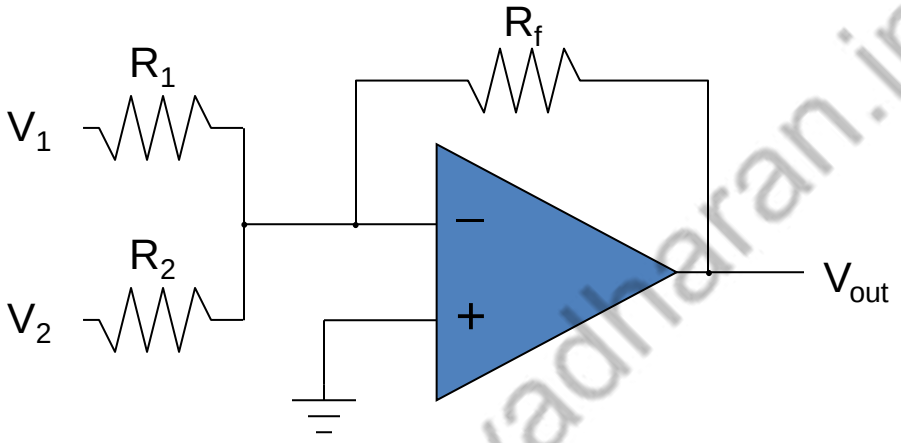
- Applying the rules: – terminal at "virtual ground"
  - so current through R_1 is $I_f = V_{in}/R_1$
- Current does not flow into op-amp (one of our rules)
  - so the current through R_1 must go through R_2
  - voltage drop across R_2 is then $I_f R_2 = V_{in} \times (R_2/R_1)$
- So $V_{out} = 0 - V_{in} \times (R_2/R_1) = -V_{in} \times (R_2/R_1)$
- Thus we amplify V_{in} by factor $-R_2/R_1$
  - negative sign earns title "inverting" amplifier
- Current is *drawn into* op-amp output terminal

Non-inverting Amplifier



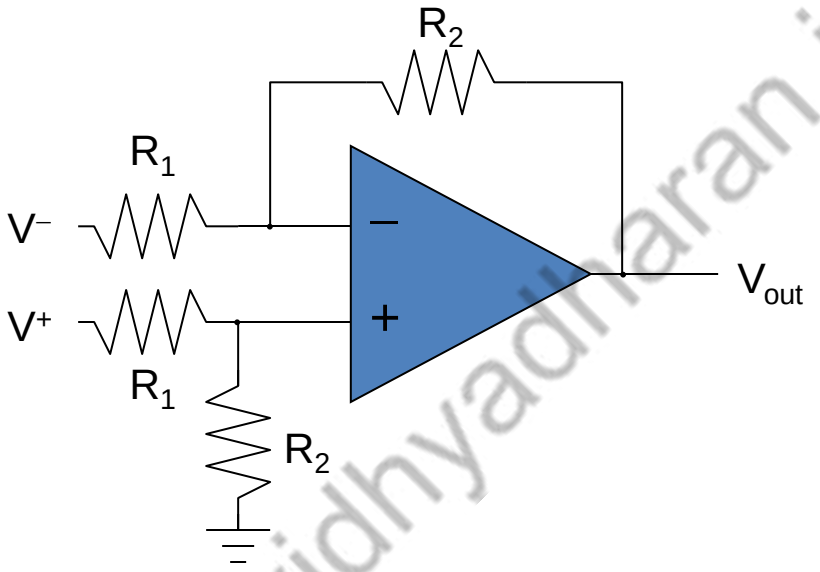
- Now neg. terminal held at V_{in}
  - so current through R_1 is $I_f = V_{in}/R_1$ (to left, into ground)
- This current cannot come from op-amp input
  - so comes through R_2 (delivered from op-amp output)
  - voltage drop across R_2 is $I_f R_2 = V_{in} \times (R_2/R_1)$
  - so that output is higher than neg. input terminal by $V_{in} \times (R_2/R_1)$
  - $V_{out} = V_{in} + V_{in} \times (R_2/R_1) = V_{in} \times (1 + R_2/R_1)$
  - thus gain is $(1 + R_2/R_1)$, and is positive
- Current is sourced from op-amp output in this example

Summing Amplifier



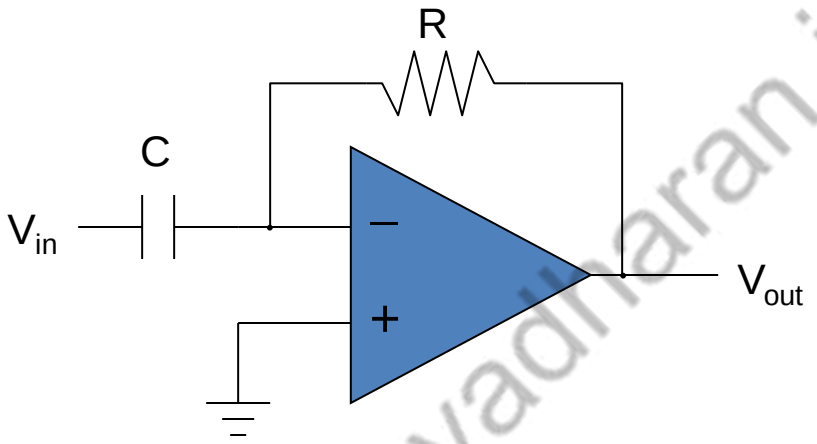
- Much like the inverting amplifier, but with two input voltages
  - inverting input still held at virtual ground
  - I_1 and I_2 are added together to run through R_f
  - so we get the (inverted) sum: $V_{out} = -R_f \times (V_1/R_1 + V_2/R_2)$
    - if $R_2 = R_1$, we get a sum proportional to $(V_1 + V_2)$
- Can have any number of summing inputs
  - we'll make our D/A converter this way

Differencing Amplifier



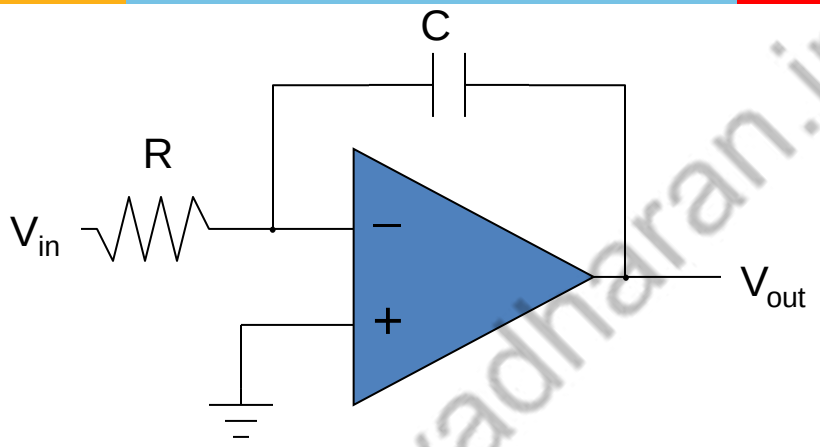
- The non-inverting input is a simple voltage divider:
  - $V_{node} = V^+R_2/(R_1 + R_2)$
- So $I_f = (V^- - V_{node})/R_1$
  - $V_{out} = V_{node} - I_fR_2 = V^+(1 + R_2/R_1)(R_2/(R_1 + R_2)) - V^-(R_2/R_1)$
  - so $V_{out} = (R_2/R_1)(V^+ - V^-)$
  - therefore we difference V^+ and V^-

Differentiator (high-pass)



- For a capacitor, $Q = CV$, so $I_{cap} = dQ/dt = C \cdot dV/dt$
  - Thus $V_{out} = -I_{cap}R = -RC \cdot dV/dt$
- So we have a differentiator, or high-pass filter
  - if signal is $V_0 \sin \omega t$, $V_{out} = -V_0 RC\omega \cos \omega t$
  - the ω-dependence means higher frequencies amplified more

Low-pass filter (integrator)



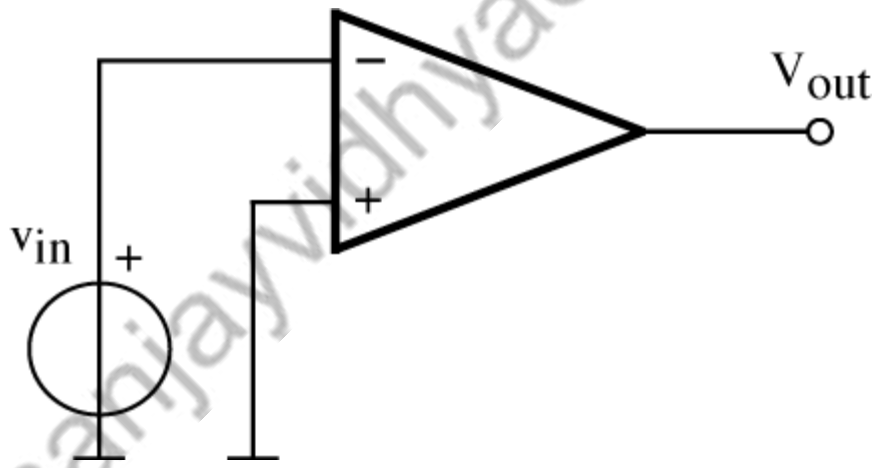
- $I_f = V_{in}/R$, so $C \cdot dV_{cap}/dt = V_{in}/R$
  - and since left side of capacitor is at virtual ground:

    $-dV_{out}/dt = V_{in}/RC$
  - so $$V_{out} = -\frac{1}{RC}\int V_{in}\,dt$$
  - and therefore we have an integrator (low pass)

Op-Amp Specifications

DC differential gain:

It is the open-loop voltage gain measured at DC with a small differential input signal. Typically Ad = 80 - 100 dB.

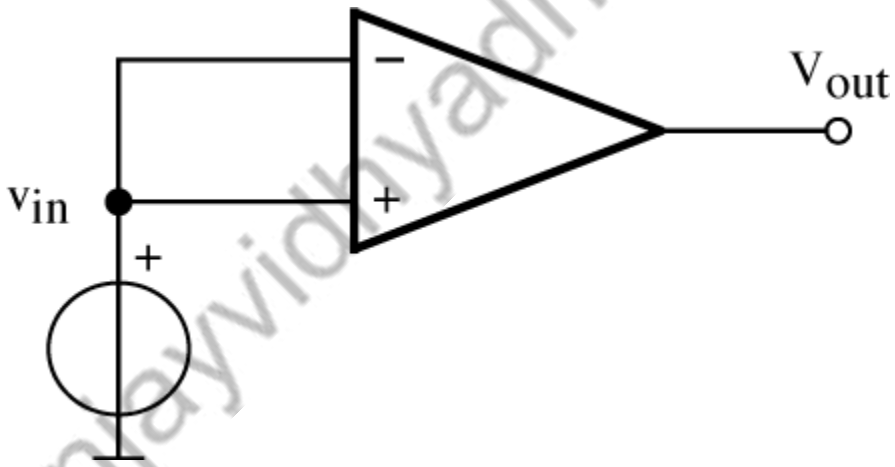


Analog Design for CMOS VLSI Systems
Franco Maloberti

Op-Amp Specifications

Common mode gain:

It is the open-loop voltage gain measured at DC with a small differential input signal. Typically Ad = 20 - 40 dB.



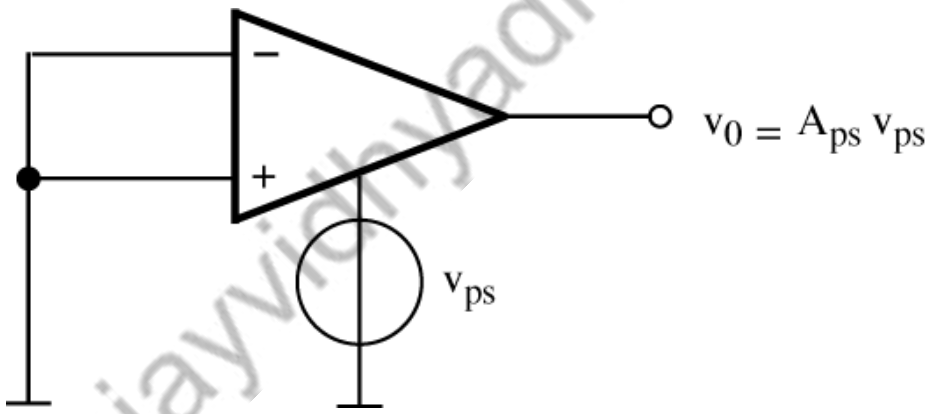
Common mode Rejection Ratio:

It is defined as the ratio between the differential gain and the common mode gain. Typically CMRR = 40 - 80 dB.

Op-Amp Specifications

Power supply rejection ratio:

If a small signal is applied in series with the positive (or negative) power supply, it is transferred to the output with a given gain A ps+ (or A ps-).
The ratios between differential gain and power supply gains furnish the two PSRRs.

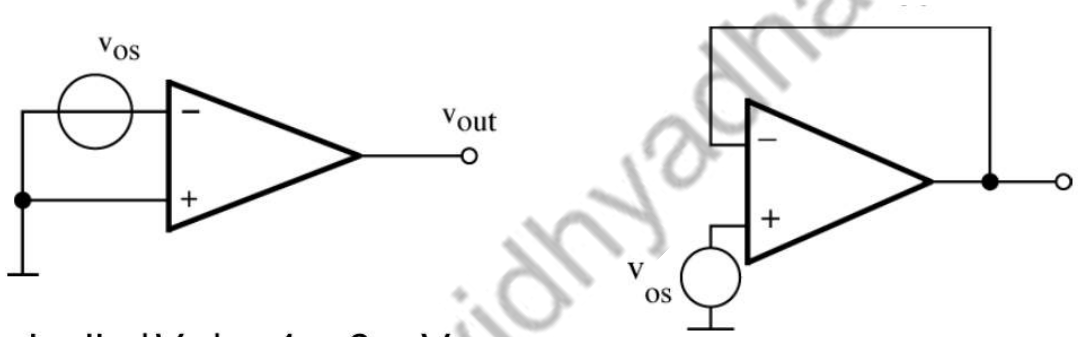


Typically: PSRR = 90 dB (DC)
PSRR = 60 dB (1 kHz)
PSRR = 30 dB (100 kHz)

Op-Amp Specifications

Input offset voltage:

In real circuits if the two input terminals are set at the same voltage the output saturates close to VDD or to VSS



Typically $|V_{os}| = 4 \div 6$ mV.

Input common mode range:

It is the maximum range of the common-mode input voltage which do not produce a significant variation of the differential gain.

Op-Amp Specifications

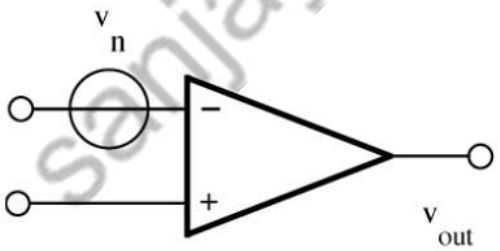
Output voltage swing:

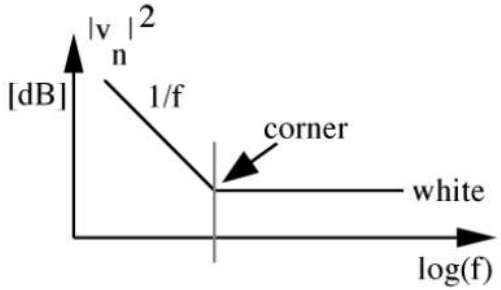
It is the swing of the output node without generating a defined amount of harmonic distortion.

Equivalent input noise:

The noise performances can be described in terms of an equivalent voltage source at the input of the op-amp.

Typically v_n = 40 - 50 nV/√Hz at 1 kHz,
in a wide band (1 MHz) it results 10 - 50 μV RMS.

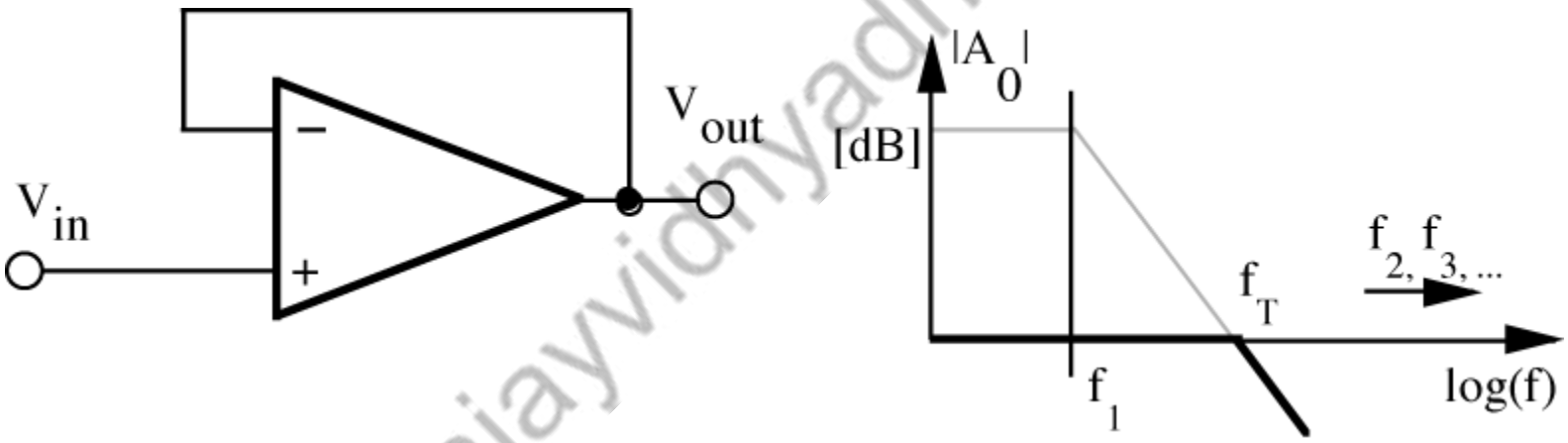




Op-Amp Specifications

Unity gain frequency:

It is the frequency where the open-loop gain is zero. It is also the -3 dB bandwidth in unity-gain closed loop conditions. Typically, f_T = 200 MHz.



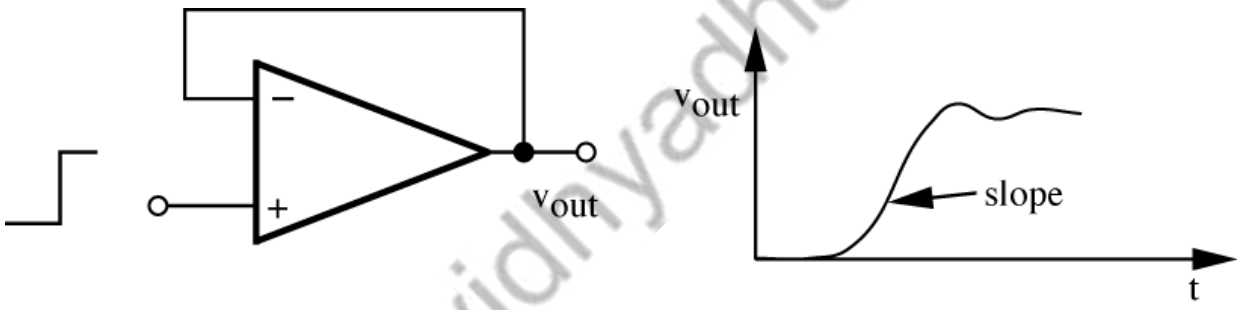
Phase margin:

It is the phase shift of the small-signal differential gain measured at the unity gain frequency. A phase margin smaller than 60° causes ringing in the output response.

Op-Amp Specifications

Slew rate:

It is the maximum slope of the output voltage. Usually it is measured in the buffer configuration. The positive slew rate can be different from the negative slew rate. Typically SR = 50 - 200 V/µs (lower values for micropower operation).



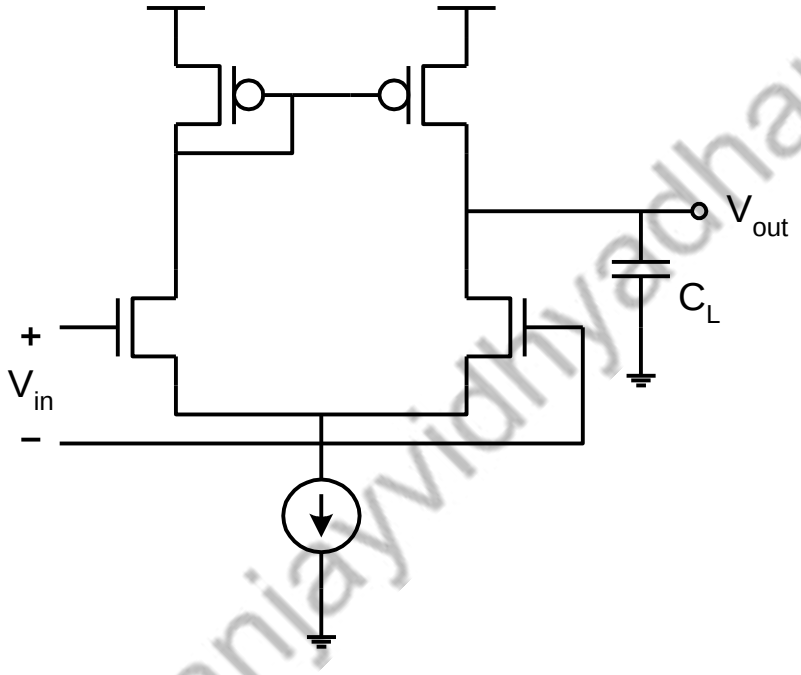
Settling time:

The settling time is the time required to settle the output within a given range (usually ± 0.1%) of the final value.

Power dissipation:

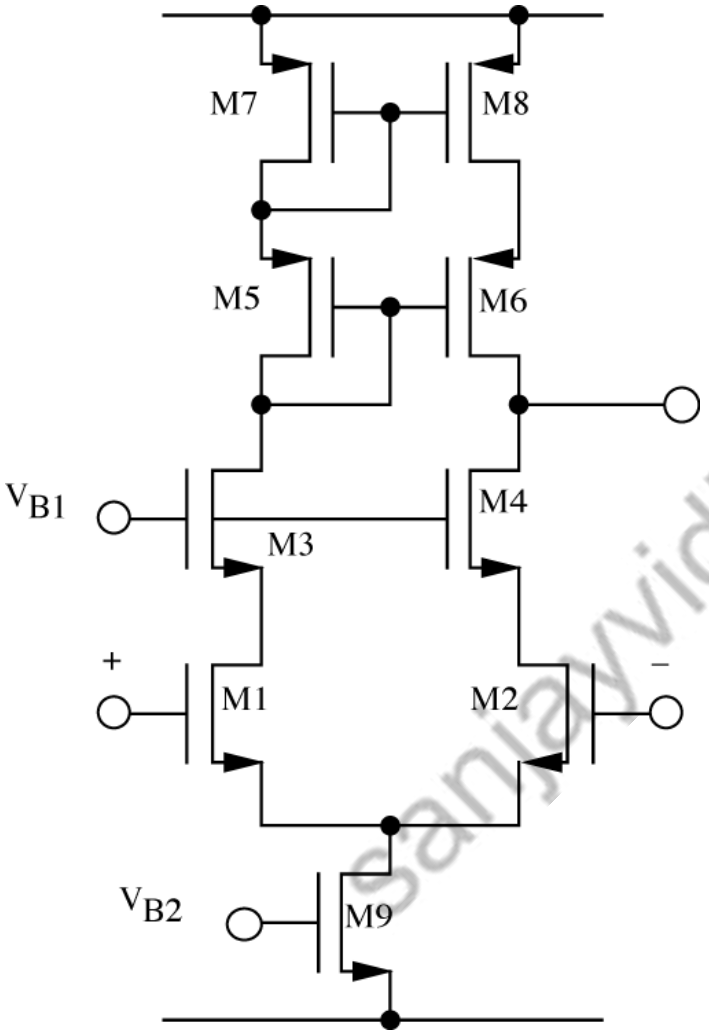
It depends on speed and bandwidth requirements.
Typically, for 1.8 V supply, it is around 600 µW.

Single Stage Op-Amp



$g_{mN}(r_{oN}||r_{oP})$.

Single Stage Cascoded Amplifier



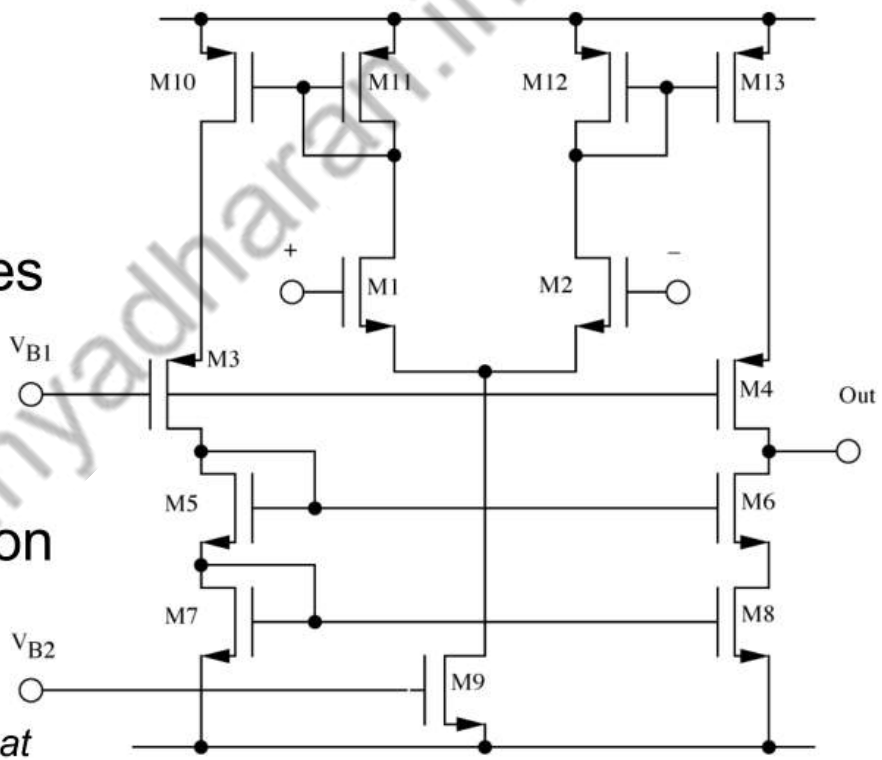
Telescopic cascode

- DC gain $A_0 \approx (g_m r_{ds})^2$
- low power consumption
- only one high impedance node: compensated with a capacitance load (if necessary)
- low output swing
- reference of the input close to the negative supply
- two bias lines (V_{B1}, V_{B2})
- 5 transistors in series

Single Stage Cascoded Amplifier

Mirrored cascode

- optimum input common mode range
- only 4 transistors in series
- improved output swing
- speed of the mirror
- higher power consumption



$$V_{outmax} = V_{B1max} + V_{GS4} - V_{sat}$$

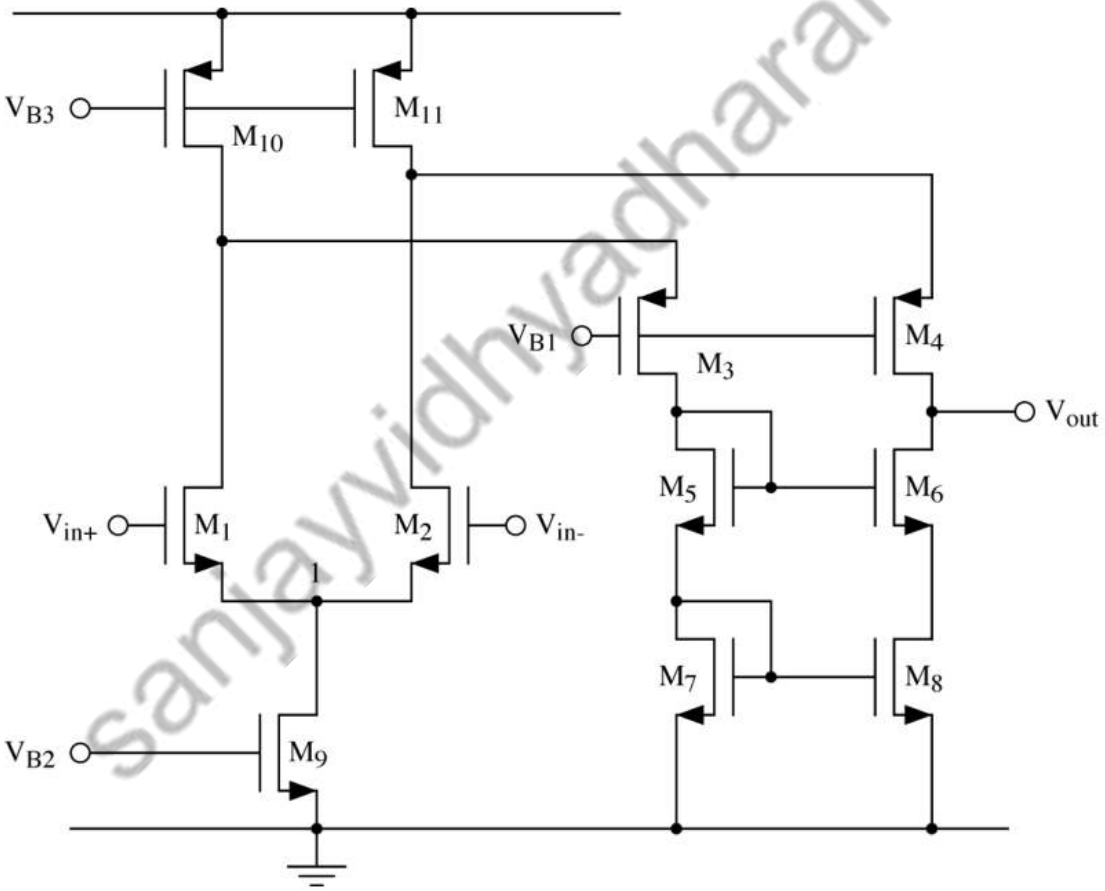
$$V_{B1max} = V_{DD} - V_{sat} - V_{GS4}$$

$$V_{outmax} = V_{DD} - 2V_{sat}$$

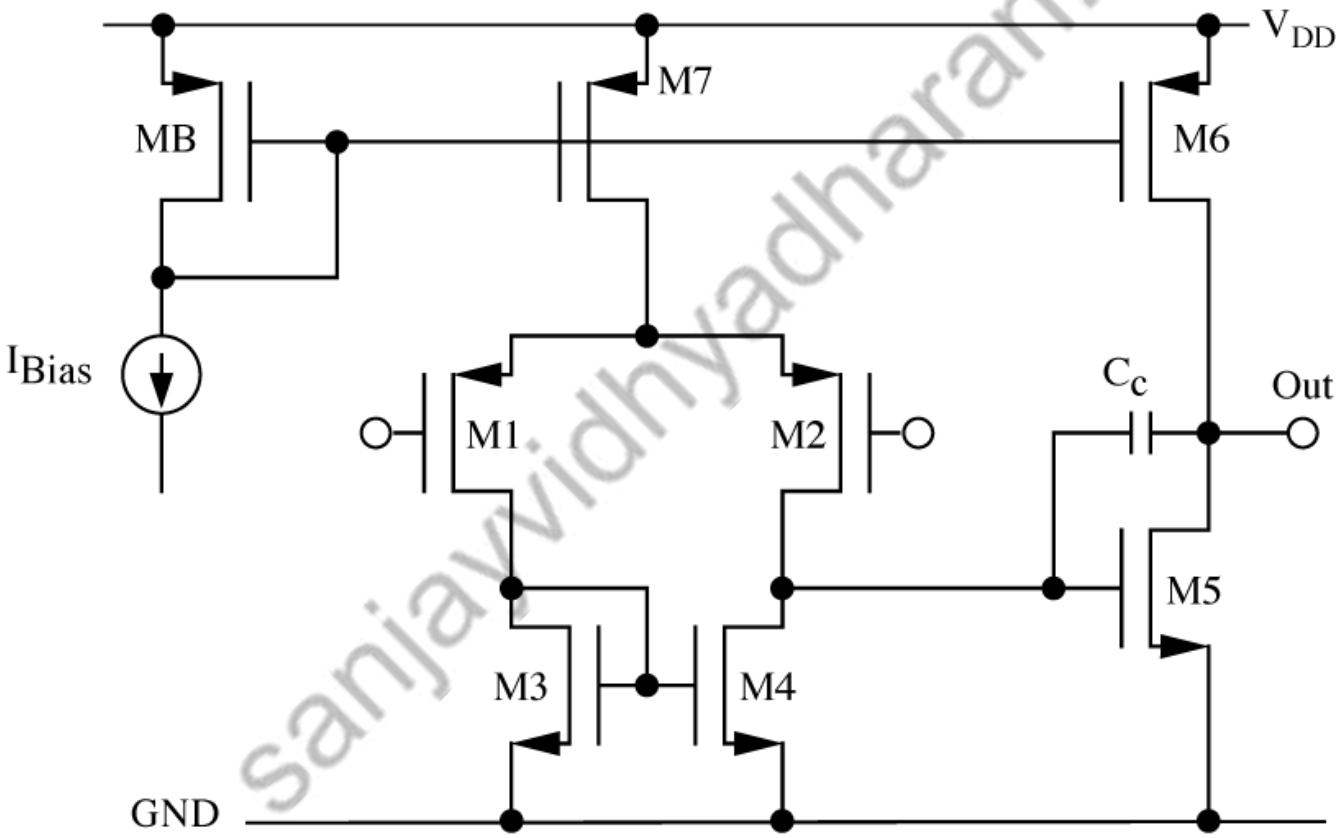
$$V_{outmax} = V_{GS7} + V_{sat}$$

Single Stage Cascoded Amplifier

Conventional folded cascode



Two-stage op-amp



Two-stage op-amp

Open-loop differential gain:

The gain is obtained by multiplying the gains of the two stages.

$$A_v = A_1 A_2 = \frac{g_{m1}}{(g_{ds2} + g_{ds4})} \frac{g_{m5}}{(g_{ds5} + g_{ds6})} =$$

$$= \frac{2\sqrt{2\mu_n \mu_p} C_{ox}}{(\lambda_n + \lambda_p)^2} \frac{\sqrt{\left(\frac{W}{L}\right)_1}\sqrt{\left(\frac{W}{L}\right)_5}\left(\frac{W}{L}\right)_B}{\sqrt{\left(\frac{W}{L}\right)_6}\sqrt{\left(\frac{W}{L}\right)_7}} \frac{1}{I_{Bias}}$$

At low frequency the gain is inversely proportional to the bias current.

$$\frac{1}{r_{eq}} = \frac{1}{r_1} + \frac{1}{r_2}$$

$$\frac{1}{r_{eq}} = g_{ds1} + g_{ds2}$$

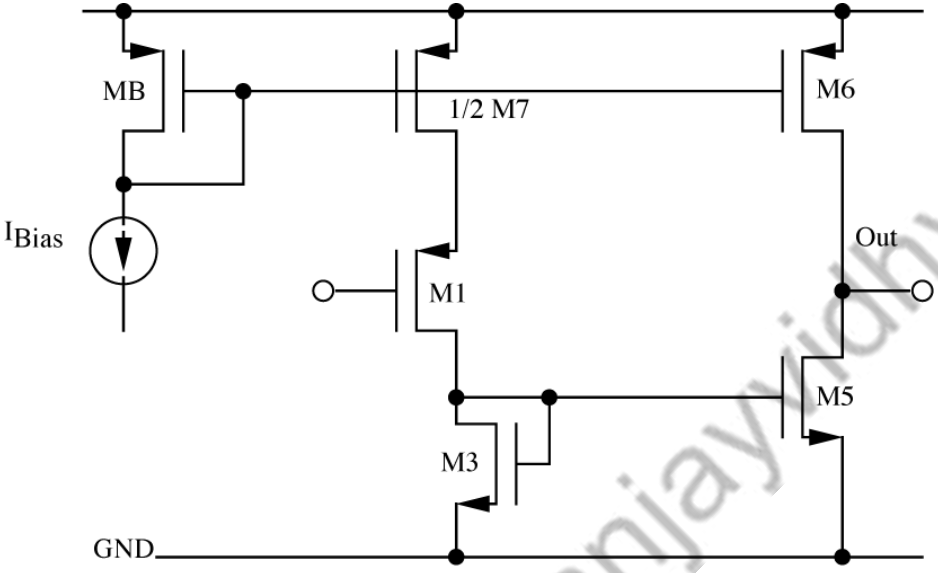
$$r_{eq} = \frac{1}{g_{ds1} + g_{ds2}}$$

$$g_m = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right) I_D}$$

$$r_o \approx \frac{1}{\lambda I_D}$$

Two-stage op-amp

Applying the same signal to both inputs the circuit becomes symmetrical and can be studied considering half circuit.

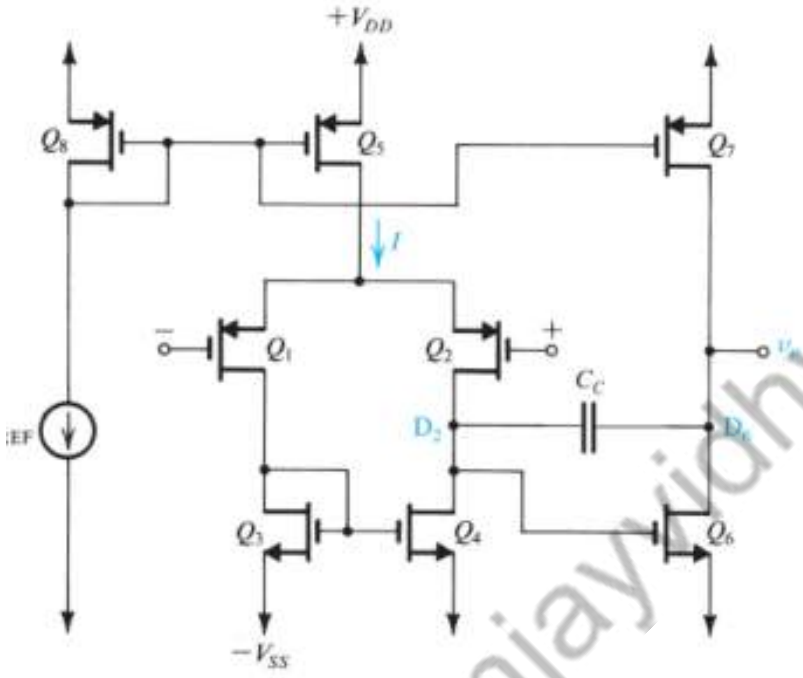


$$A_v = A_1 A_2 = \frac{g_{m1}}{(g_{ds2} + g_{ds4})} \frac{g_{m5}}{(g_{ds5} + g_{ds6})}$$

$$A_{CM} = A_{CM1} A_{CM2} = \left(\frac{-g_{ds7}}{2g_{m3}} \right) \left(\frac{-g_{m5}}{g_{ds5} + g_{ds6}} \right)$$

$$CMRR = \frac{A_v}{A_{CM}} = \frac{2g_{m1} g_{m3}}{g_{ds7}(g_{ds2} + g_{ds4})}$$

Example of Two-stage op-amp



	Q1	Q2	Q3	Q4
W/L in um	20/0.8	20/0.8	5/0.8	5/0.8

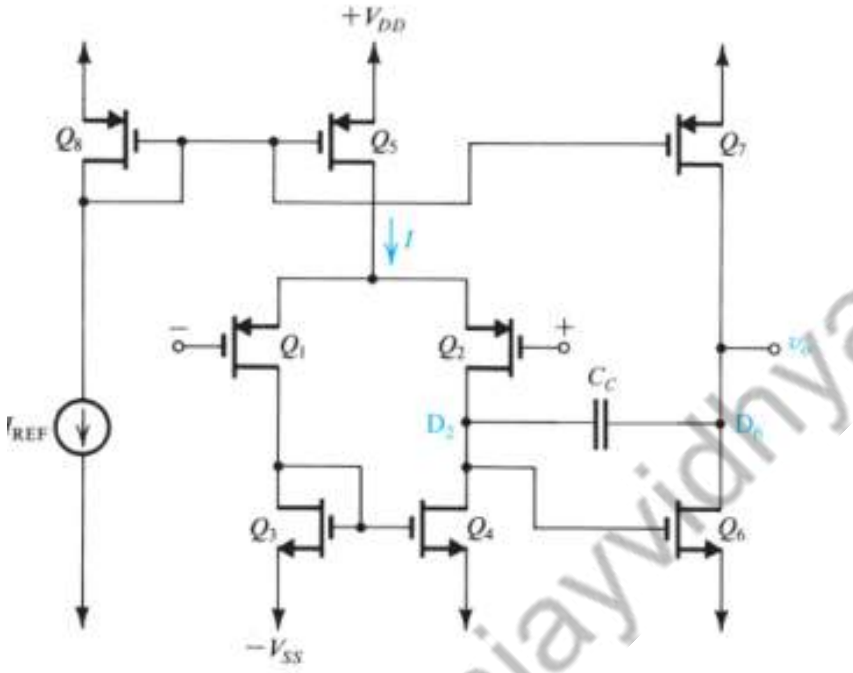
	Q5	Q6	Q7	Q8
W/L in um	40/0.8	10/0.8	4/0.8	4/0.8

I_{REF} = 90 µA, V_{tn} = 0.7V, V_{tp} = -0.8V
$\mu_n C_{ox}$ = 160 µA/V², $\mu_p C_{ox}$ = 40 µA/V²
$|V_A|$ = 10V for all devices
$V_{DD} = V_{SS}$ = 2.5V

Find I_D, $|V_{OV}|$, $|V_{GS}|$, g_m, r_o for all Q's,
voltage gain,
input common mode range,
output voltage range.

Example of Two-stage op-amp

Solution: DC Parameters



$$I_{REF} = 90\mu A$$

$$I_{D5} = \frac{(W/L)_5}{(W/L)_8} = 90\mu A$$

$$I_{D7} = \frac{(W/L)_7}{(W/L)_8} = 90\mu A$$

$$I_{D1} = I_{D2} = I_{D3} = I_{D4} = \frac{I_{D5}}{2} = 45\mu A$$

$$I_{Di} = \frac{1}{2}\mu_i C_{ox}\left(\frac{W}{L}\right)|V_{OV}|^2$$

$$|V_{OV1}| = |V_{OV2}| = |V_{OV3}| = |V_{OV4}| = 0.3$$

$$|V_{OV5}| = |V_{OV6}| = |V_{OV7}| = |V_{OV8}| = 0.3$$

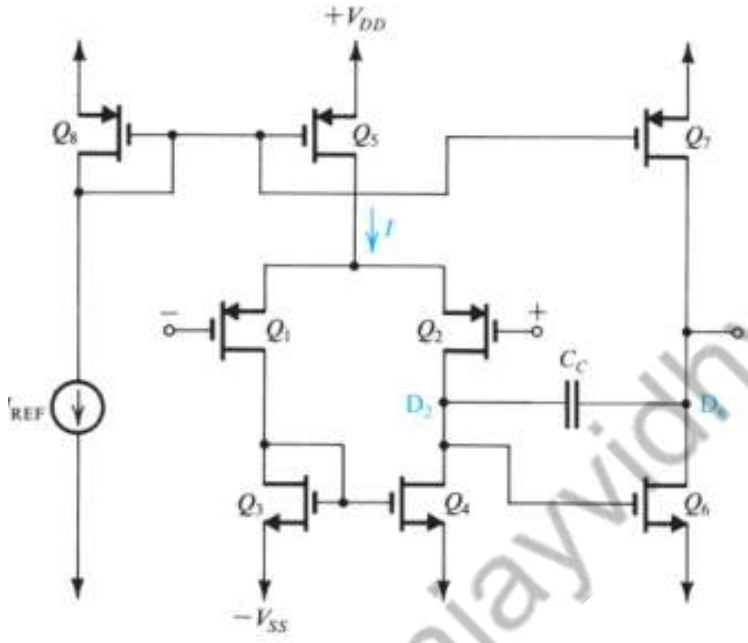
$$|V_{GS}| = |V_{OV}| + |V_t|$$

$$\text{NMOS}: |V_{GS}| = 0.3 + 0.7 = 1.0V$$

$$\text{PMOS}: |V_{GS}| = 0.3 + 0.8 = 1.1V$$

Example of Two-stage op-amp

Solution: AC Parameters



$$g_m = \frac{2I_D}{|V_{OV}|}$$

$$g_{m1-4} = 2 \times 45\mu A / 0.3V = 0.3mA / V$$

$$g_{m5-8} = 2 \times 90\mu A / 0.3V = 0.6mA / V$$

$$r_o = \frac{|V_A|}{I_D}$$

$$r_{o1-4} = \frac{10V}{45\mu A} = 222k\Omega$$

$$r_{o5-8} = \frac{10V}{90\mu A} = 111k\Omega$$

$$A_1 = -g_{m1}\left(r_{o2} \parallel r_{o4}\right)$$

$$= -0.3 \times 222 / 2 = -33.3V / V$$

$$A_2 = -g_{m6}\left(r_{o6} \parallel r_{o7}\right)$$

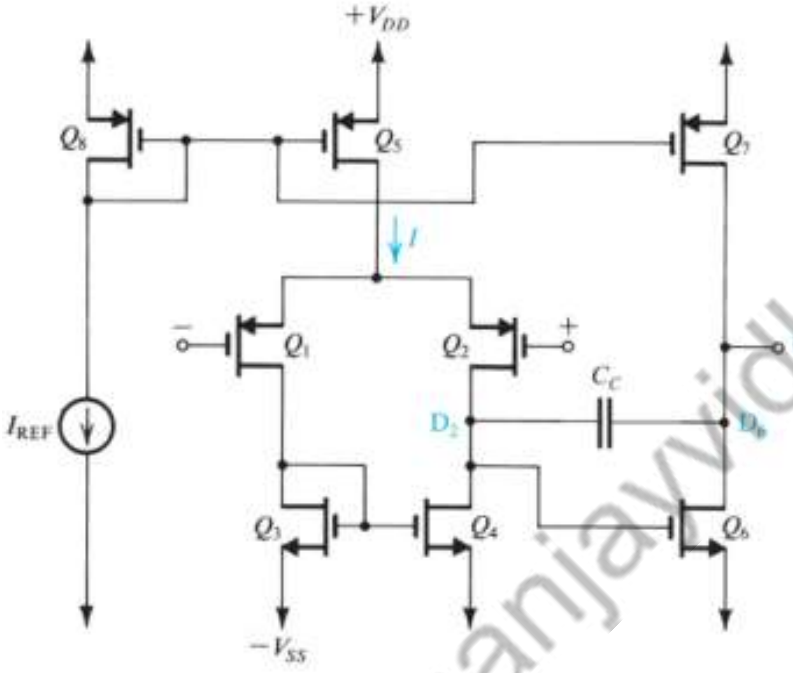
$$= -0.6 \times 111 / 2 = -33.3V / V$$

$$A_o = A_1 A_2 = 1109V / V$$

$$= 20\log(1109) = 61dB$$

Example of Two-stage op-amp

Solution: Input Common-Mode Ranges



Input common-mode voltage range:

Maximum: Q_5 near edge of saturation

$$|V_{DS5}| = |V_{OV5}| = 0.3V$$

$$v_{icm\max} = 2.5 - |V_{OV5}| - |V_{GS5}|$$

$$= 2.5 - 0.3 - 1.1 = 1.1V$$

Minimum: Q_1 near edge of saturation

$$v_{D1} = -V_{SS} + V_{GS3} = -2.5 + 1 = -1.5V$$

$$|v_{DS1}| = |v_{GS1}| - |v_{tp}|$$

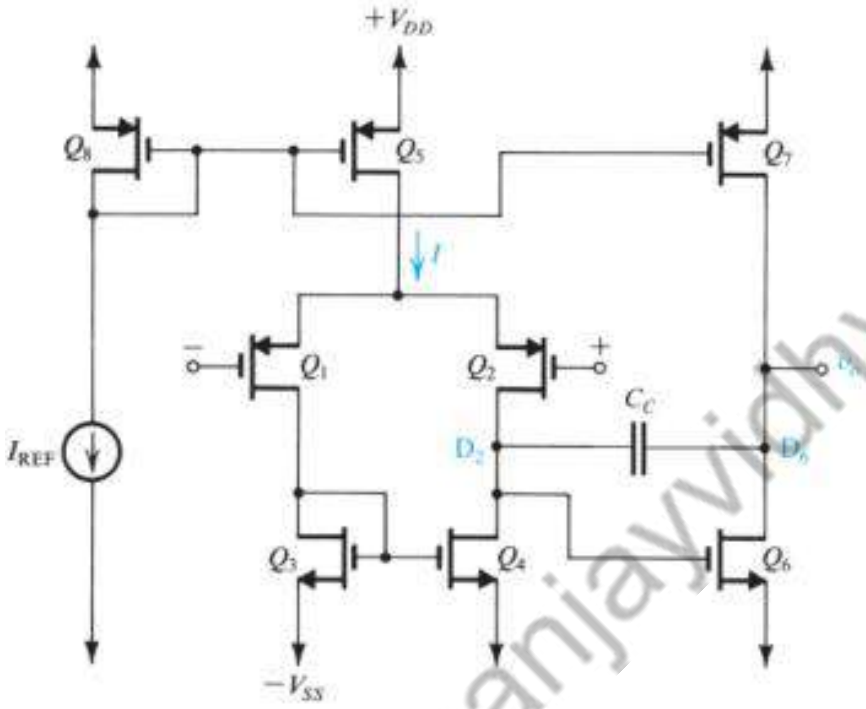
$$-v_{DS1} = -v_{GS1} - 0.8$$

$$-v_{D1} = -v_{G1} - 0.8$$

$$v_{icm\min} = v_{G1} = v_{D1} - 0.8 = -2.3V$$

Example of Two-stage op-amp

Solution: Output Ranges



Output voltage range:

Maximum: Q_7 near edge of saturation

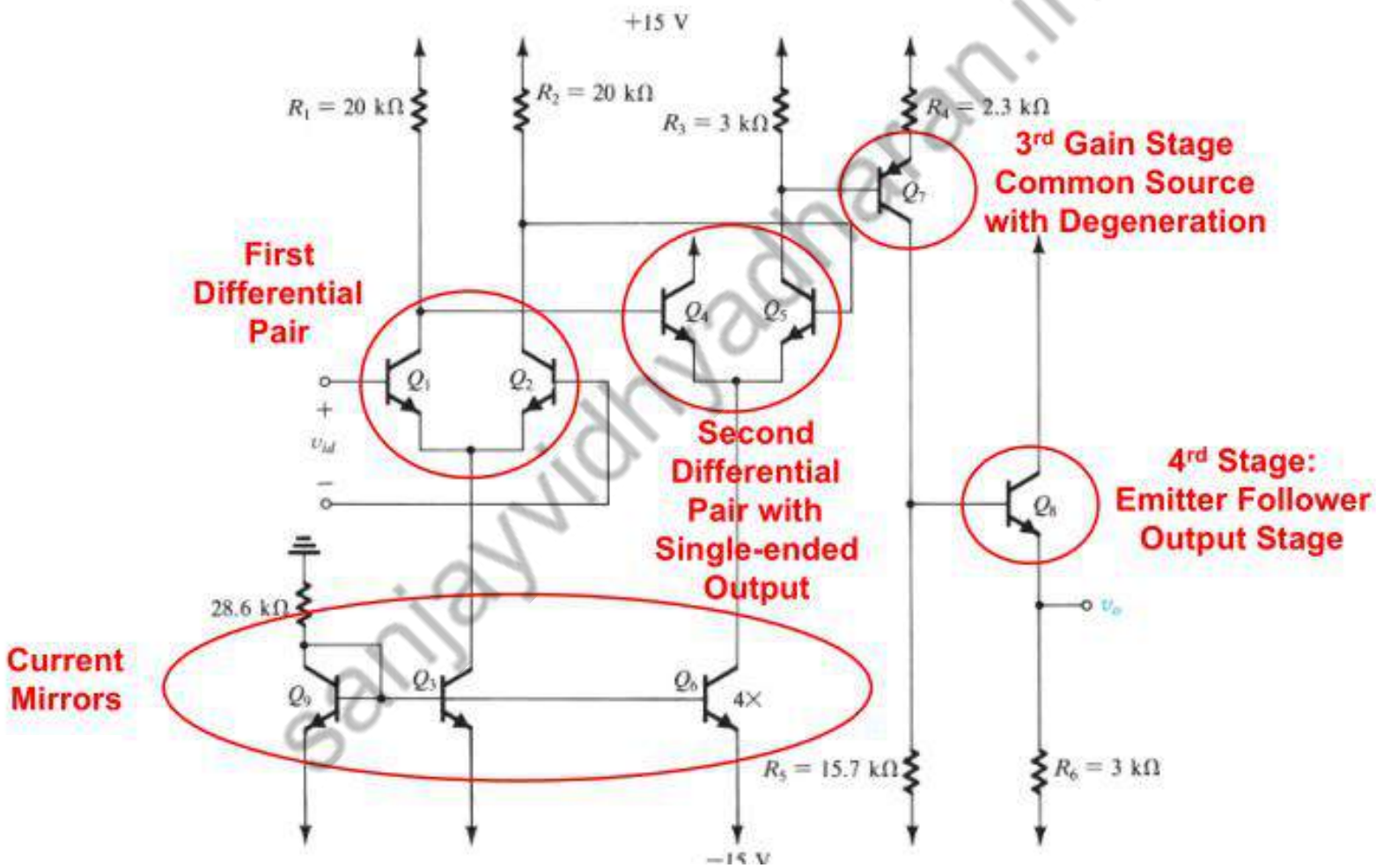
$$|V_{OV7}| = 0.3V$$

$$v_{o\max} = 2.5 - |V_{OV7}| = 2.2V$$

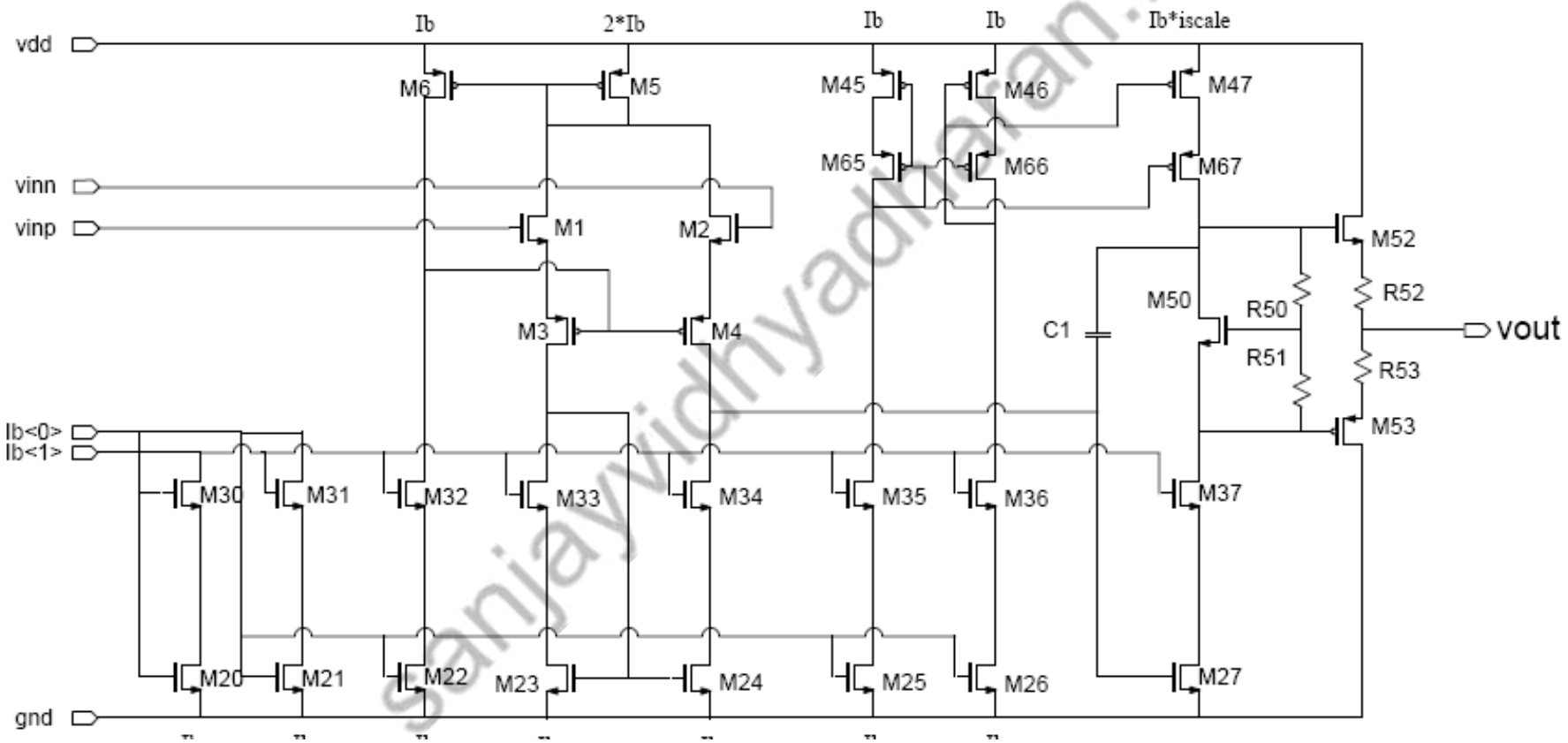
Minimum: Q_6 near edge of saturation

$$v_{o\min} = -V_{SS} + |V_{OV6}| = -2.5 + 0.3 = -2.2V$$

A Four-Stage Bipolar Op-Amp



CMOS Implementation of 741 Op-Amp



Thankyou