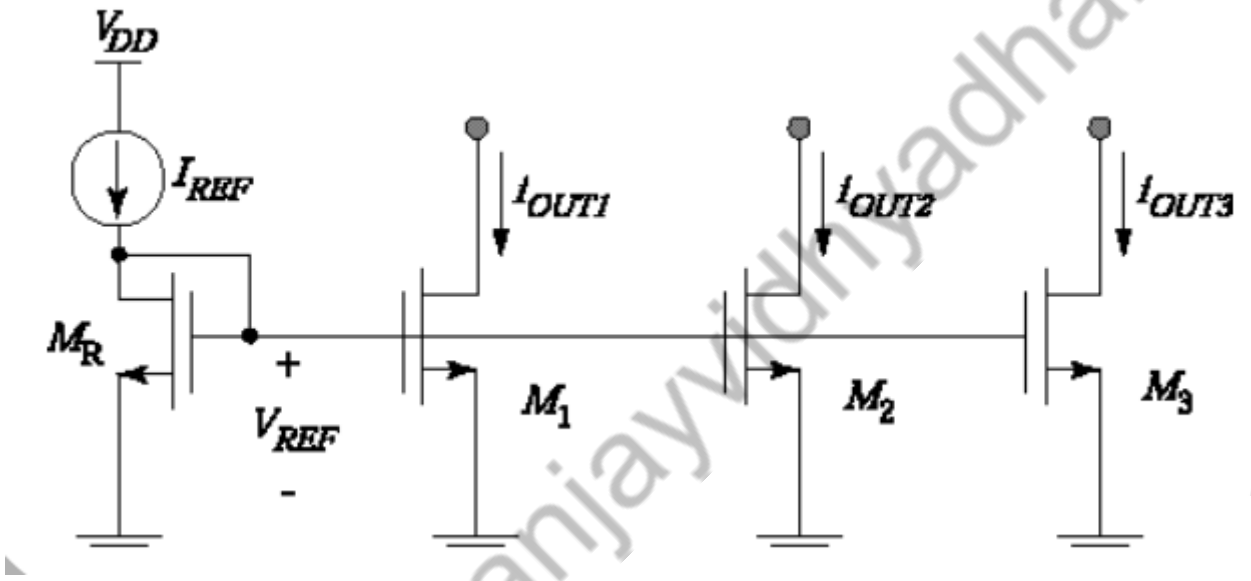
Analog IC Design : 2022-23
Lecture 8
DC Voltage and DC Current Sources
Part-2

By Dr. Sanjay Vidhyadharan

Current Mirrors

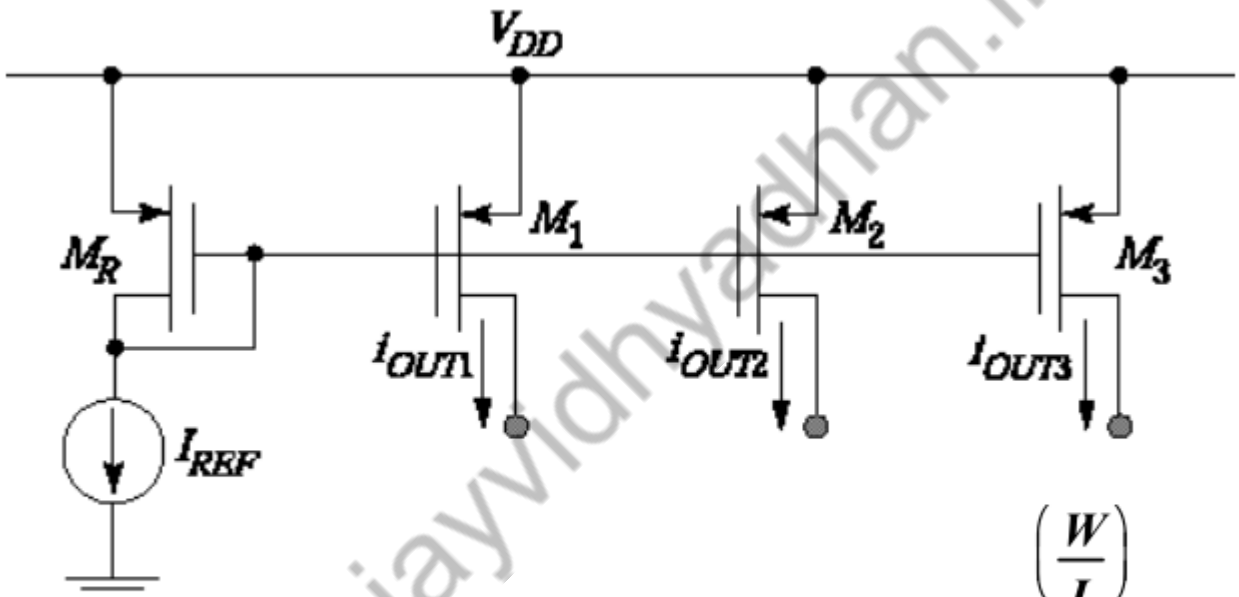
NMOS Current Mirror



$$I_{OUTn} = I_{REF} \frac{\left(\frac{W}{L}\right)_n}{\left(\frac{W}{L}\right)_R}$$

Current Mirrors

PMOS Current Mirror



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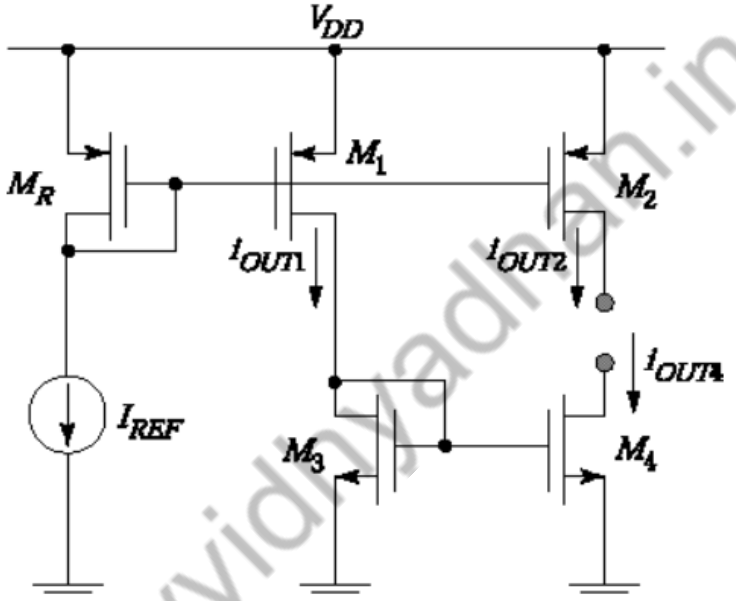
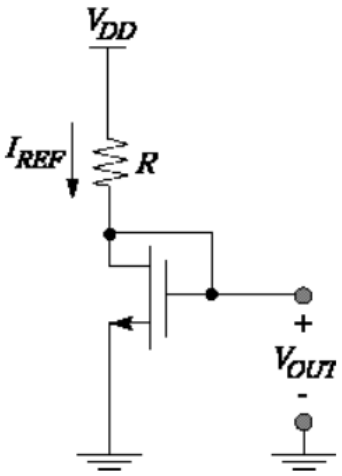
Current Mirrors



$$I_{OUT1} = I_{REF}\frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_R} \qquad I_{OUT2} = I_{REF}\frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_R}$$

$$I_{OUT4} = I_{OUT1}\frac{\left(\frac{W}{L}\right)_4}{\left(\frac{W}{L}\right)_3} = I_{REF}\frac{\left(\frac{W}{L}\right)_4\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_3\left(\frac{W}{L}\right)_R}$$

Generating I_{REF}



$$I_{REF} = \frac{V_{DD} - V_{OUT}}{R}$$

$$V_{OUT} = V_{Tn} + \sqrt{\frac{I_{REF}}{\frac{W}{2L}\mu_n C_{ox}}}$$

For large W/L: $$I_{REF} \approx \frac{V_{DD} - V_{Tn}}{R}$$

Advantages
– I_{REF} set by value of resistor
• Disadvantages
– V_{DD} also affects I_{REF} .
– V_{Tn} and R are functions of temperature
In the real world, more sophisticated circuits are used to generate I_{REF} that are V_{DD} and T independent.

Influence of the Channel Modulation Parameter λ

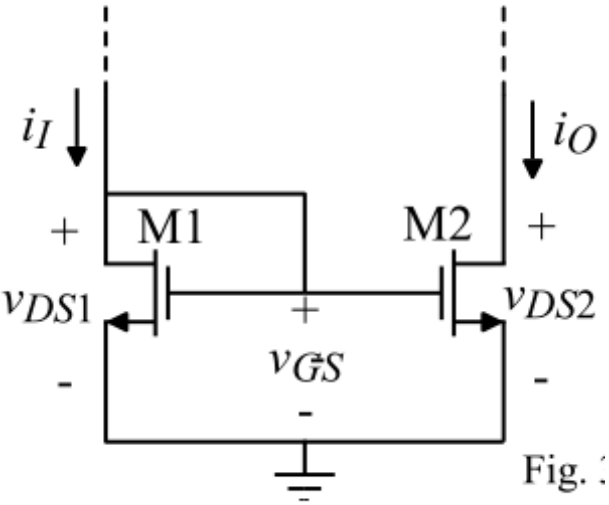


Fig. 1

Assume that $v_{DS2} > v_{GS} - V_{T2}$, then

$$\frac{i_O}{i_I} = \left(\frac{L_1 W_2}{W_1 L_2}\right)\left(\frac{V_{GS}-V_{T2}}{V_{GS}-V_{T1}}\right)^2\left[\frac{1+\lambda v_{DS2}}{1+\lambda v_{DS1}}\left(\frac{K_2'}{K_1'}\right)\right]$$

If the transistors are matched, then $K_1' = K_2'$ and $V_{T1} = V_{T2}$

$$\frac{i_O}{i_I} = \left(\frac{L_1 W_2}{W_1 L_2}\right)\left(\frac{1+\lambda v_{DS2}}{1+\lambda v_{DS1}}\right)$$

If $v_{DS1} = v_{DS2}$, then

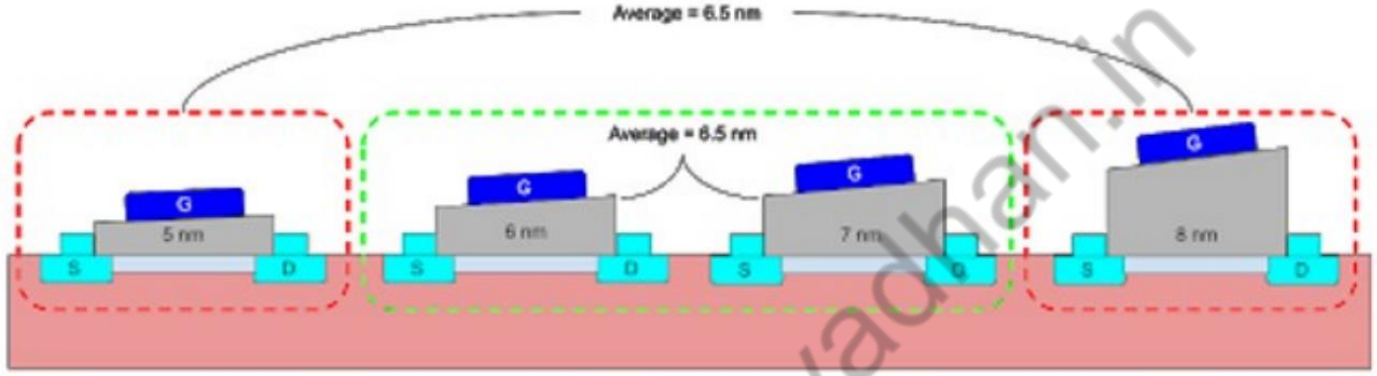
$$\frac{i_O}{i_I} = \left(\frac{L_1 W_2}{W_1 L_2}\right)$$

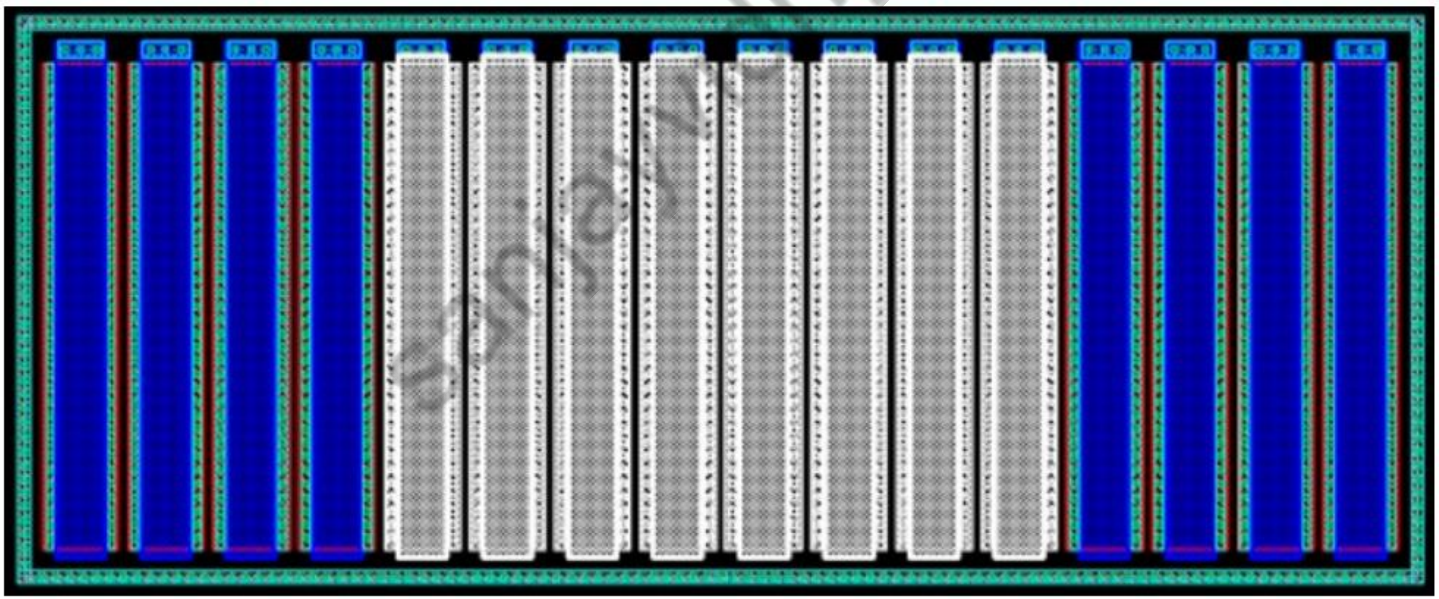
Therefore the sources of error are:

1.) $v_{DS1} \neq v_{DS2}$

2.) M1 and M2 are not matched.

Common centroid design evens out the effect of the process variation.





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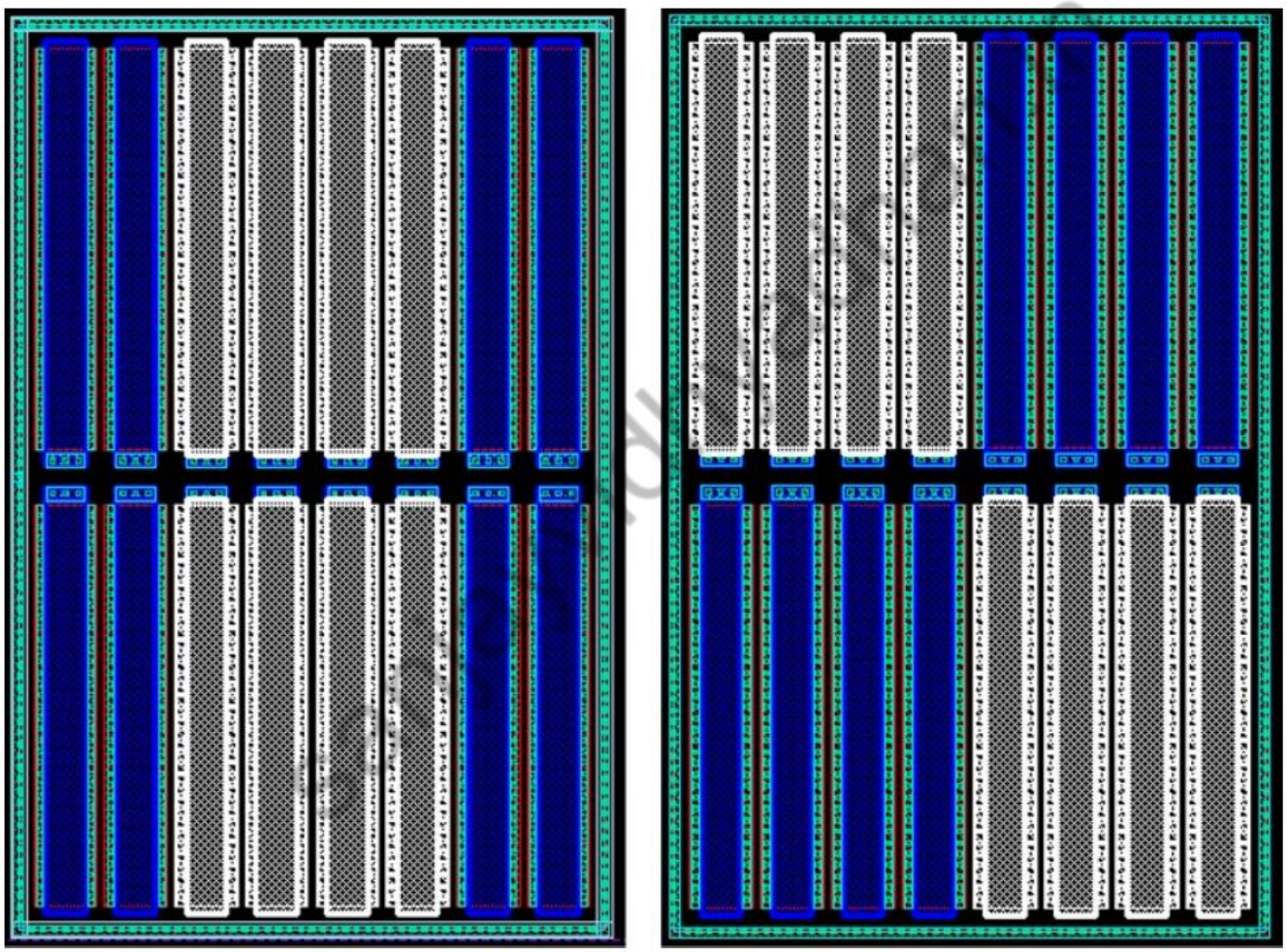
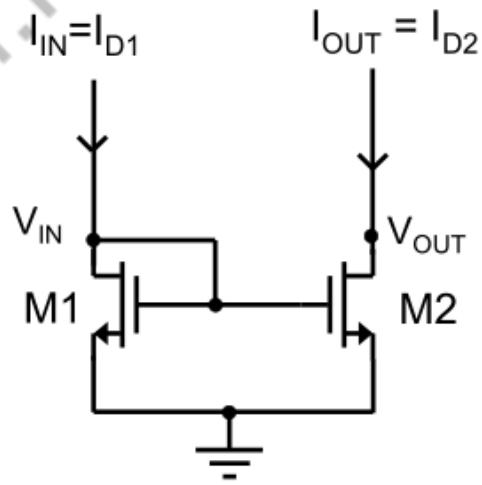


Current Mirror Analysis

- As $V_{GS1} = V_{GS2}$ and assuming matched $V_{TH1} = V_{TH2}$

$$\frac{I_{OUT}}{I_{IN}} = \frac{\left(W/L\right)_2 (1+\lambda V_{OUT})}{\left(W/L\right)_1 (1+\lambda V_{IN})}$$



- The output resistance of current source is the output resistance of M2

$$R_O = \frac{1}{\lambda I_{D2}} = \frac{1}{\lambda I_{OUT}}$$

- Normally, larger L is used so that λ effect is reduced and the output resistance is higher.
- The current gain systematic error is:

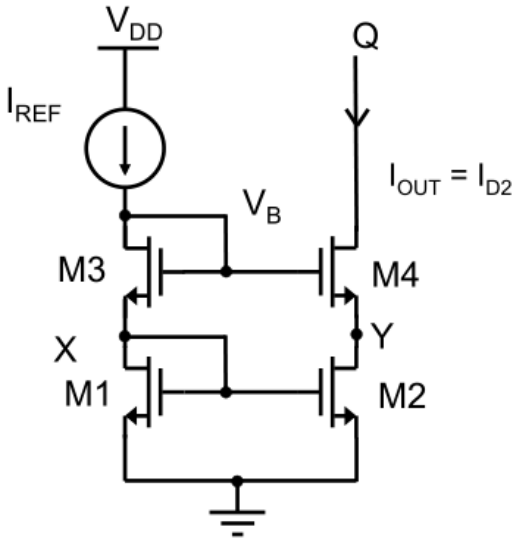
$$I_{OUT\_ideal} = \frac{(W/L)_2}{(W/L)_1} I_{IN}$$

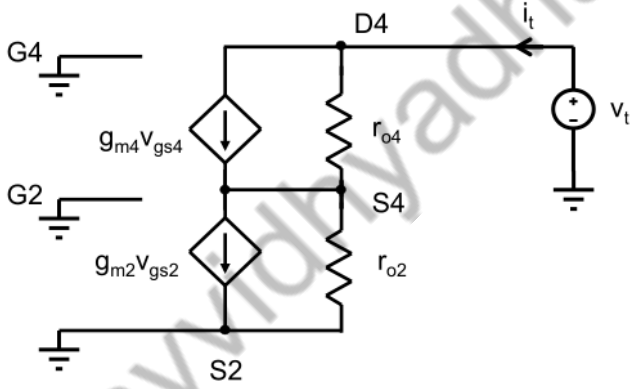
$$E = \frac{I_{OUT} - I_{OUT\_ideal}}{I_{OUT\_ideal}} = \frac{(1+\lambda V_{OUT})}{(1+\lambda V_{IN})} - 1 = \frac{\lambda}{(1+\lambda V_{IN})}(V_{OUT} - V_{IN}) \approx \lambda (V_{OUT} - V_{IN})$$

Systematic error

Standard Cascode Current Mirror

Output Resistance





$v_{gs2}=0,\ v_{gs4} = -\ i_t\ r_{o2}$

$$i_t = \frac{v_t - v_{s4}}{r_{o4}} - g_{m4} i_t r_{o2}$$

$$i_t(1 + g_{m4} r_{o2}) = \frac{v_t - i_t r_{o2}}{r_{o4}}$$

$$R_O = \frac{v_t}{i_t} = r_{o4}(1 + g_{m4} r_{o2}) + r_{o2}$$

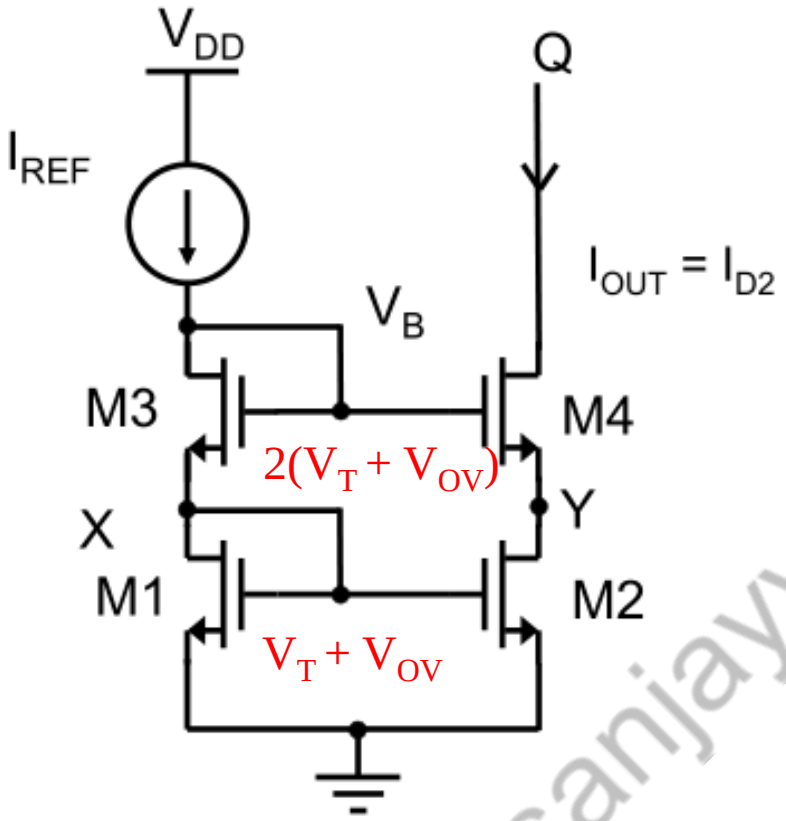
$$R_O = g_{m4} r_{o2}^2$$

If body effect is included: $R_O = (g_{m4} + g_{mb}) r_{o2}^2$

Features of Cascode current mirror:

- No current gain systematic error.
- Higher output resistance.
- Higher minimum output voltage.

Standard Cascode Current Mirror



Note V_{OV} of M1 and M2 will equal

$V_Y = V_T + V_{OV}$

All 4 MOSFETs have the same V_{TH} if body effect is ignored.

$V_X = V_Y = V_{TH} + V_{OV}$

$V_{GS3} = V_{OV} + V_{TH}$ as M1 and M3 carry the same "I"

$V_{G3} = V_{GS3} + V_X = 2V_{TH} + 2V_{OV}$ ignoring body effect.

$V_{G4} = 2V_{TH} + 2V_{OV}$

This should also be the case with body effect – only $2V_{TH}$ will become $V_{TH1} + V_{TH3}$.

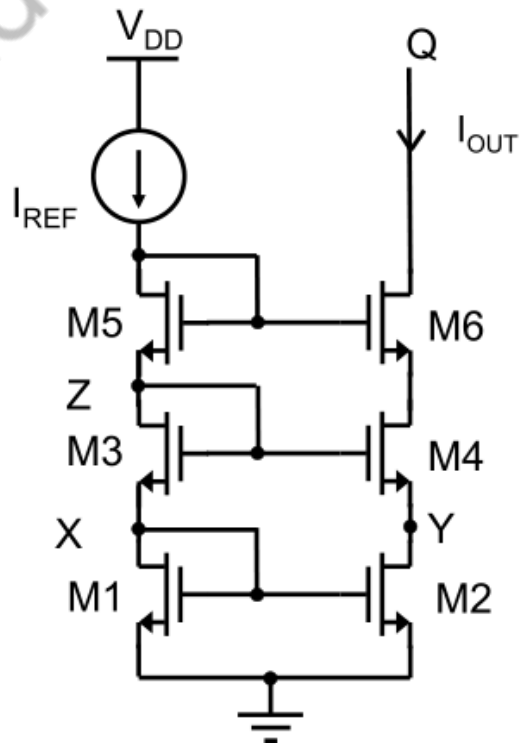
Min Vout $= V_X + V_{OV} = V_{TH} + 2V_{OV}$

No Systematic error

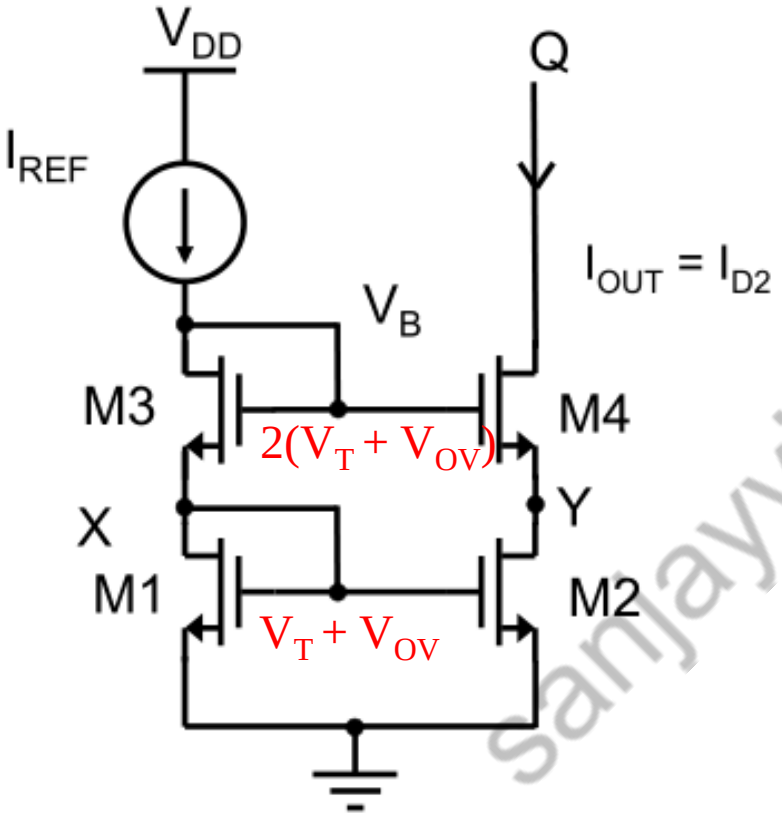
Triple Cascode Current Mirror

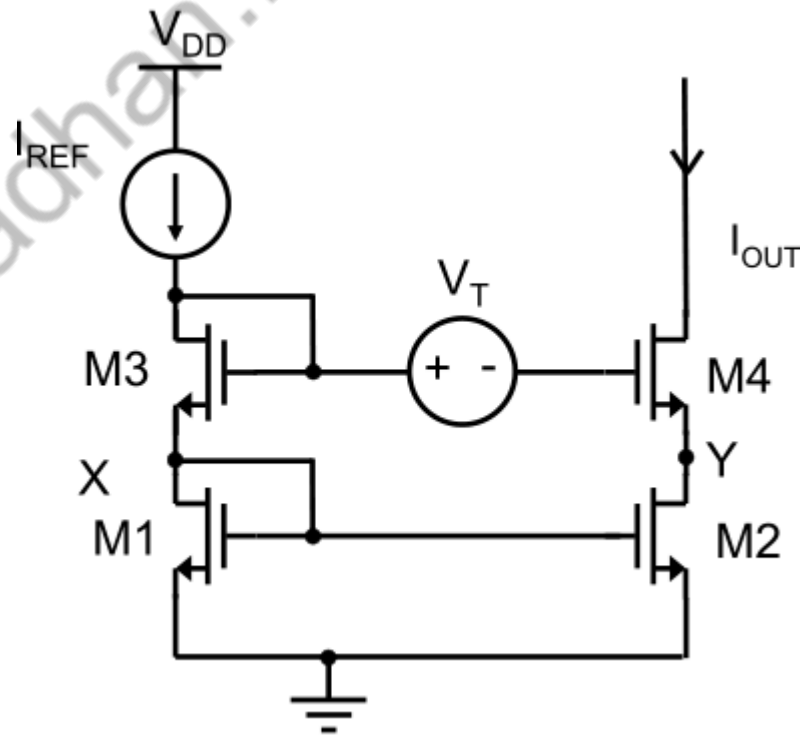
A variation of this circuit known as triple Cascode current mirror where a device is added on the left and right is also possible. R_O in this case will be

$$R_O = r_{o6}\{1 + g_{m6}[r_{o4}(1 + g_{m4}r_{o2}) + r_{o2}]\} + r_{o4}(1 + g_{m4}r_{o2}) + r_{o2}$$
$$= g_{m6}g_{m4}r_o^3$$
$$\approx r_o(g_m r_o)^2$$



Low Voltage Cascode Current Source 1





Low Voltage Cascode Current Source 1

All transistors have the same overdrive except M3. $V_X=V_{TH}+V_{OD}$

Since W3=1/4W1, $I_{REF}=\frac{1}{2}\mu C_{OX}\frac{1}{4}\left(\frac{W}{L}\right)(V_{GS3}-V_{TH})^2=\frac{1}{2}\mu C_{OX}\left(\frac{W}{L}\right)V_{OD}^2$

$V_{GS3}=V_{TH}+2V_{OD} \rightarrow V_{G3}=V_X+V_{GS3}=2V_{TH}+3V_{OD}$

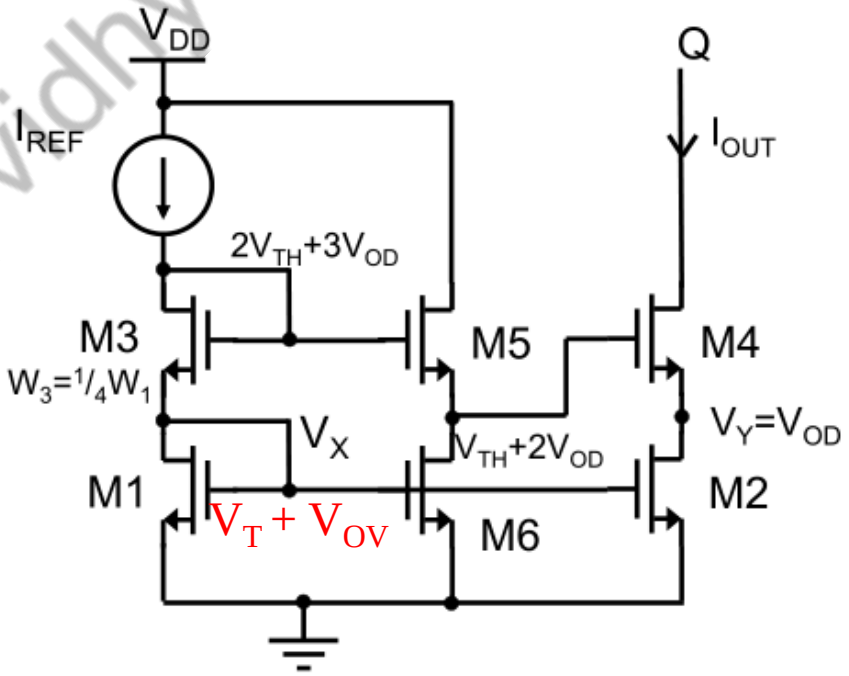
$V_{G4}=V_{TH}+2V_{OD} \rightarrow$

$V_Y=V_{OD}$

$V_{Omin}=2V_{OD}$

1. The output resistance remains the same as the Cascode current mirror.
2. $E \approx \lambda(V_Y-V_X)=-\lambda V_{TH}$

Gain systematic error is not zero



Low Voltage Cascode Current Source 2

All the transistors have the same overdrive. Set $V_B=V_{TH}+2V_{OD}$

$V_X=V_Y=V_B-(V_{TH}+V_{OD})=V_{OD}$

Then the minimum output voltage is:

$V_{OUT}=2V_{OD}$

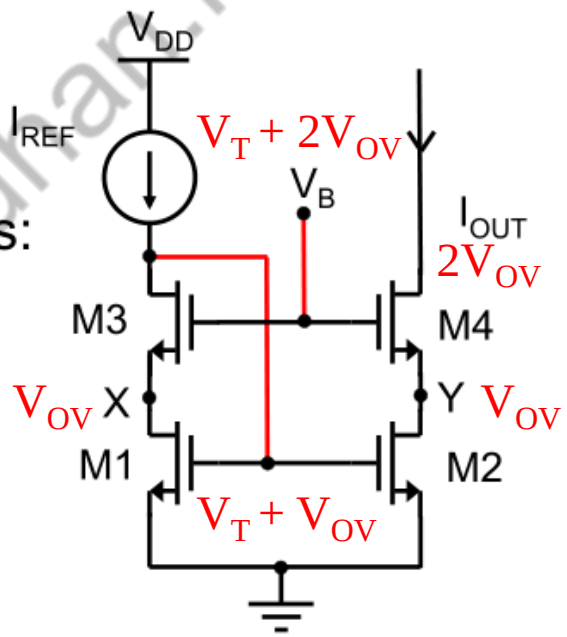
And since $V_X=V_Y$ →

no current gain systematic error.

Design all transistors' overdrive smaller than its V_{TH}.

Since $V_{DS3}=V_{GS1}-V_{DS1}=V_{TH}>V_{OD}$ → M3 at saturation region.

All transistors are at saturation region.

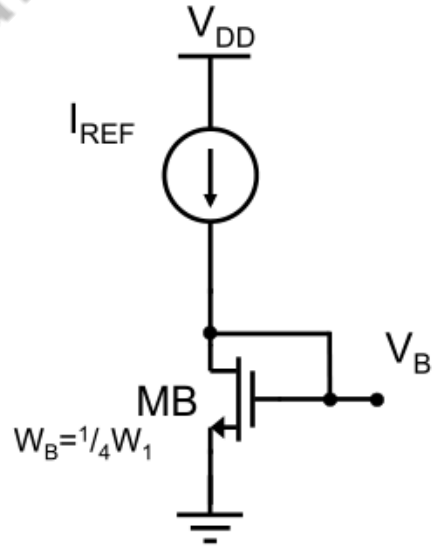


Low Voltage Cascode Current Source 2

- The low voltage cascade current source 2 has:
  - High output resistance
  - Low output voltage: $V_{OUT}=2V_{OD}$
  - No current gain systematic error.
- How to generate $V_B=V_{TH}+2V_{OD}$?
- Two ways:
  - Assuming same L for all transistors,
  - Since $W_B=1/4W_1$ and same current

$$I_{REF}=\frac{1}{2}\mu C_{OX}\frac{1}{4}\left(\frac{W}{L}\right)(V_B-V_{TH})^2=\frac{1}{2}\mu C_{OX}\left(\frac{W}{L}\right)V_{OD}^2$$

  - $V_B=V_{GS1}=V_{TH}+2V_{OD}$



Low Voltage Cascode Current Source 2

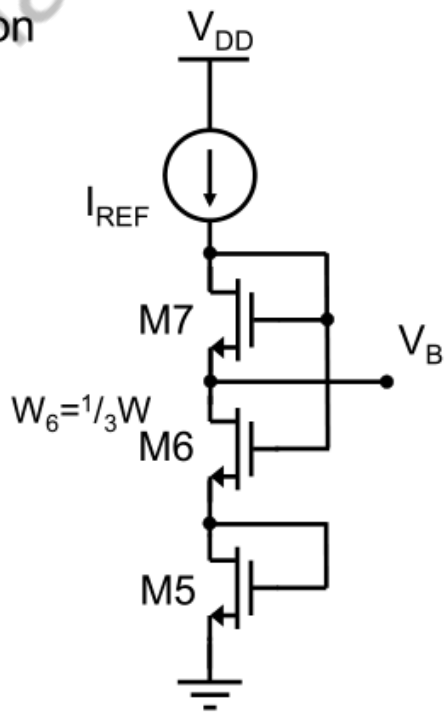
- Another way to generate V_B:
- All transistor have the same overdrive except M6.
- $V_{DS6}=V_{GS6}-V_{GS7} \rightarrow V_{GS6}=V_{DS6}+V_{GS7}$
- Since $V_{GS7}>V_{TH}$, $V_{DS6}<V_{GS6}-V_{TH} \rightarrow$ linear region
- $V_{GS6}-V_{TH}=V_{DS6}+V_{GS7}-V_{TH}=V_{DS6}+V_{OD}$

$$I_{D6}=\frac{1}{3}\frac{W}{L}\mu C_{OX}\left[(V_{GS6}-V_{TH})\cdot V_{DS6}-\frac{1}{2}V_{DS6}^2\right]$$

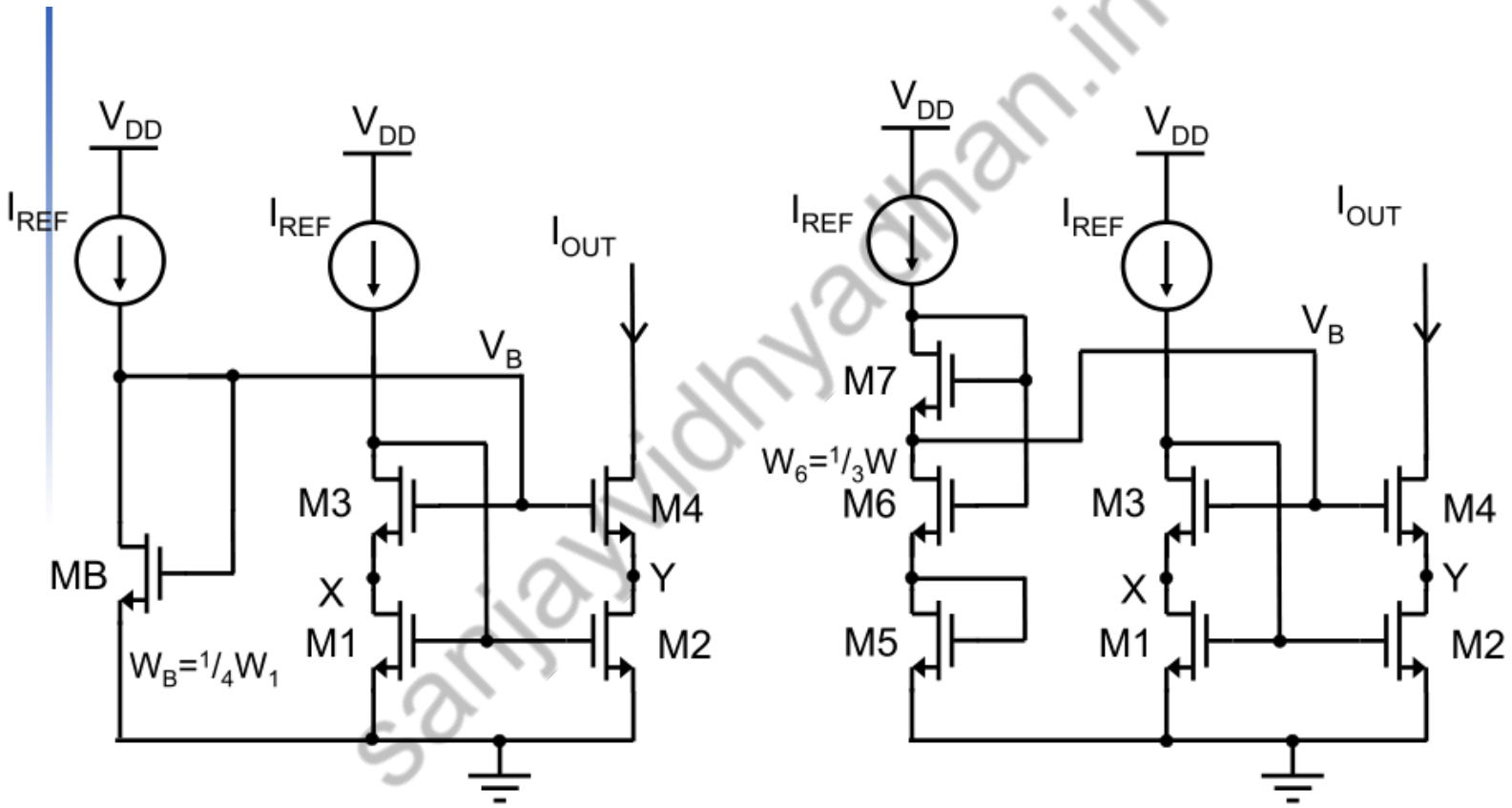
$$I_{D7}=\frac{1}{2}\frac{W}{L}\mu C_{OX}V_{OD}^2$$

$$I_{D6}=I_{D7} \qquad and \qquad V_{GS6}-V_{TH}=V_{DS6}+V_{OD}$$

- Solve the equations: $V_{DS6}=V_{OD}$
- $V_B=V_{GS5}+V_{DS6}=V_{TH}+2V_{OD}$



Low Voltage Cascode Current Source 2



Full schematic of two types of low voltage Cascode current mirror 2.

No Systematic error

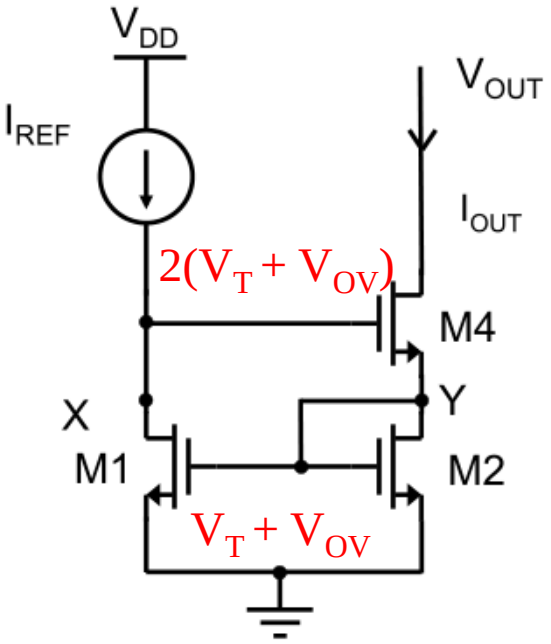
Wilson Current Mirror

- Transistor M1 and M2 have the same overdrive:

$$\frac{I_{OUT}}{I_{IN}} = \frac{\left(W/L\right)_2 (1+\lambda V_Y)}{\left(W/L\right)_1 (1+\lambda V_X)}$$

- Use feedback to stabilize the output current.
- $V_{OUT}\uparrow \rightarrow I_{OUT}\uparrow \rightarrow V_Y\uparrow \rightarrow V_X\downarrow \rightarrow I_{OUT}\downarrow$
- High output resistance: $g_m r_o^2$
- Minimum output voltage: $V_{TH}+2V_{OD}$
- Since $V_X \neq V_Y$, the current gain systematic error is not zero.

$$E \approx \lambda(V_Y - V_X)$$



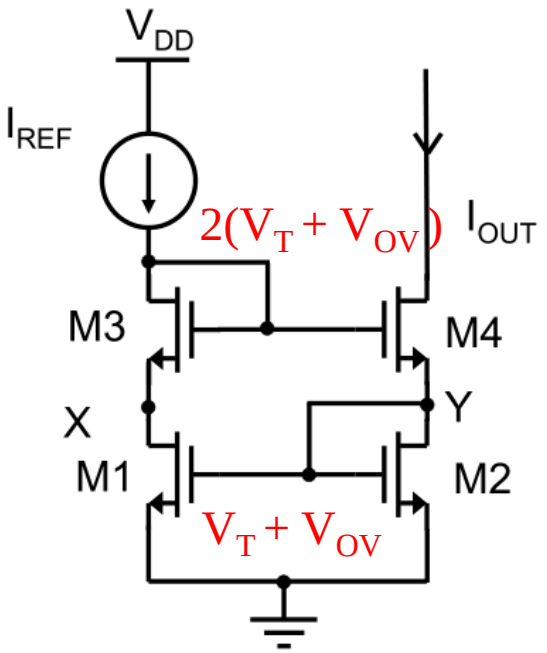
Wilson Current Mirror

By adding M3, V_X=V_Y, the current gain systematic error is zero.

High output resistance: $g_m r_o^2$

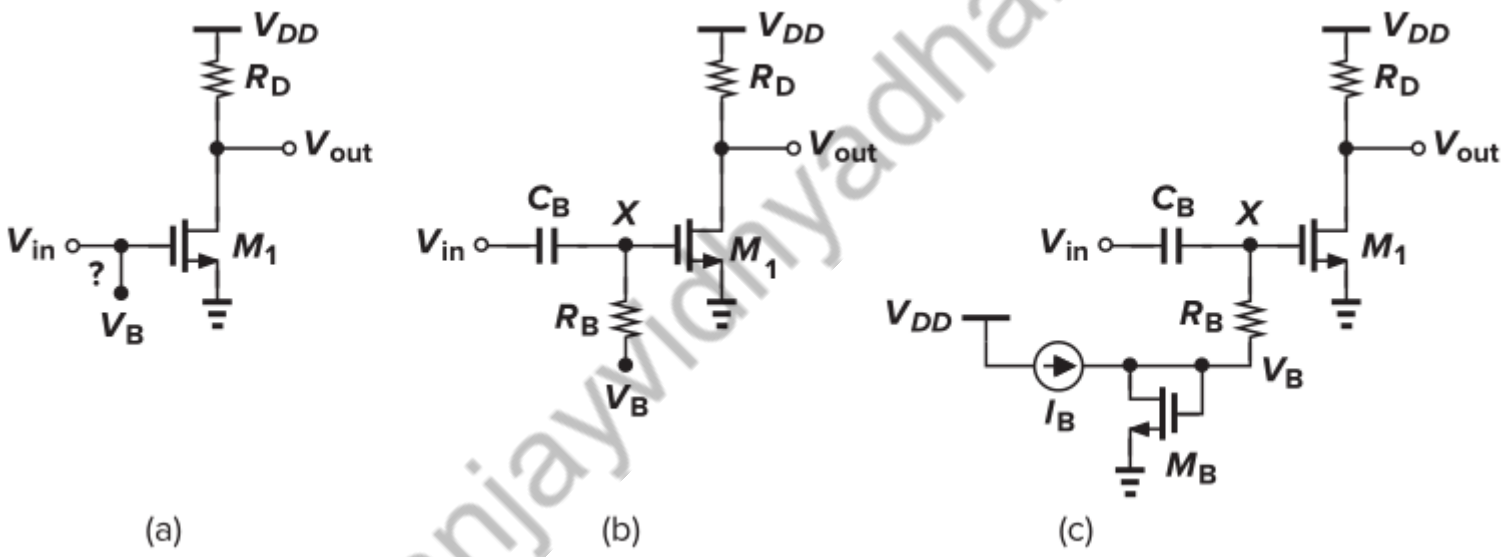
Minimum output voltage: $V_{TH}+2V_{OD}$

Not good for low-voltage design

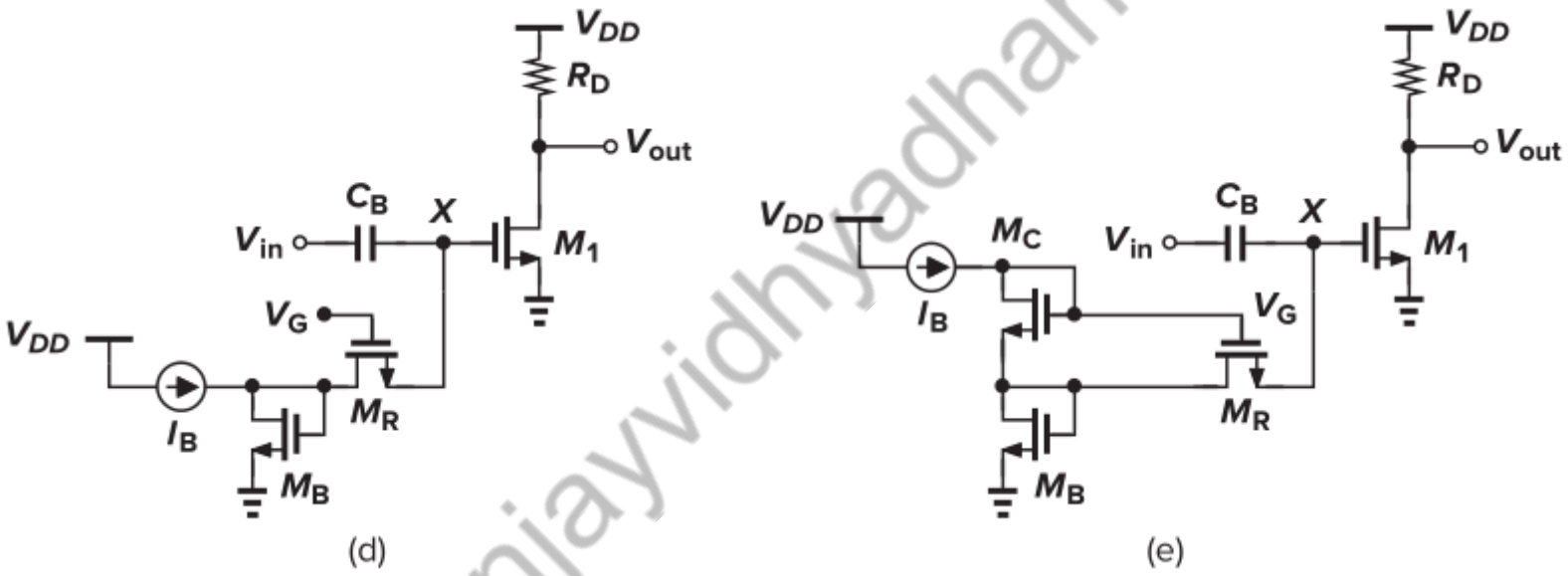


Biasing Techniques

Simple CS Stage

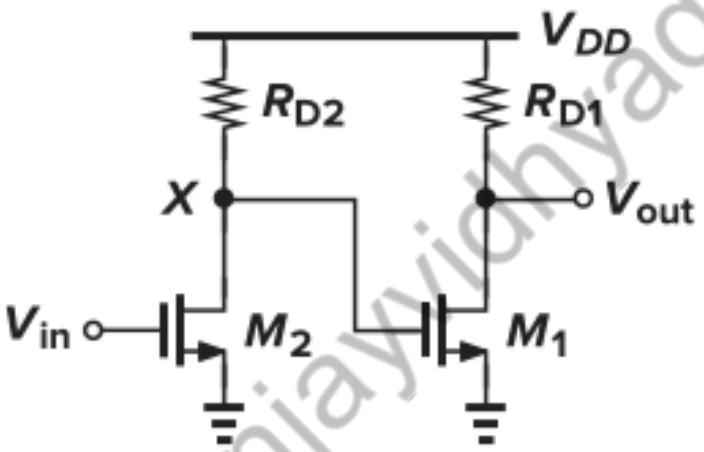


Biasing Techniques



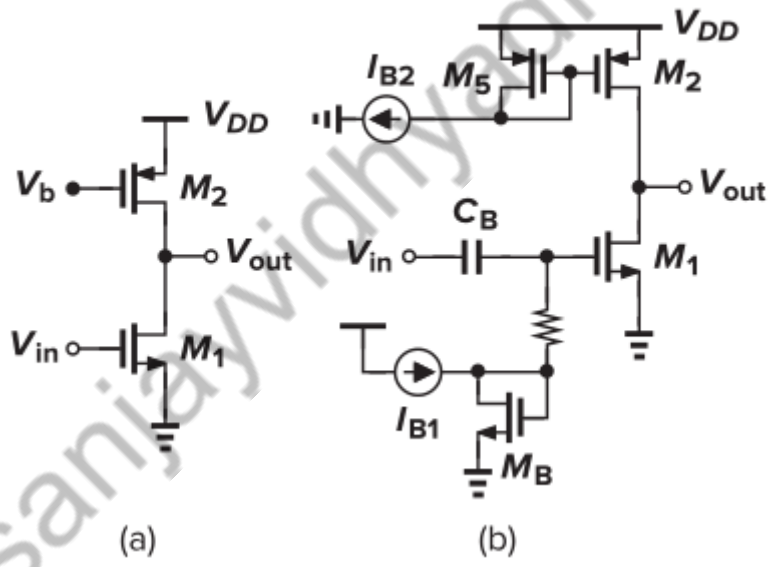
Biasing Techniques

Direct coupling between two stages.



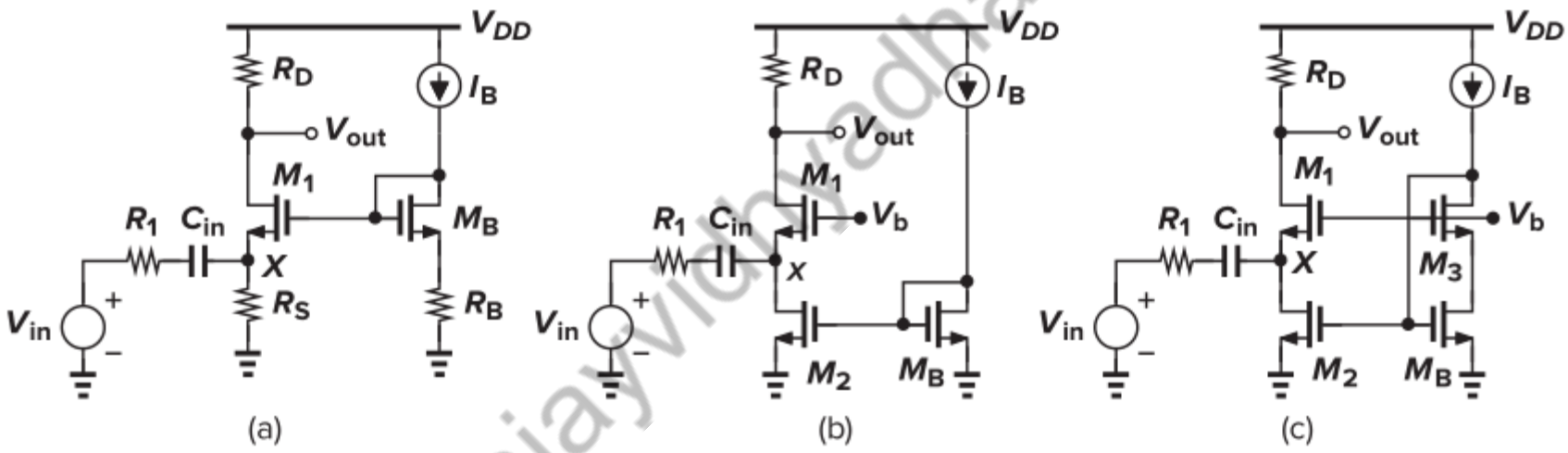
Biasing Techniques

CS Stage with Current-Source Load



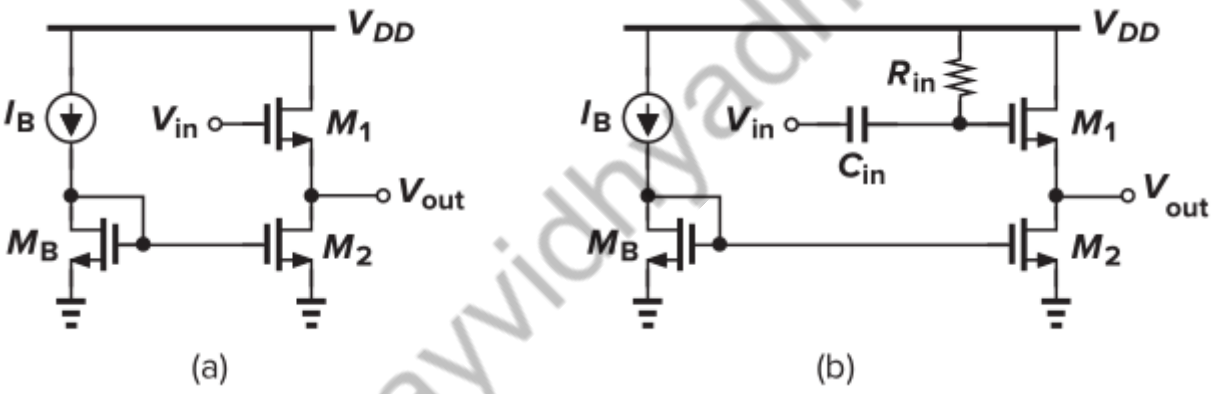
Biasing Techniques

CG Stage with Current-Source Load



Biasing Techniques

Source Follower Biasing



Thankyou