Analog IC Design : 2022-23
Lecture 7
DC Voltage and DC Current Sources

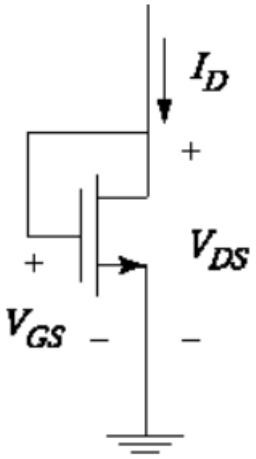
By Dr. Sanjay Vidhyadharan

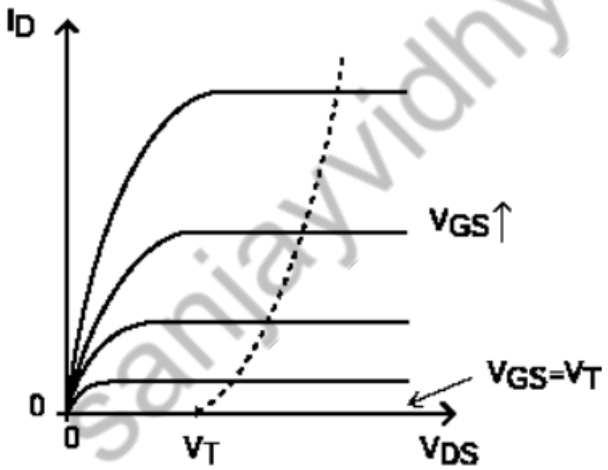
DC Voltage Sources

Characteristics of DC Voltage Sources :

- A well controlled output voltage

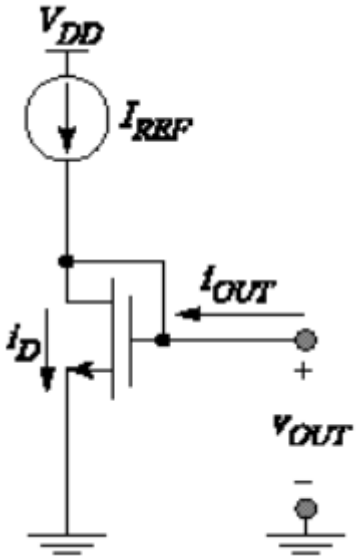
MOSFET connected in “diode configuration”





$$I_D = \frac{W}{2L}\mu_n C_{ox}(V_{GS} - V_{Tn})^2 = \frac{W}{2L}\mu_n C_{ox}(V_{DS} - V_{Tn})^2$$

DC Voltage Sources



$V_{GS} = V_{DS}$ takes a value needed to sink current

$$i_D = I_{REF} + i_{OUT} = \frac{W}{2L}\mu_n C_{ox}\left(v_{OUT} - V_{Tn}\right)^2$$

Then:

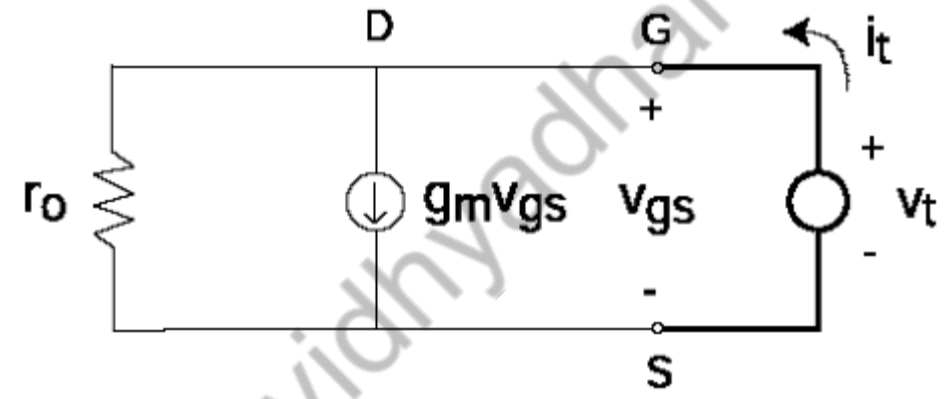
$$i_{OUT} = \frac{W}{2L}\mu_n C_{ox}\left(v_{OUT} - V_{Tn}\right)^2 - I_{REF}$$

Solving for v_{OUT}:

$$v_{OUT} = V_{Tn} + \sqrt{\frac{I_{REF} + i_{OUT}}{\frac{W}{2L}\mu_n C_{ox}}}$$

DC Voltage Sources

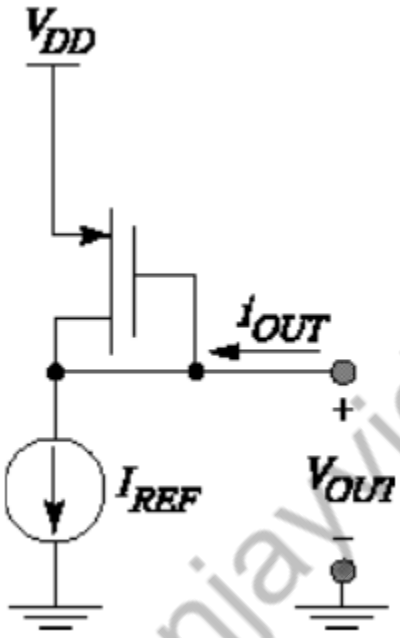
Small Signal Equivalent Circuit Model:



$$R_{out} = \frac{1}{g_m} \| r_o \approx \frac{1}{g_m}$$

DC Voltage Sources

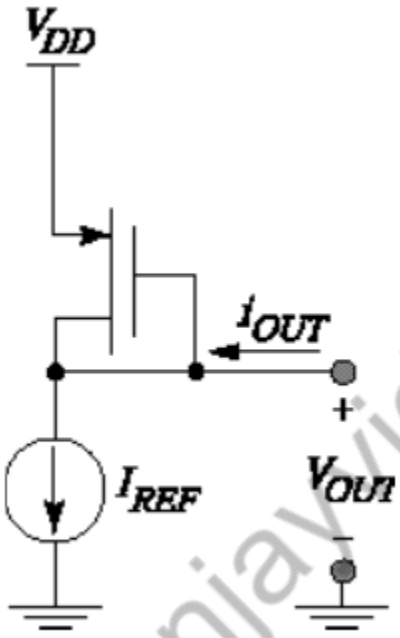
PMOS voltage source



Same operation and characteristics as NMOS voltage source. PMOS needs to be larger to attain the same Rout .

DC Voltage Sources

PMOS voltage source



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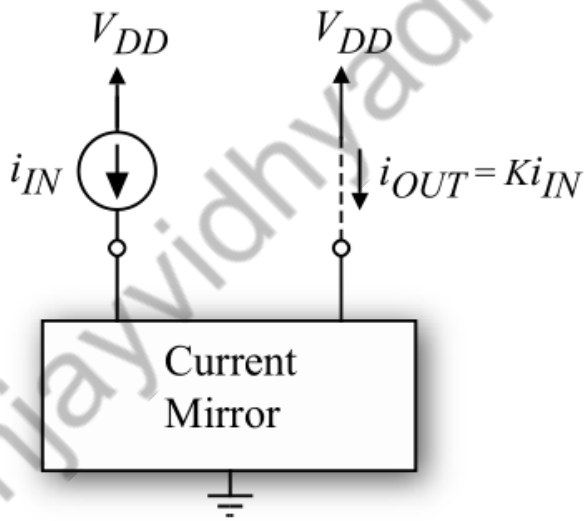
DC CURRENT MIRRORS

A current mirror replicates the input current of a current sink or current source as an output current. The output current may be identical to the input current or can be a scaled version of it.



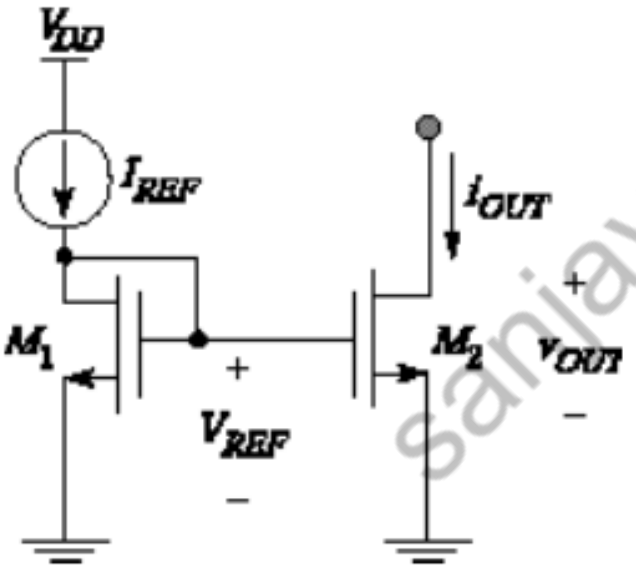
DC Current Sources

Characteristics of Current Sources

- A well controlled output current
- Supplied current does not depend on output voltage

  ⇒ High Norton Resistance

Current Mirror Circuit



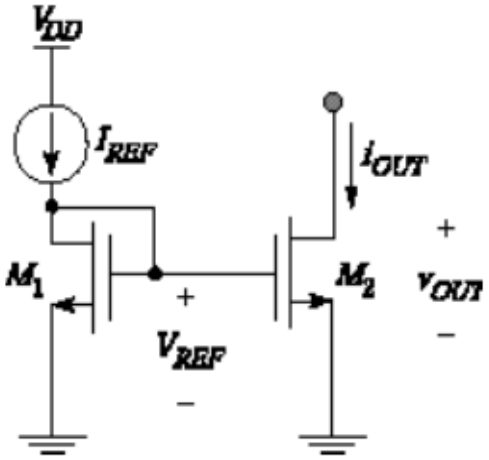
$$I_{OUT} \approx \frac{1}{2}\left(\frac{W}{L}\right)_2 \mu_n C_{ox}(V_{REF} - V_{Tn})^2$$

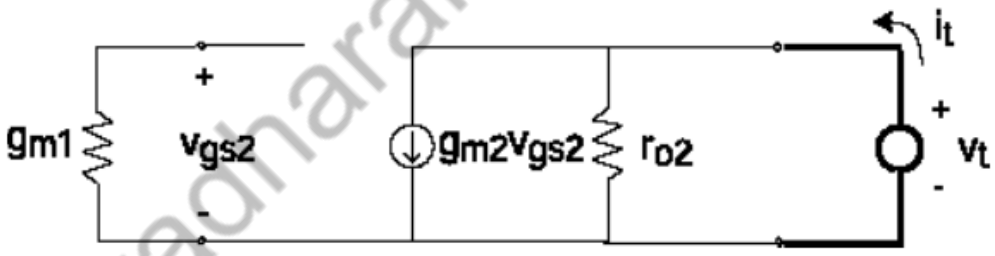
$$I_{REF} \approx \frac{1}{2}\left(\frac{W}{L}\right)_1 \mu_n C_{ox}(V_{REF} - V_{Tn})^2$$

$$I_{OUT} = I_{REF} \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1}$$

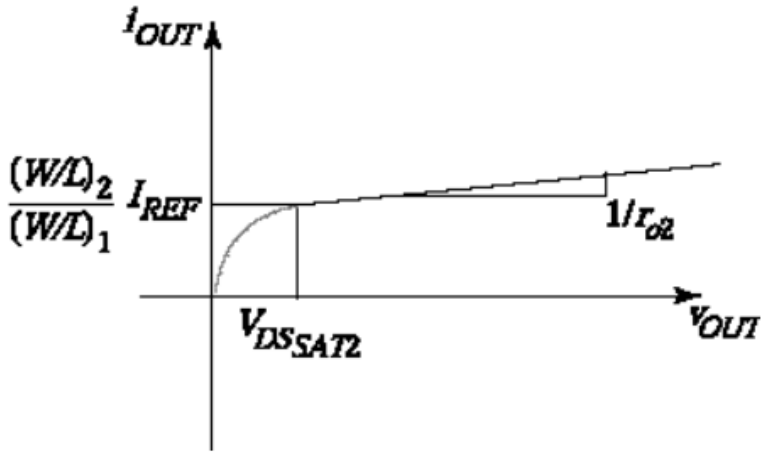
DC Current Sources

Small Signal Equivalent Circuit Model:



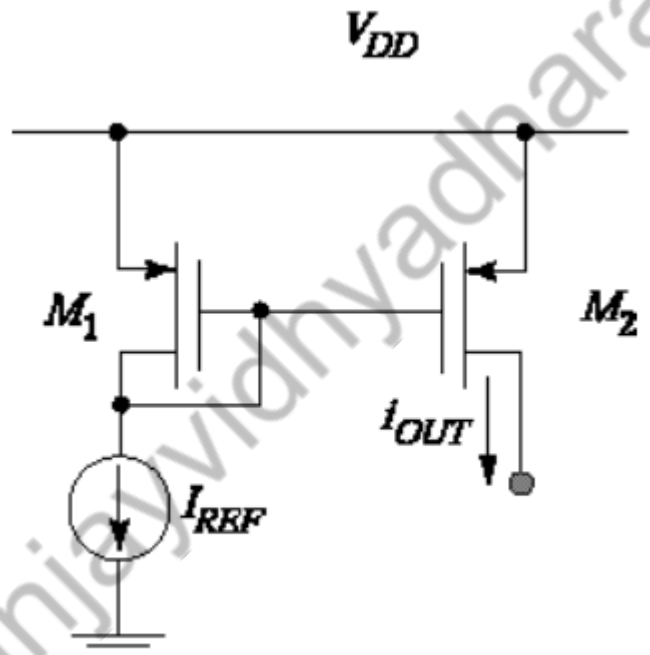


$$R_{out2} = r_{o2}$$



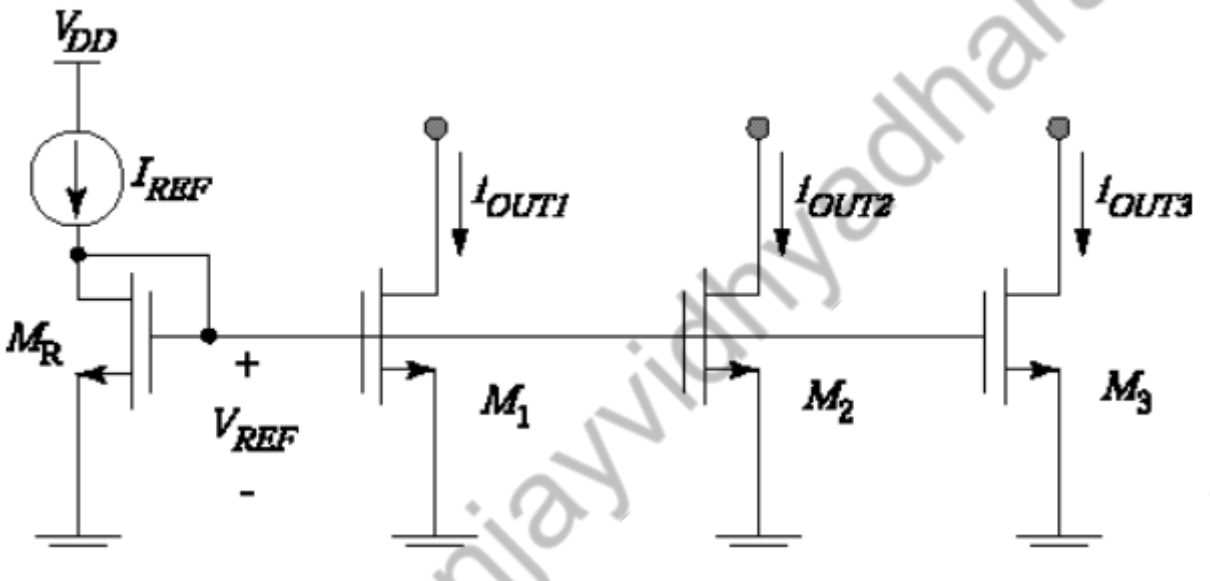
DC Current Sources

PMOS Current Source



Current Mirrors

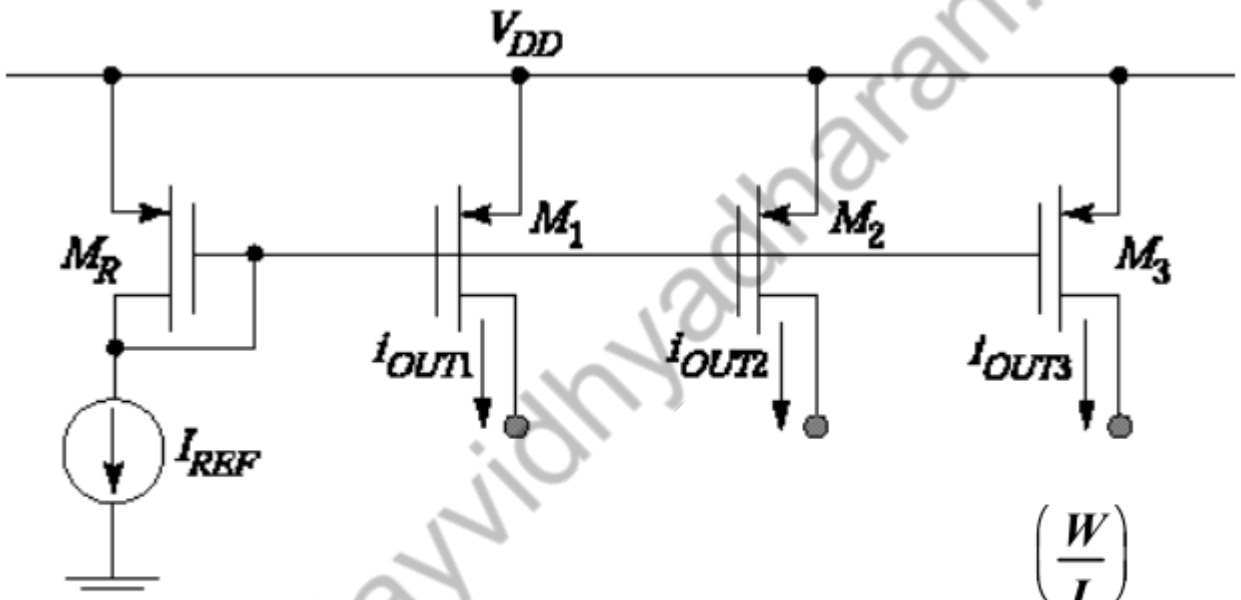
NMOS Current Mirror



$$I_{OUTn} = I_{REF} \frac{\left(\frac{W}{L}\right)_n}{\left(\frac{W}{L}\right)_R}$$

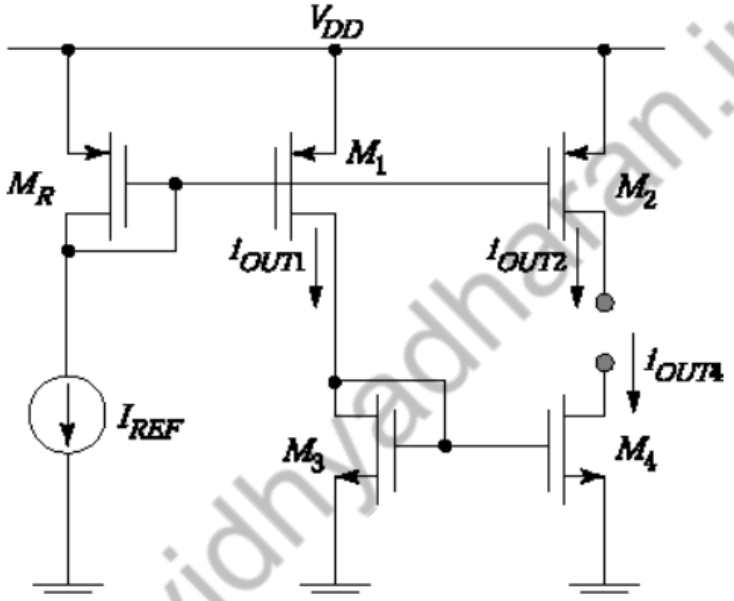
Current Mirrors

PMOS Current Mirror



$$I_{OUTn} = I_{REF} \frac{\left(\frac{W}{L}\right)_n}{\left(\frac{W}{L}\right)_R}$$

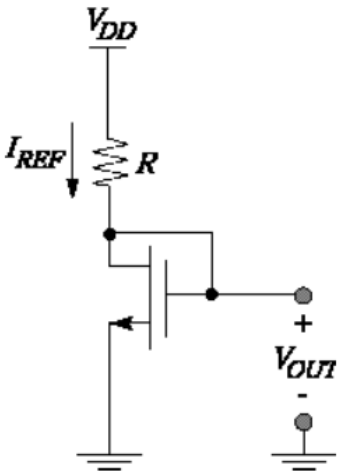
Current Mirrors



$$I_{OUT1} = I_{REF}\frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_R} \qquad I_{OUT2} = I_{REF}\frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_R}$$

$$I_{OUT4} = I_{OUT1}\frac{\left(\frac{W}{L}\right)_4}{\left(\frac{W}{L}\right)_3} = I_{REF}\frac{\left(\frac{W}{L}\right)_4\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_3\left(\frac{W}{L}\right)_R}$$

Generating I_{REF}



$$I_{REF} = \frac{V_{DD} - V_{OUT}}{R}$$

$$V_{OUT} = V_{Tn} + \sqrt{\frac{I_{REF}}{\frac{W}{2L}\mu_n C_{ox}}}$$

For large W/L: $$I_{REF} \approx \frac{V_{DD} - V_{Tn}}{R}$$

Advantages

– I_{REF} set by value of resistor

• Disadvantages

– V_{DD} also affects I_{REF} .

– V_{Tn} and R are functions of temperature

In the real world, more sophisticated circuits are used to generate I_{REF} that are V_{DD} and T independent.

Influence of the Channel Modulation Parameter λ

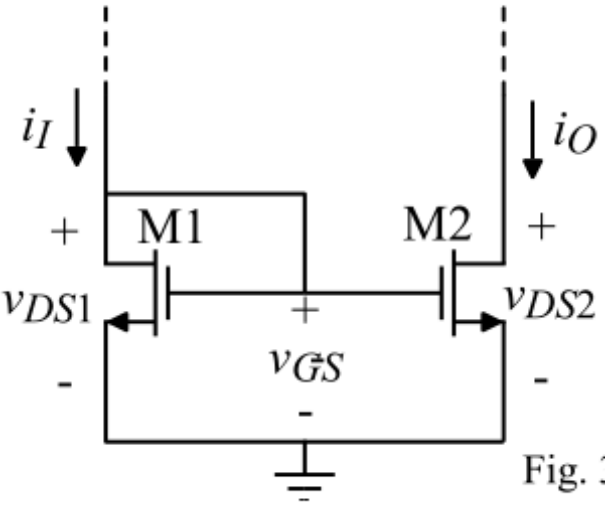


Fig. 1

Assume that $v_{DS2} > v_{GS} - V_{T2}$, then

$$\frac{i_O}{i_I} = \left(\frac{L_1 W_2}{W_1 L_2}\right)\left(\frac{V_{GS}-V_{T2}}{V_{GS}-V_{T1}}\right)^2\left[\frac{1+\lambda v_{DS2}}{1+\lambda v_{DS1}}\left(\frac{K_2'}{K_1'}\right)\right]$$

If the transistors are matched, then $K_1' = K_2'$ and $V_{T1} = V_{T2}$

$$\frac{i_O}{i_I} = \left(\frac{L_1 W_2}{W_1 L_2}\right)\left(\frac{1+\lambda v_{DS2}}{1+\lambda v_{DS1}}\right)$$

If $v_{DS1} = v_{DS2}$, then

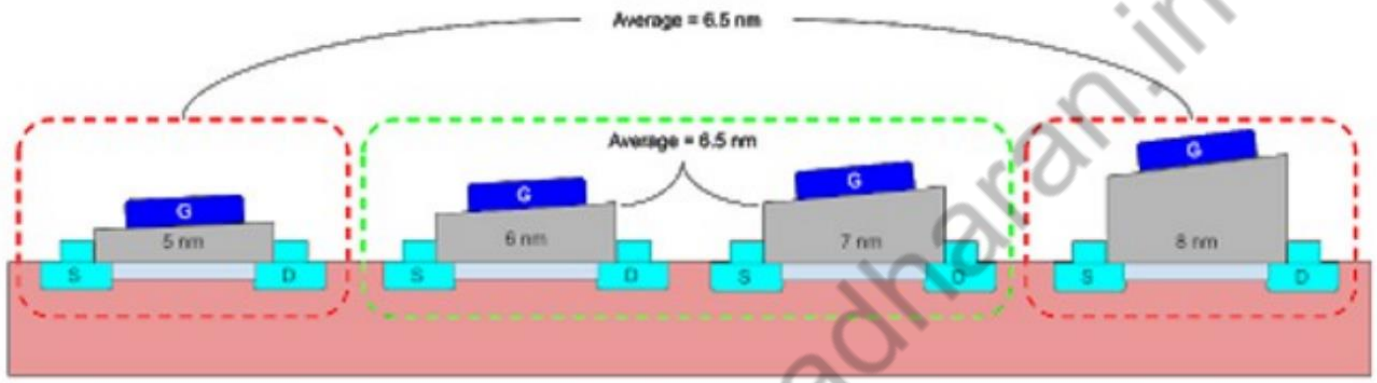
$$\frac{i_O}{i_I} = \left(\frac{L_1 W_2}{W_1 L_2}\right)$$

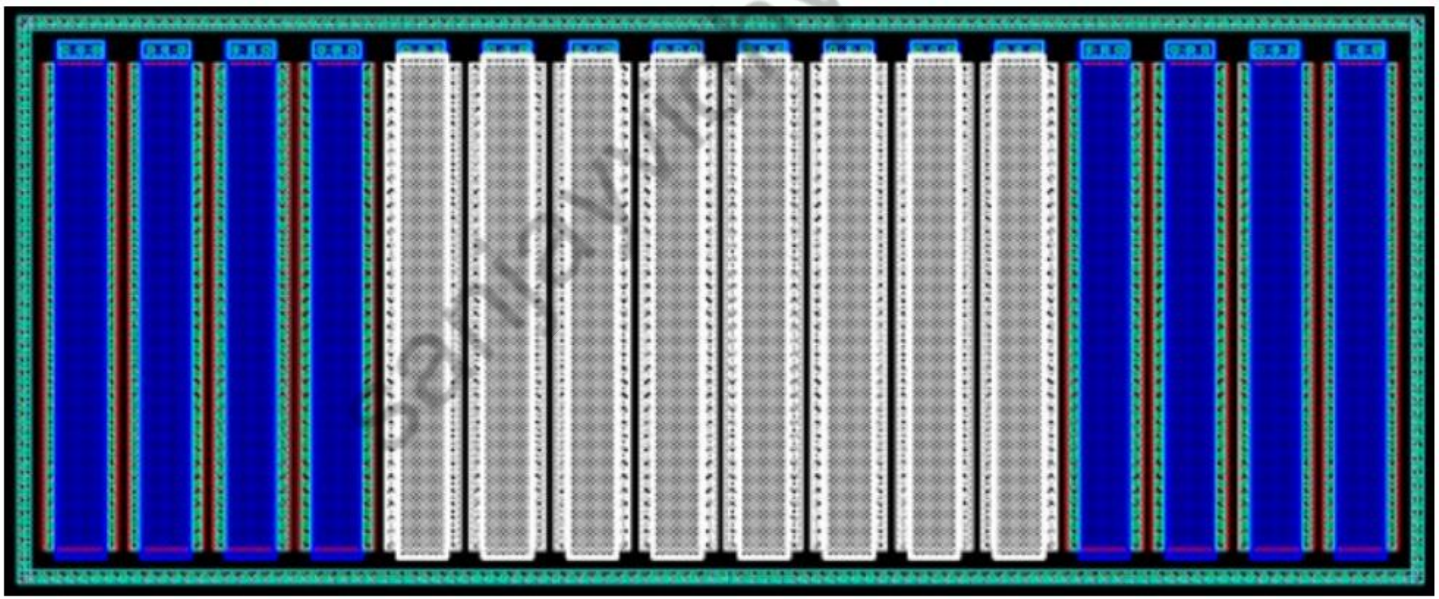
Therefore the sources of error are:

1.) $v_{DS1} \neq v_{DS2}$

2.) M1 and M2 are not matched.

Common centroid design evens out the effect of the process variation.





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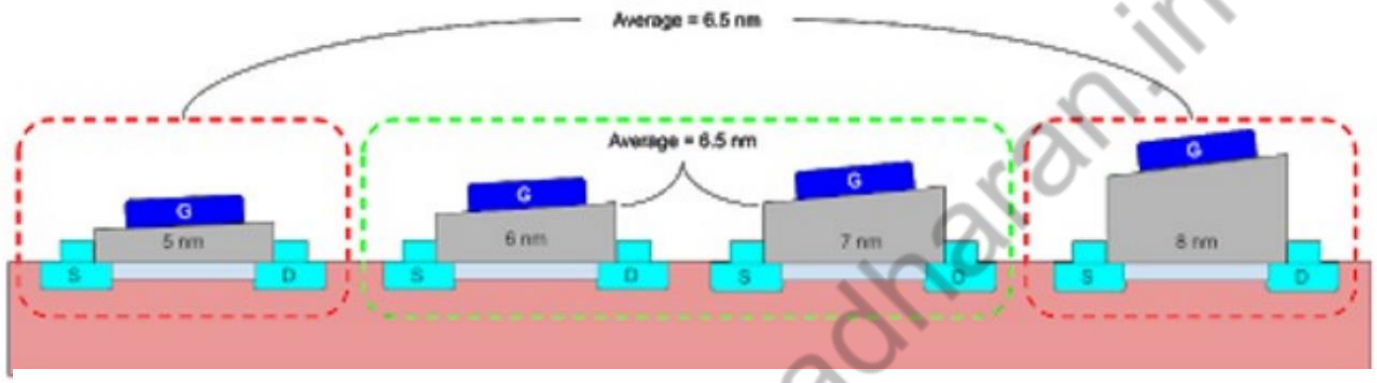

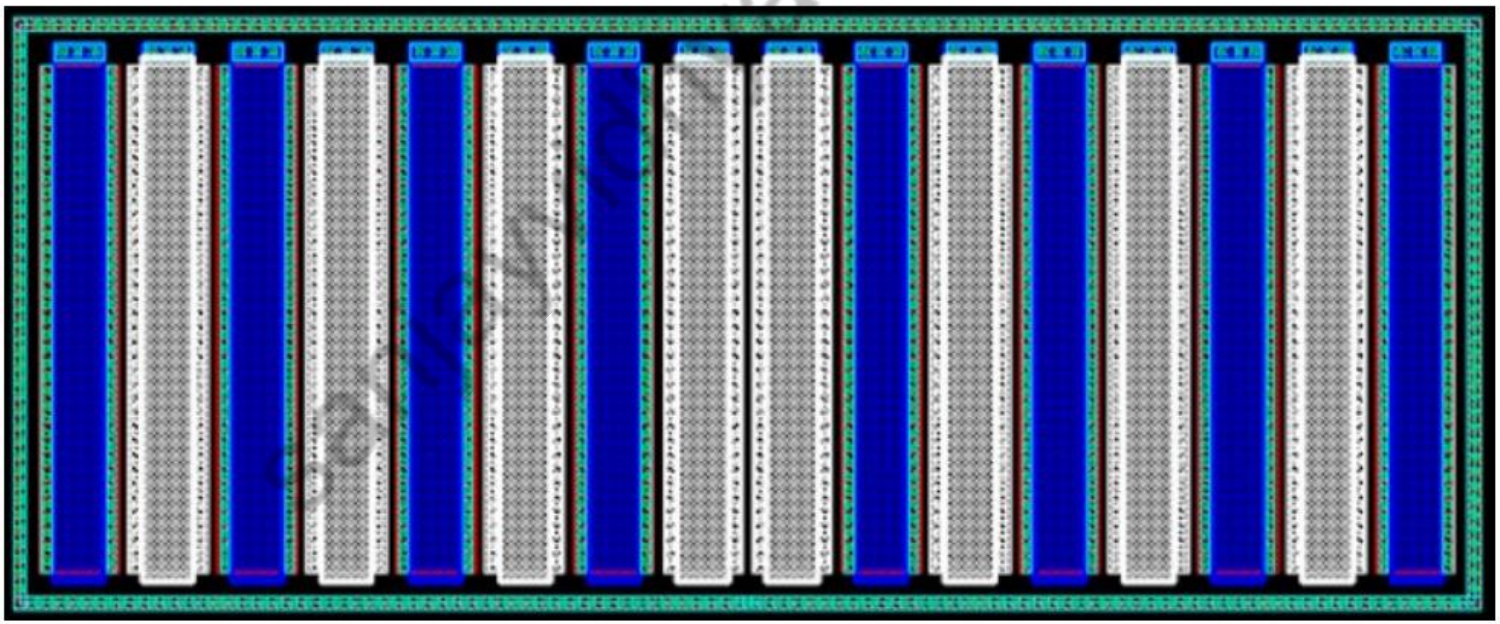

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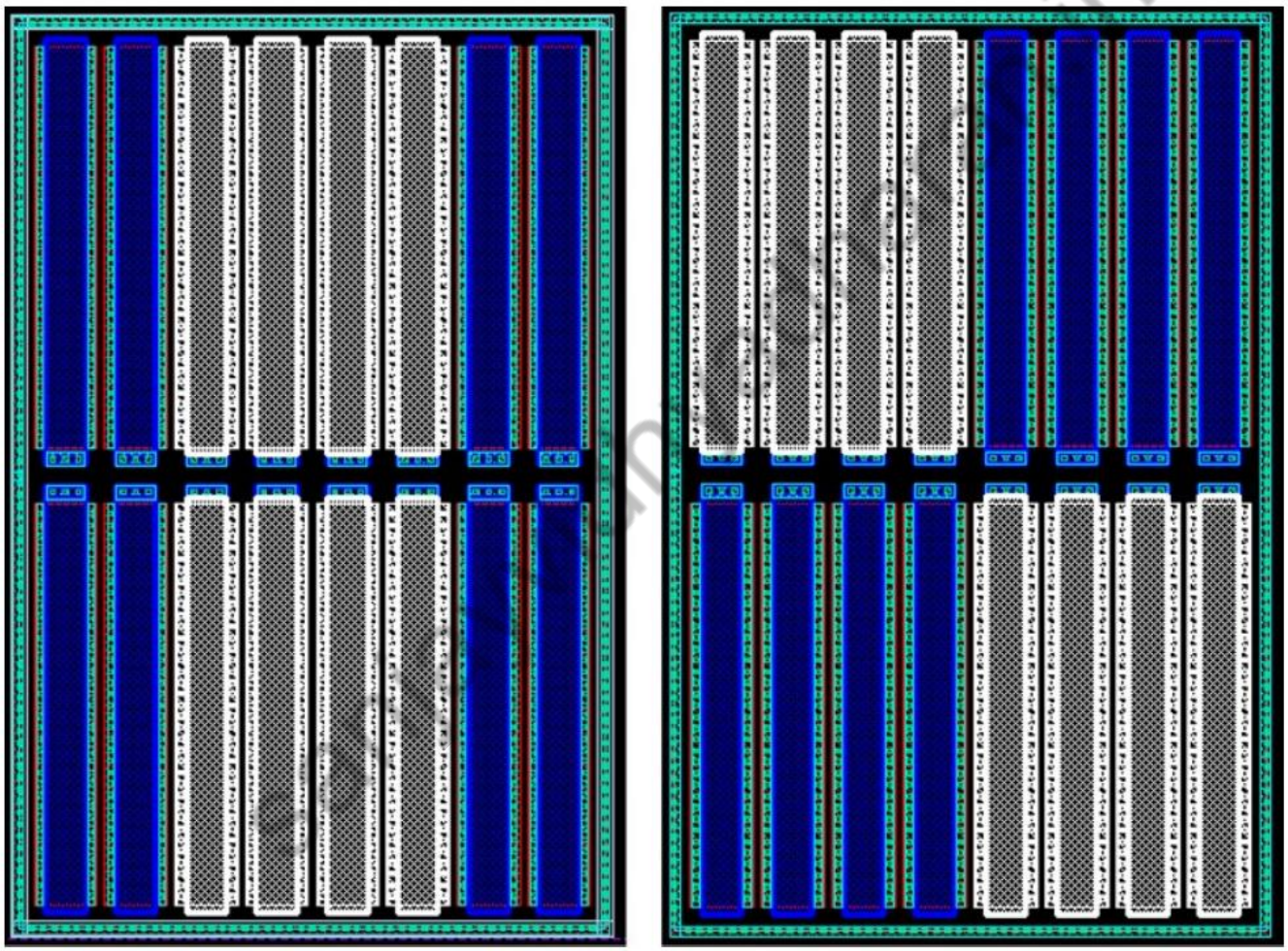

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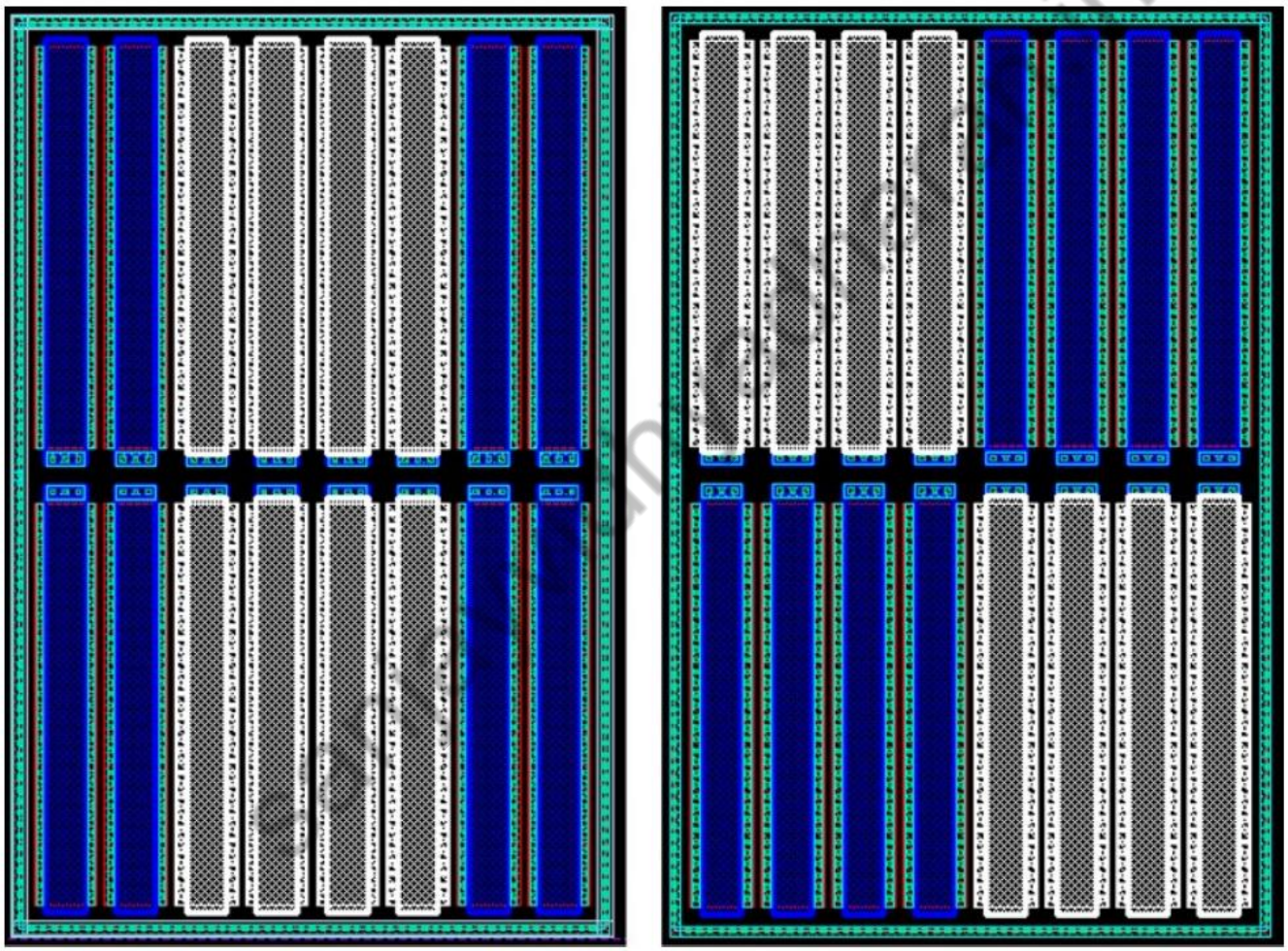


Current Mirror Specifications

- Small-signal output resistance R_O.
- Minimum output voltage V_{Omin}.
- Current gain error definition:

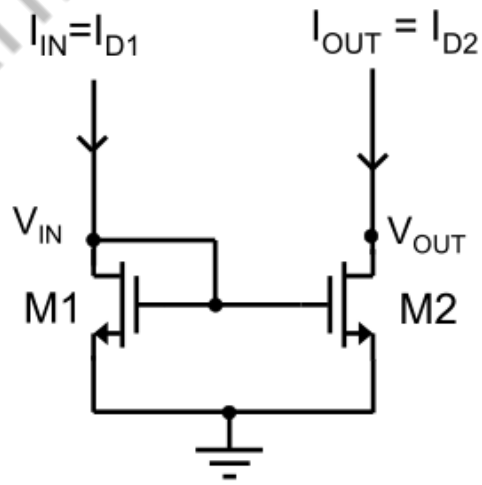
$$E = \frac{I_{OUT} - I_{OUT\_ideal}}{I_{OUT\_ideal}}$$

- Two types of error:
  - systematic error: error caused by circuit structure.
  - Random error: error caused by process variations.
- These two types of error are commonly seen in many analog circuits.
- A robust design is to minimize both systematic error and random error.

Current Mirror Analysis

- As $V_{GS1} = V_{GS2}$ and assuming matched $V_{TH1} = V_{TH2}$

$$\frac{I_{OUT}}{I_{IN}} = \frac{\left(W/L\right)_2 (1+\lambda V_{OUT})}{\left(W/L\right)_1 (1+\lambda V_{IN})}$$



- The output resistance of current source is the output resistance of M2

$$R_O = \frac{1}{\lambda I_{D2}} = \frac{1}{\lambda I_{OUT}}$$

- Normally, larger L is used so that λ effect is reduced and the output resistance is higher.
- The current gain systematic error is:

$$I_{OUT\_ideal} = \frac{(W/L)_2}{(W/L)_1} I_{IN}$$

$$E = \frac{I_{OUT} - I_{OUT\_ideal}}{I_{OUT\_ideal}} = \frac{(1+\lambda V_{OUT})}{(1+\lambda V_{IN})} - 1 = \frac{\lambda}{(1+\lambda V_{IN})}(V_{OUT} - V_{IN}) \approx \lambda (V_{OUT} - V_{IN})$$

Current Mirror Analysis

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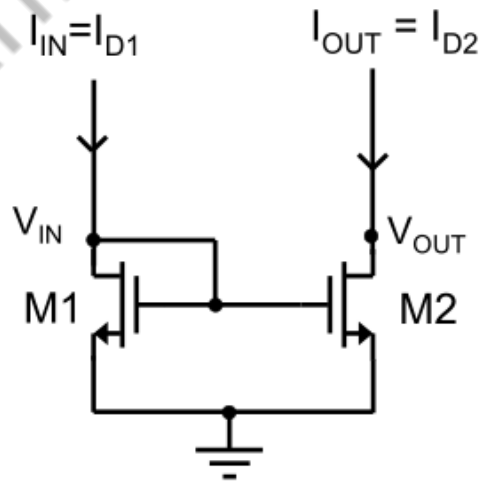

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Current Mirror Analysis

- This current relationship will be true as long as M2 is in saturation. Clearly, this will happen when $V_O = V_{DS2} > V_{OD2}$
- Gates of two transistors are connected: $V_{GS2} = V_{GS1}$ so $V_{GS2} - V_{TH2} = V_{GS1} - V_{TH1}$ as $V_{TH1} = V_{TH2} \rightarrow V_{OD1} = V_{OD2}$
- Define the minimum output voltage: $V_{Omin} > V_{GS2} - V_{TH2} = V_{OD}$
- Hence it is a benefit to have a low gate overdrive to increase the output swing.
- How much should the gate overdrive be?
- For same drain current, if the overdrive is small, transistor size will be very large, giving area penalty and speed penalty.
- Overdrive voltage is a trade-off between speed and minimum output swing. Typically, overdrive is selected between 0.1-0.4V.

Current Mirror Analysis

A current mirror with current ratio of two is designed. Assume $V_{IN}=V_{OUT}$ to eliminate the channel length modulation effect.

Due to mismatch between M1 and M2, the output current is not exactly two times of the input current.

3 ways to implement:

- A: $W_2=W_1$, $L_2=0.5L_1$

$$\frac{I_{OUT}}{I_{IN}}=\frac{\left(W/L\right)_2(1+\lambda_2 V_{OUT})}{\left(W/L\right)_1(1+\lambda_1 V_{IN})}\neq 2$$

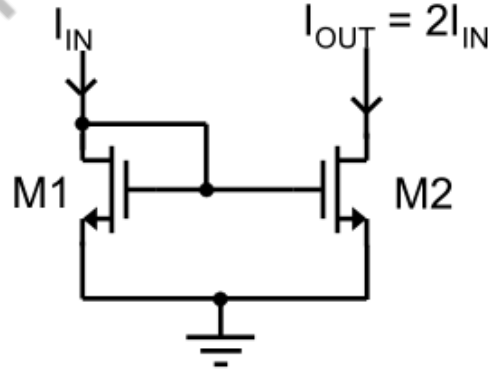
  - λ mismatch
- B: $W_2=2W_1$, $L_2=L_1$
  - ΔW and ΔL mismatch

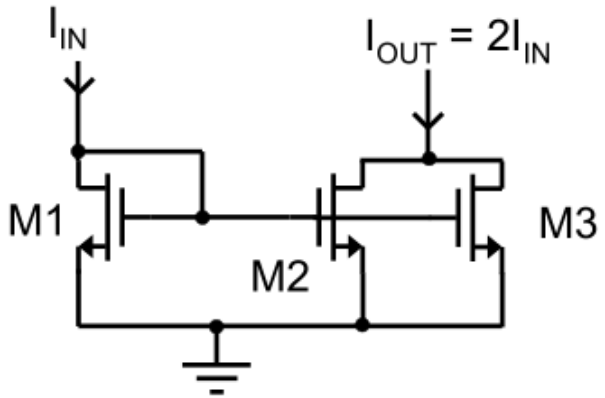
$$\frac{I_{OUT}}{I_{IN}}=\frac{\frac{2W+\Delta W}{L+\Delta L}}{\frac{W+\Delta W}{L+\Delta L}}\neq 2$$

- C: Two transistors in parallel, $W_3=W_2=W_1$, $L_3=L_2=L_1$

  Best solution

$$\frac{I_{OUT}}{I_{IN}}=\frac{\frac{2(W+\Delta W)}{L+\Delta L}}{\frac{W+\Delta W}{L+\Delta L}}=2$$





Eliminate the Systematic Error

As we have seen, first simple current mirror output current ($I_{OUT} = I_{D2}$) changes when the drain voltage of M2 changes. From model parameter $\lambda = 0.05$, the change in I_{OUT} for a 1V change in V_{D2} will be 5%, which is not acceptable in many analog applications.

Can we do something about this?

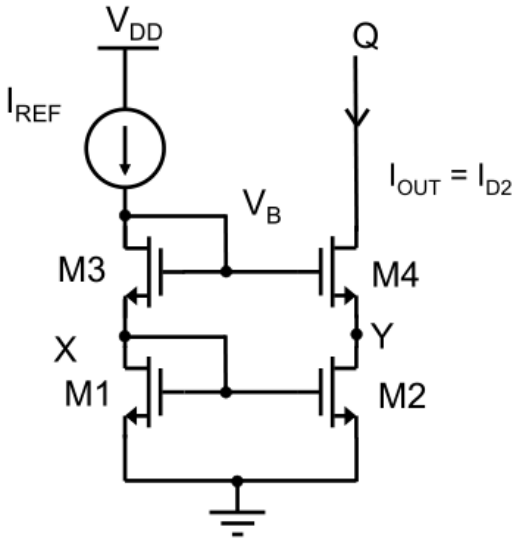
$$E = \frac{I_{OUT} - I_{OUT\_ideal}}{I_{OUT\_ideal}} = \frac{(1+\lambda V_{OUT})}{(1+\lambda V_{IN})} - 1 \approx \lambda(V_{OUT} - V_{IN})$$

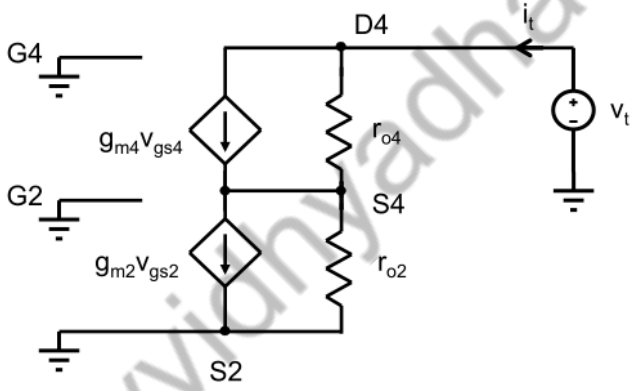
The key to eliminate the current gain systematic error is to make $V_{OUT}=V_{IN}$ in the simple current mirror.

A straightforward way to achieve this would be having an extra MOSFET in series with M2 and fix the drain voltage of M2 to V_{IN}. This extra transistor is called cascode transistor.

Standard Cascode Current Mirror

Output Resistance





$v_{gs2}=0,\ v_{gs4} = -\ i_t\ r_{o2}$

$$i_t = \frac{v_t - v_{s4}}{r_{o4}} - g_{m4} i_t r_{o2}$$

$$i_t(1 + g_{m4} r_{o2}) = \frac{v_t - i_t r_{o2}}{r_{o4}}$$

$$R_O = \frac{v_t}{i_t} = r_{o4}(1 + g_{m4} r_{o2}) + r_{o2}$$

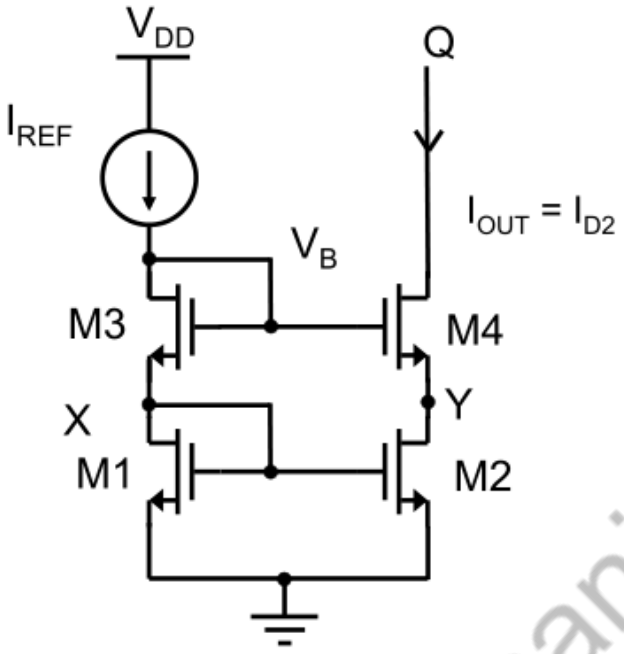
$$R_O = g_{m4} r_{o2}^2$$

If body effect is included: $R_O = (g_{m4} + g_{mb}) r_{o2}^2$

Features of Cascode current mirror:

- No current gain systematic error.
- Higher output resistance.
- Higher minimum output voltage.

Standard Cascode Current Mirror



All 4 MOSFETs have the same V_{TH} if body effect is ignored.

$V_X = V_Y = V_{TH} + V_{OV}$

$V_{GS3} = V_{OV} + V_{TH}$ as M1 and M3 carry the same "I"

$V_{G3} = V_{GS3} + V_X = 2V_{TH} + 2V_{OV}$ ignoring body effect.

$V_{G4} = 2V_{TH} + 2V_{OV}$

This should also be the case with body effect – only $2V_{TH}$ will become $V_{TH1} + V_{TH3}$.

Min Vout = $V_X + V_{OV} = V_{TH} + 2V_{OV}$