Analog IC Design : 2022-23
Lecture 5
Differential Amplifiers Part-2

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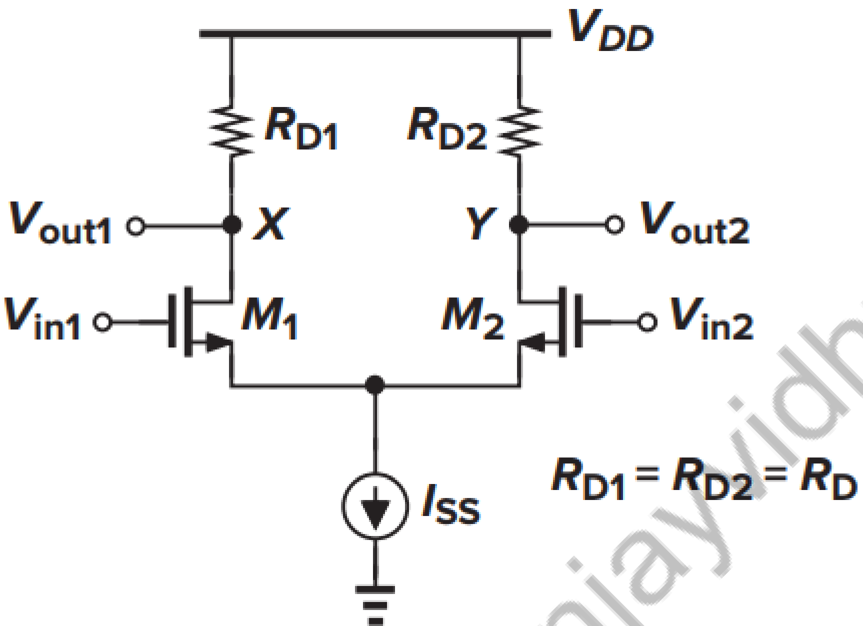
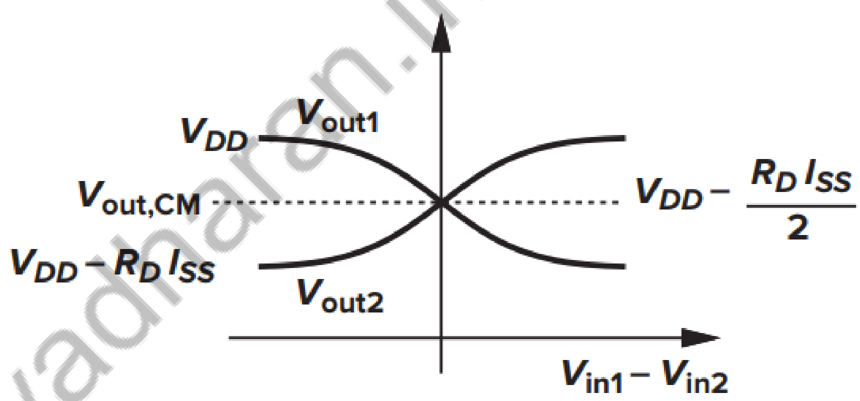
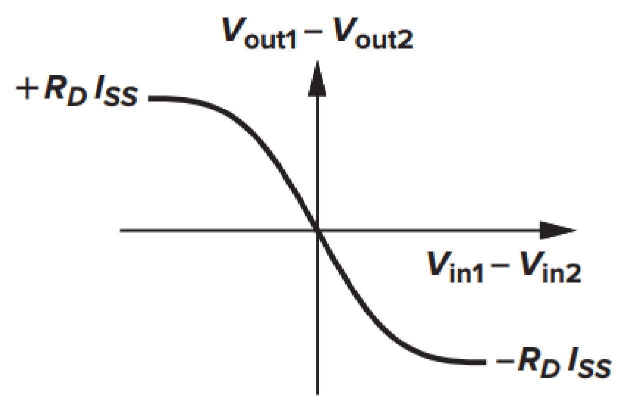
ELECTRICAL ELECTRONICS COMMUNICATION INSTRUMENTATION

Basic MOS Differential Pair

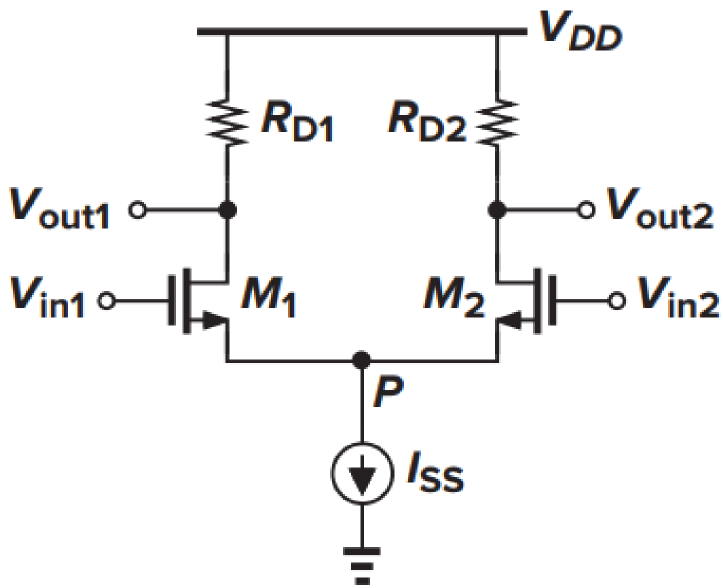






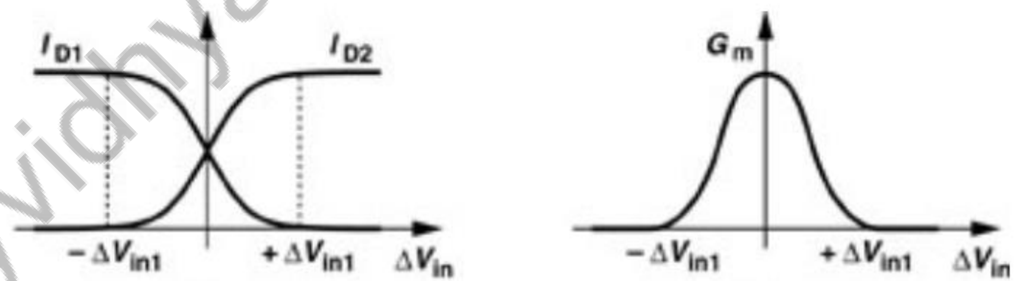
"Current stealing " phenomenon

MOS Differential Pair



Differential Transconductance Gain vs. Input Voltage

$$\frac{\partial \Delta I_D}{\partial \Delta V_{in}} = G_m = \frac{\mu_n C_{ox}}{2}\frac{W}{L}\frac{\frac{4I_{SS}}{\mu_n C_{ox} W/L} - 2(V_{in1}-V_{in2})^2}{\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - (V_{in1}-V_{in2})^2}}$$



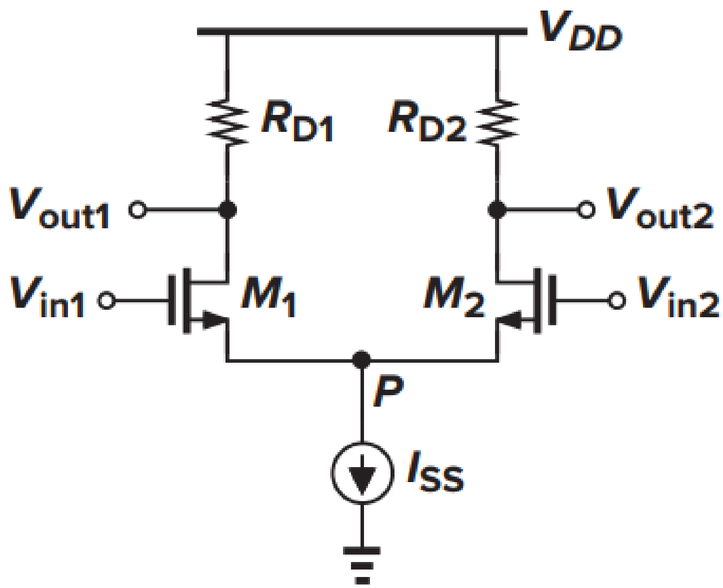
(a) (b)

Maximum Differential Transconductance Gain Occurs at ΔVin=0

$$g_m = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)I_D}$$

$$G_{m,\max} = \sqrt{\mu_n C_{ox}\left(\frac{W}{L}\right)I_{SS}}$$

MOS Differential Pair



Differential Voltage Gain

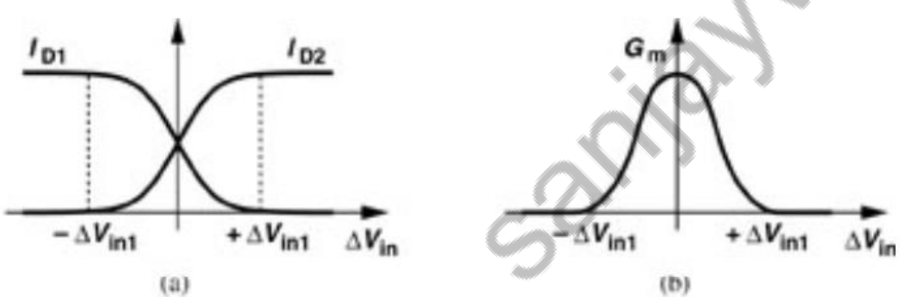
$$V_{out1} - V_{out2} = R_D \Delta I_D = R_D G_m \Delta V_{in}$$

Differential Voltage Gain near ΔVin= 0

$$|A_V| = \frac{\Delta V_{out}}{\Delta V_{in}} = G_{m,\max} R_D = \sqrt{\mu_n C_{ox} \frac{W}{L} I_{SS}}\, R_D$$

Differential Transconductance Gain Falls to Zero at ΔVin= ΔVin1

$$\frac{\partial \Delta I_D}{\partial \Delta V_{in}} = G_m = \frac{\mu_n C_{ox}}{2} \frac{W}{L} \frac{\frac{4I_{SS}}{\mu_n C_{ox} W/L} - 2(V_{in1} - V_{in2})^2}{\sqrt{\frac{4I_{SS}}{\mu_n C_{ox} \frac{W}{L}} - (V_{in1} - V_{in2})^2}}$$

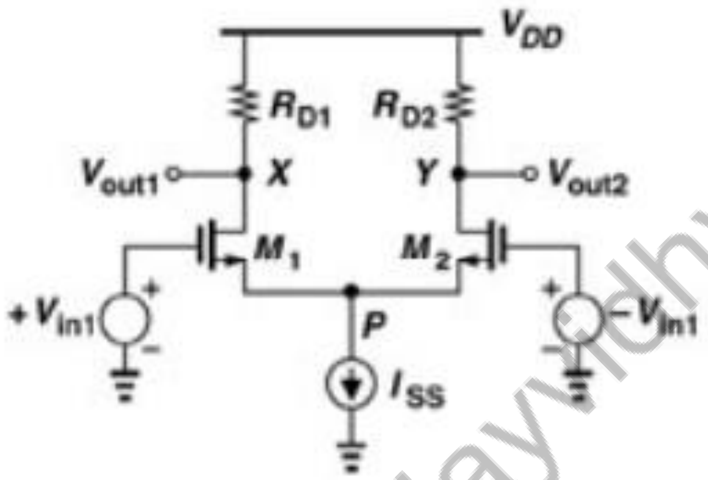


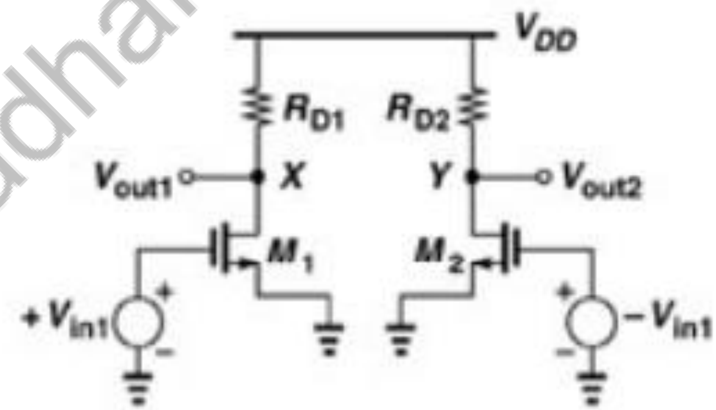
$$\Delta V_{in1} = \sqrt{\frac{2I_{SS}}{\mu_n C_{ox} \frac{W}{L}}}$$

ΔVin= ΔVin1 is the maximum differential input that the amplifier can "handle"

The "Virtual Ground" Concept

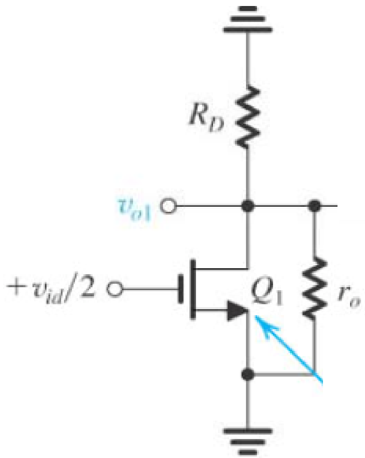
The "Half-Circuit" Concept





Differential Mode Response

Differential-mode small-signal half-circuit



$$\frac{v_{o1}}{v_{id}/2} = -g_m(R_D \parallel r_o)$$

For the total circuit

$$v_{od} = v_{o1} - v_{o2}$$

$$\text{But } v_{o2} = -v_{o1}$$

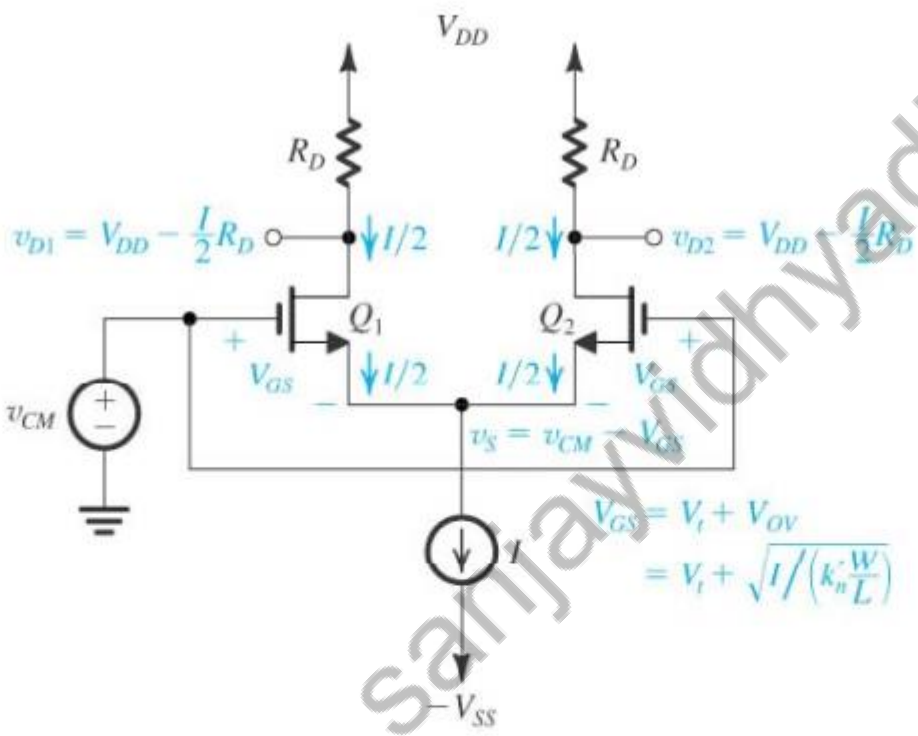
$$\therefore v_{od} = 2v_{o1}$$

CS amplifier for input difference!

$$A_d = \frac{v_{od}}{v_{id}} = \frac{2v_{o1}}{v_{id}} = -g_m(R_D \parallel r_o)$$

MOS Differential Pair

Common-Mode



For identical Q_1 and Q_2

$$i_{D1} = i_{D2} = \frac{I}{2}$$

$$v_{D1} = v_{D2} = V_{DD} - \frac{I}{2}R_D$$

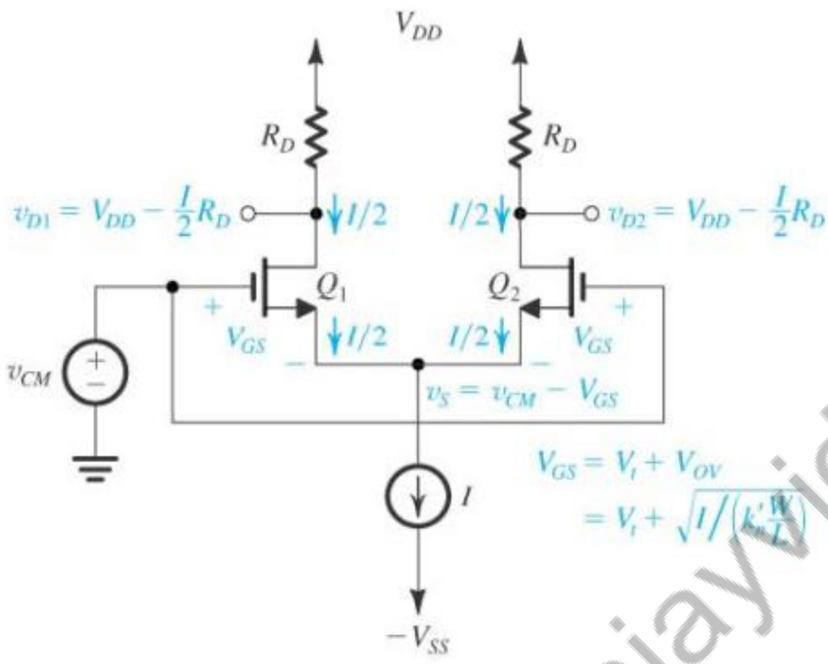
$$\therefore v_{D1} - v_{D2} = 0$$

==> No CM output

CMRR = ????

MOS Differential Pair

Common-Mode



$V_{CM,\,max}$?

$$v_{DS} \geq v_{GS} - V_t$$

$$(V_{DD} - \frac{I}{2}R_D) - (V_{CM} - v_{GS}) \geq v_{GS} - V_t$$

$$\therefore V_{DD} - \frac{I}{2}R_D + V_t \geq V_{CM}$$

$$V_{CM,\max} = V_{DD} - \frac{I}{2}R_D + V_t$$

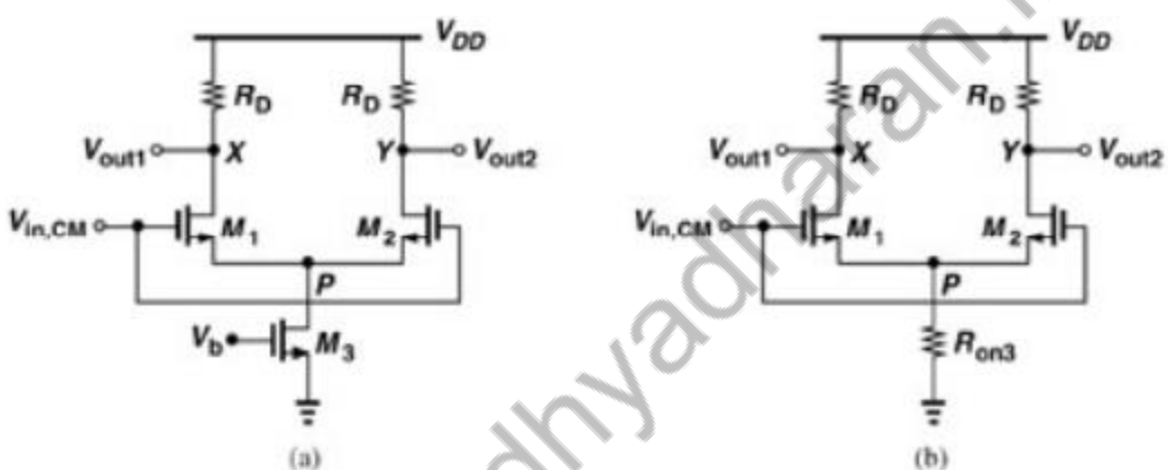
How to Maximise ?

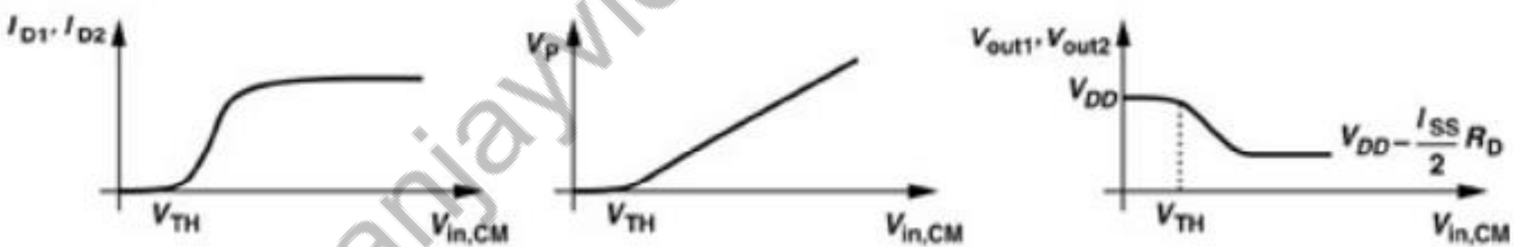
If a voltage V_{CS} is needed across the current source, then

$V_{CMmin} = -V_{SS} + V_{CS} + V_t + V_{OV}$

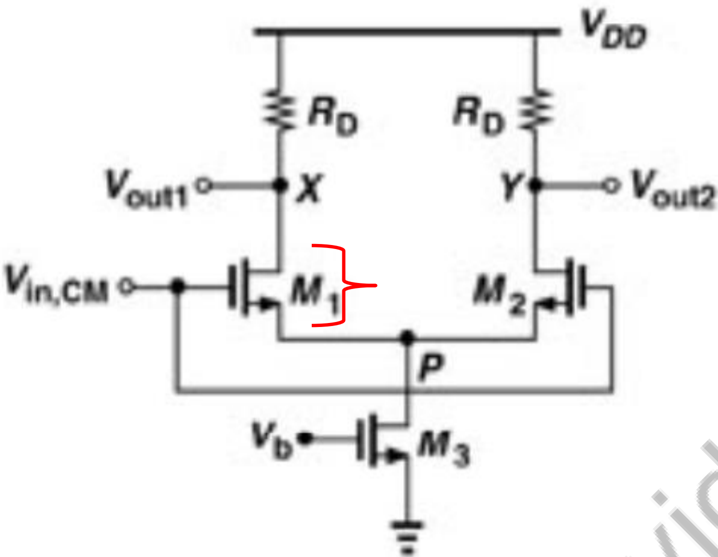
How to Minimise ?

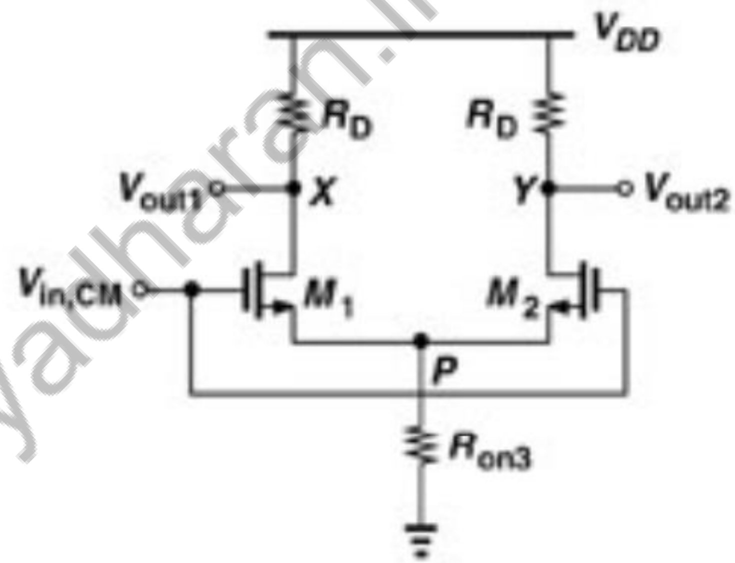
Common-Mode Response





Common-Mode Response



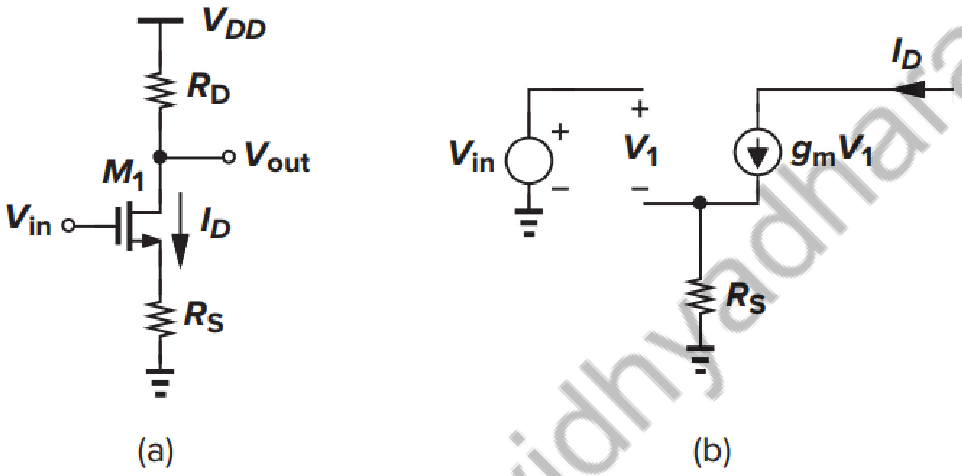


$$V_{GS1} + (V_{GS3} - V_{TH3}) \le V_{in,CM} \le \min[V_{DD} - R_D \frac{I_{SS}}{2} + V_{TH1}, V_{DD}]$$

Input common-mode range (*ICMR*) The input common-mode range is the range of common-mode voltages over which the differential amplifier continues to sense and amplify the difference signal with the same gain.

Typically, the *ICMR* is defined by the common-mode voltage range over which all MOSFETs remain in the saturation region

CS stage with Source Degeneration.



$$v_{in} = v_{gs+}\, i_d\, R_s$$

$$v_{in} = v_{gs+}\, g_m\, v_{gs}\, R_s$$

$$v_{in} = v_{gs}\ \ (1 + g_m\, R_s)$$

$$v_{out} = -i_d\, R_D$$

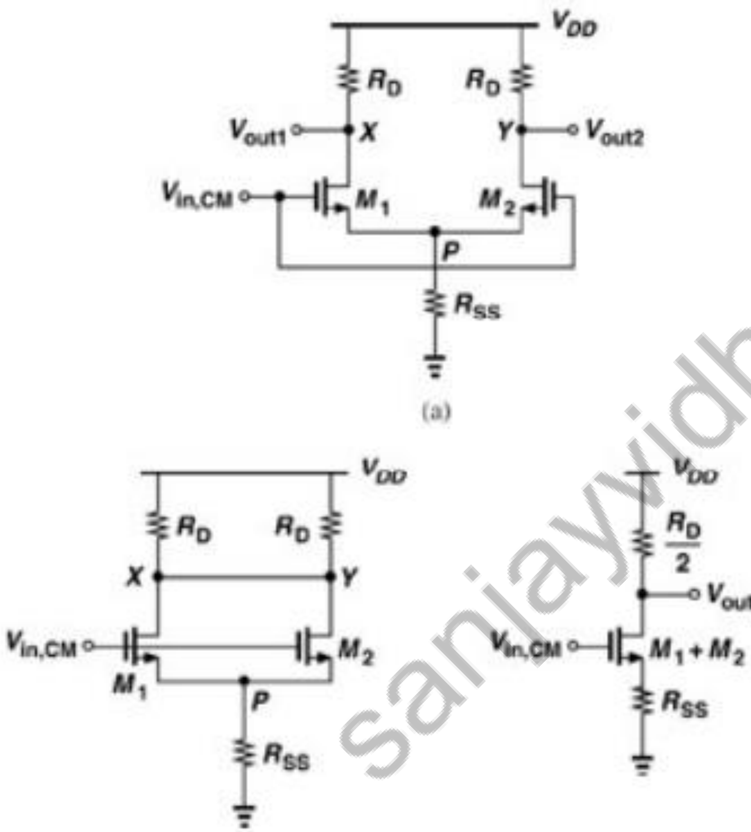
$$v_{out} = -v_{gs}\ \ g_m\, R_D$$

$$Gain = \frac{-g_m\, R_D}{1 + g_m\, R_s}$$

$$Gain = \frac{-R_D}{\frac{1}{g_m} + R_s}$$

Common-Mode Response

Single-ended Common-Mode Response of a symmetric amplifier



(a) (b) (c)

As $V_{in,CM}$ changes so does V_P. As a result, I_D currents change and V_X and V_Y change. V_X-V_Y continues to be zero

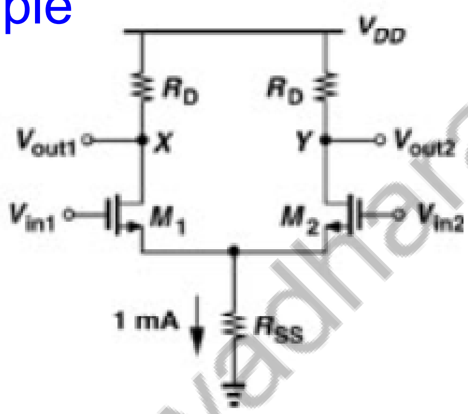
$$A_{V,CM} = \frac{V_{out}}{V_{in,CM}} = \frac{V_X}{V_{in,CM}} = \frac{V_Y}{V_{in,CM}}$$

$$= -\frac{R_D/2}{1/(2g_m) + R_{SS}}$$

How to Minimize A_{CM}?

Example

"Resistor current source" example



$R_D = 3.16K\Omega$

- Example: Let V_{DD}=3V, $(W/L)_1=(W/L)_2=25/0.5$
- $\mu_n C_{OX}=50\mu A/V^2$, $V_{TH}=0.6V$, $\lambda=0$, $\gamma=0$, $R_{SS}=500\Omega$
- Because $I_{D1}=I_{D2}=0.5mA$, we have:

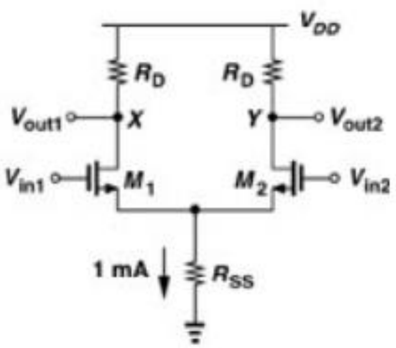
$$V_{GS1}=V_{GS2}=\sqrt{\frac{2I_{D1}}{\mu_n C_{OX}\frac{W}{L}}}+V_{TH}=1.23V$$

  - Also: $V_S=I_{ss}R_{SS}=0.5V$
  - Bias voltage at gates $V_{in,CM}=V_{GS1}+V_S=1.73V$

What is min CM Voltage?

Example

"Resistor current source" example



$R_D = 3.16K\Omega$

$$g_m = \sqrt{2\mu_n C_{OX}\frac{W}{L}I_{D1}} = \frac{1}{632\Omega}$$

$$g_m = \sqrt{(2 * 50 * 10^{-6} * \frac{25}{0.5} * 0.5 * 10^{-3}}$$

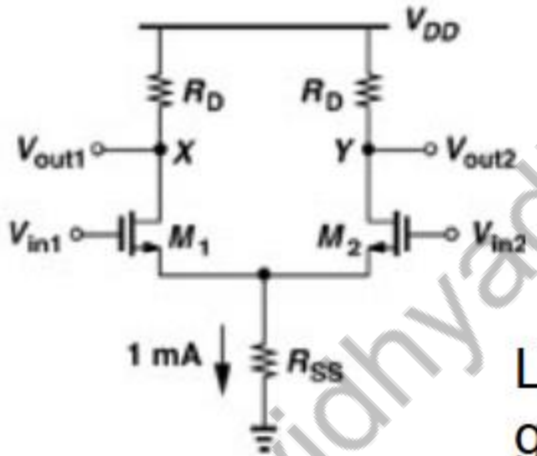
Hence differential voltage gain = $g_m R_D$=5

$V_{out1} = V_{out2} = V_{DD} - I_D R_D = 1.42\ V > V_{GS} - V_{TH}$

$V_{GS} - V_{TH} = 1.23 - 0.6 = 0.63V$ (the overdrive) What is max CM Voltage?

Example

“Resistor current source” example



$R_D = 3.16K\Omega$

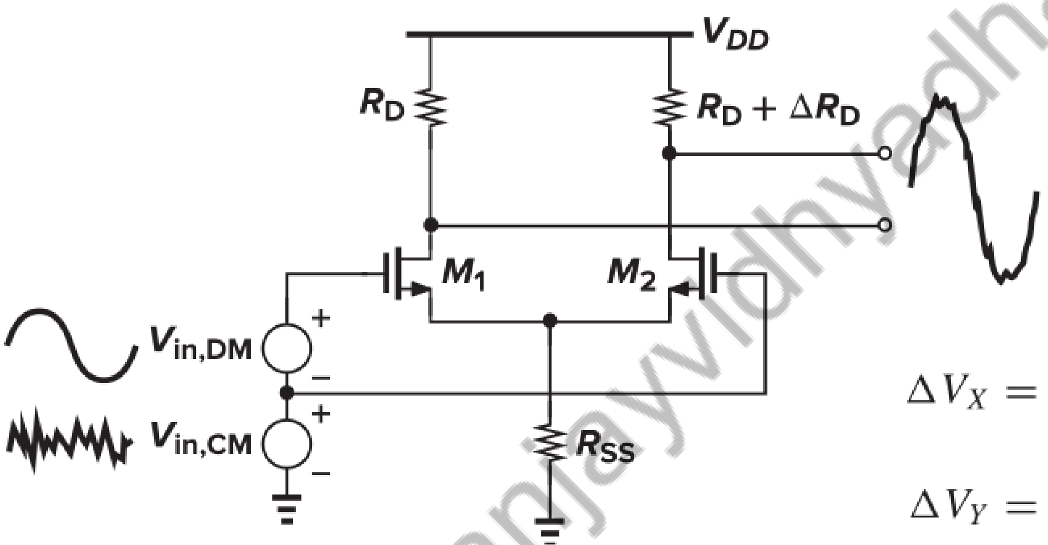
$$A_{V,CM} = \frac{\Delta V_{out}}{\Delta V_{in,CM}} = -\frac{R_D / 2}{1/(2g_m) + R_{SS}}$$

Large CM gain of 1.94 is due to the small R_{SS}

CMRR = 5 / 1.94 = 51.7

Common-Mode Response

Common-mode response in the presence of resistor mismatch.



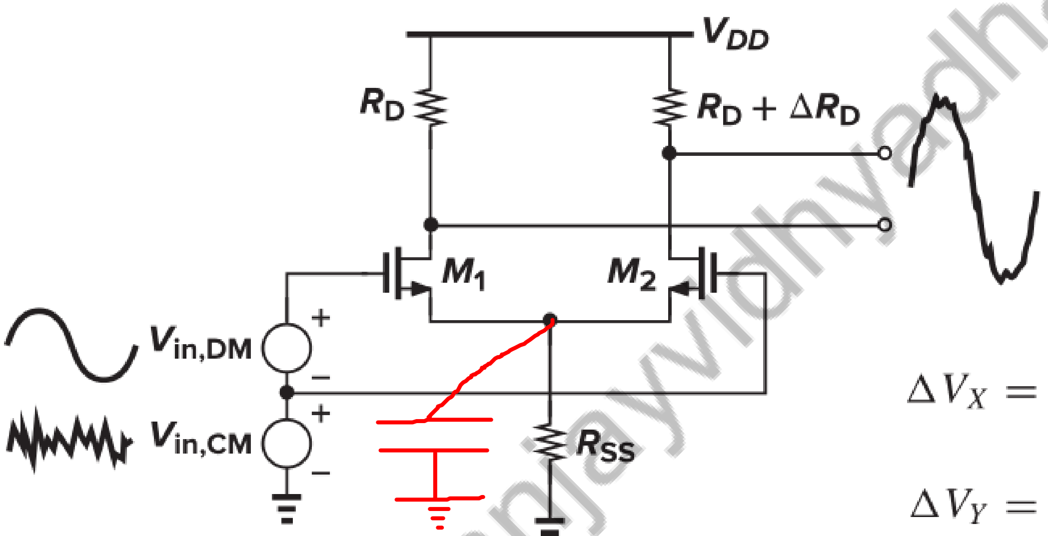
$$\Delta V_X = -\Delta V_{in,CM} \frac{g_m}{1 + 2g_m R_{SS}} R_D$$

$$\Delta V_Y = -\Delta V_{in,CM} \frac{g_m}{1 + 2g_m R_{SS}} (R_D + \Delta R_D)$$

R_{SS} should be large for Noise immunity .

Common-Mode Response

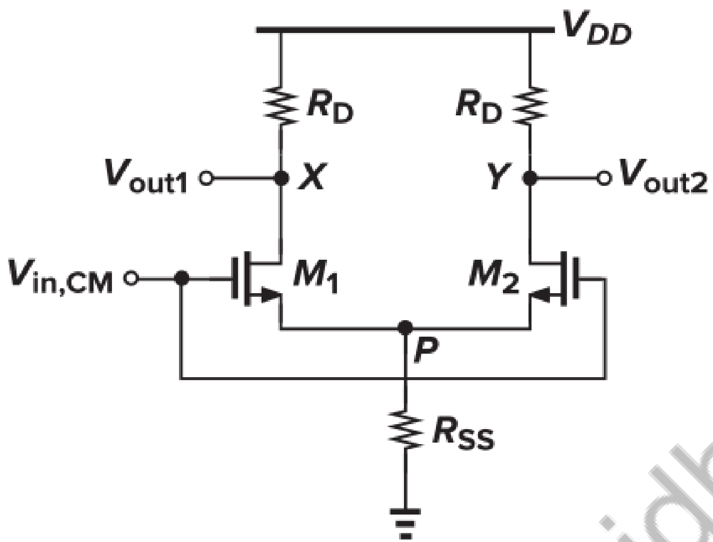
CM response with finite tail capacitance.

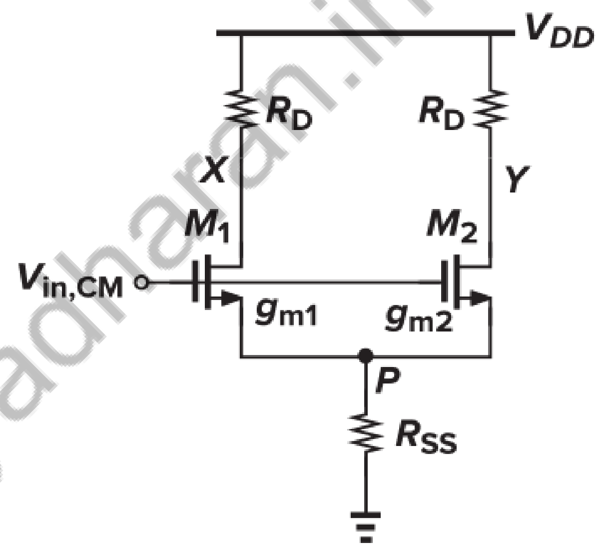


$$\Delta V_X = -\Delta V_{in,CM} \frac{g_m}{1 + 2g_m R_{SS}} R_D$$

$$\Delta V_Y = -\Delta V_{in,CM} \frac{g_m}{1 + 2g_m R_{SS}} (R_D + \Delta R_D)$$

Common-Mode Response





$$V_X = -g_{m1}(V_{in,CM} - V_P)R_D = \frac{-g_{m1}}{(g_{m1}+g_{m2})R_{SS}+1}R_D V_{in,CM}$$

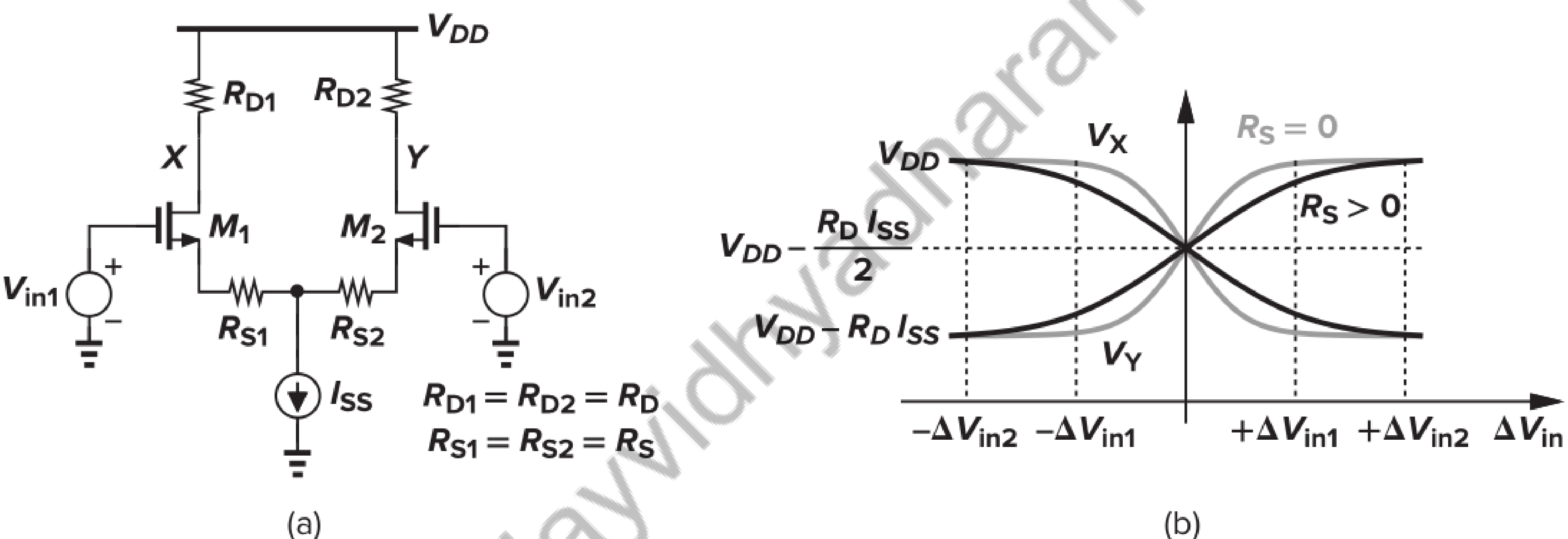
$$V_Y = -g_{m2}(V_{in,CM} - V_P)R_D = \frac{-g_{m2}}{(g_{m1}+g_{m2})R_{SS}+1}R_D V_{in,CM}$$

$$V_X - V_Y = -\frac{g_{m1}-g_{m2}}{(g_{m1}+g_{m2})R_{SS}+1}R_D V_{in,CM}$$

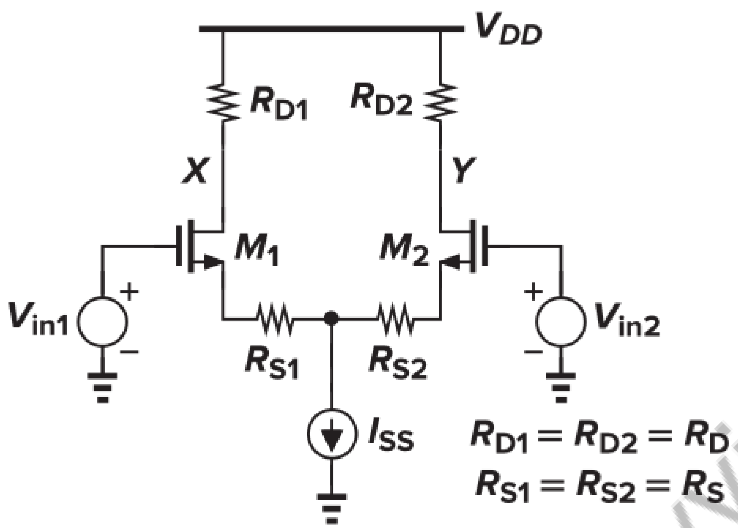
$$A_{CM-DM} = -\frac{\Delta g_m R_D}{(g_{m1}+g_{m2})R_{SS}+1}$$

A CM−DM denotes common-mode to differential-mode conversion

Degenerated Differential Pairs



Degenerated Differential Pairs



(a)

$$V_{in1} - V_{GS1} - R_S I_{SS} = V_{in2} - V_{TH}$$

$$V_{in1} - V_{in2} = V_{GS1} - V_{TH} + R_S I_{SS}$$

$$= \sqrt{\frac{2I_{SS}}{\mu_n C_{ox}\frac{W}{L}}} + R_S I_{SS}$$

$$\Delta V_{in2} - \Delta V_{in1} = R_S I_{SS}$$

Guess the Drawback

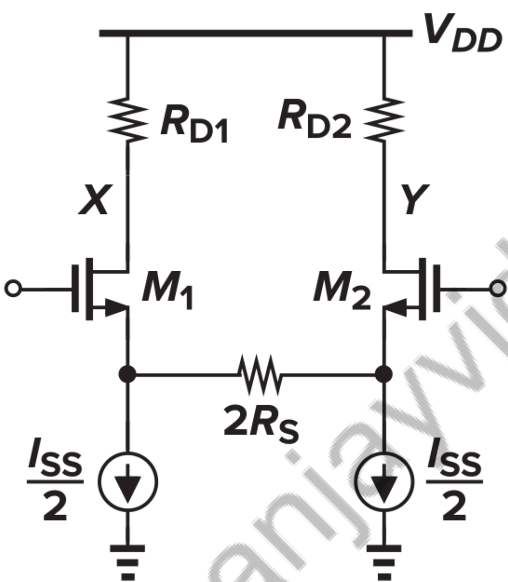
$$|A_v| = \frac{R_D}{\frac{1}{g_m} + R_S}$$

Trades gain for linearity

Each resistor sustains a voltage drop of $R_S I_{SS}/2$

Degenerated Differential Pairs

Degenerated differential pair with split tail current source.



Thank you