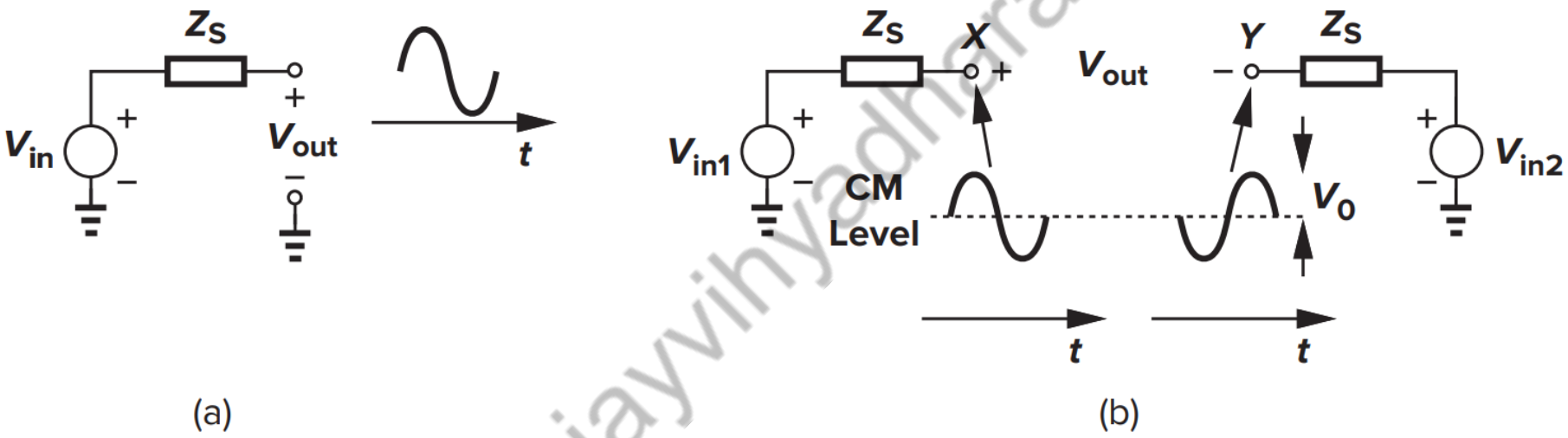
Analog IC Design : 2022-23
Lecture 4
Differential Amplifiers Part-1

By Dr. Sanjay Vidhyadharan

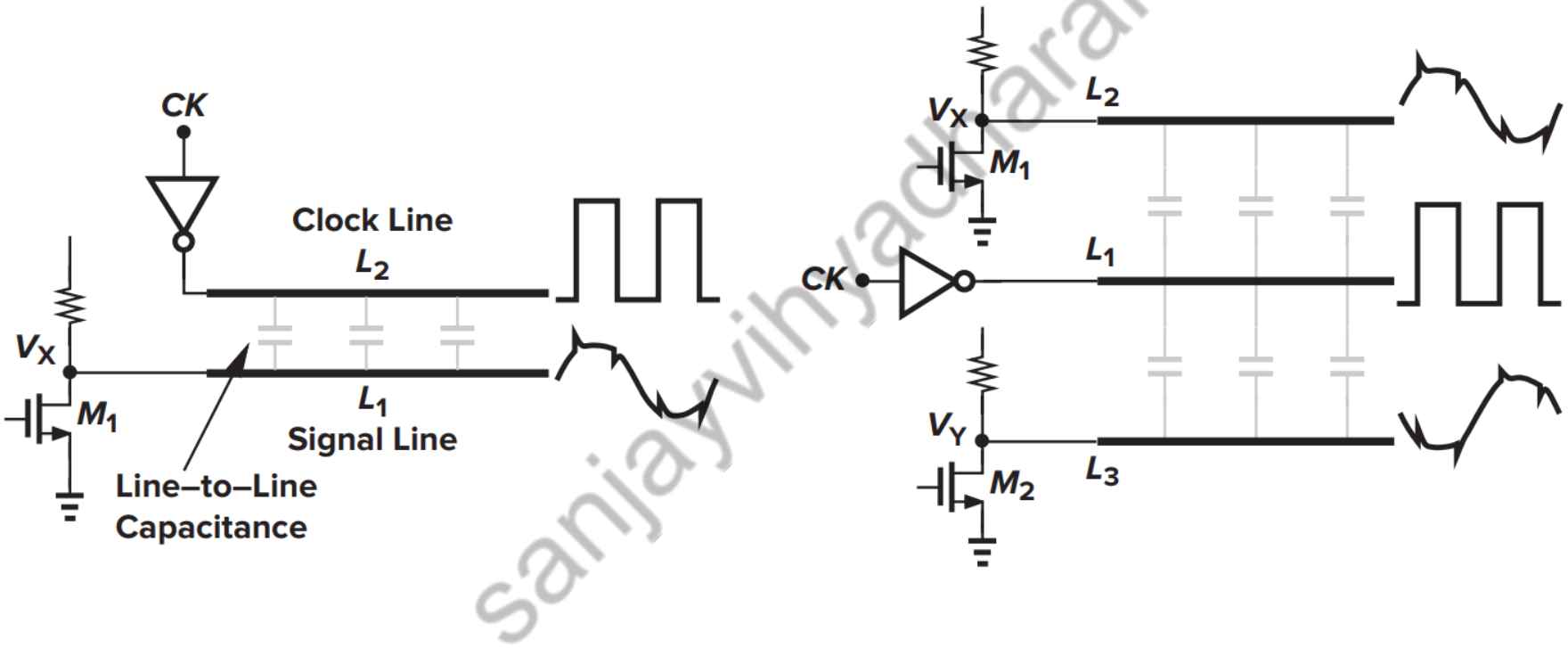
Single-Ended and Differential Operation



(a) Single-ended and (b) differential signals.

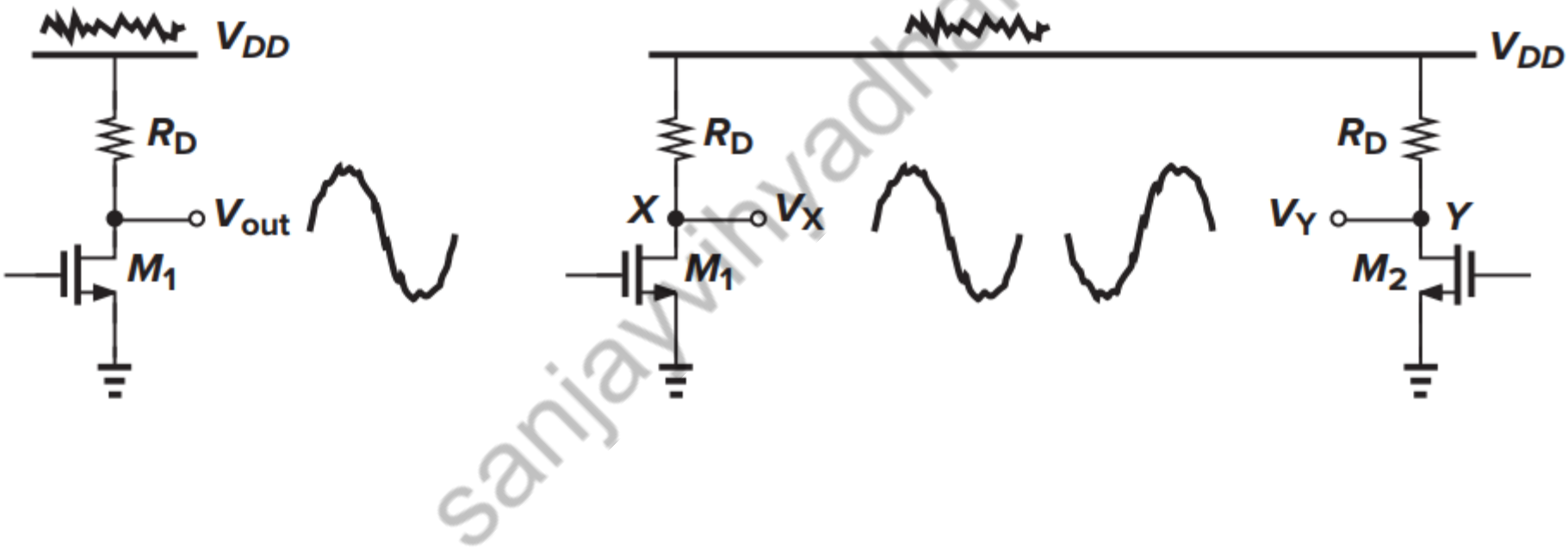
Advantages of Differential Signals

Transmission Line Noise Cancellation

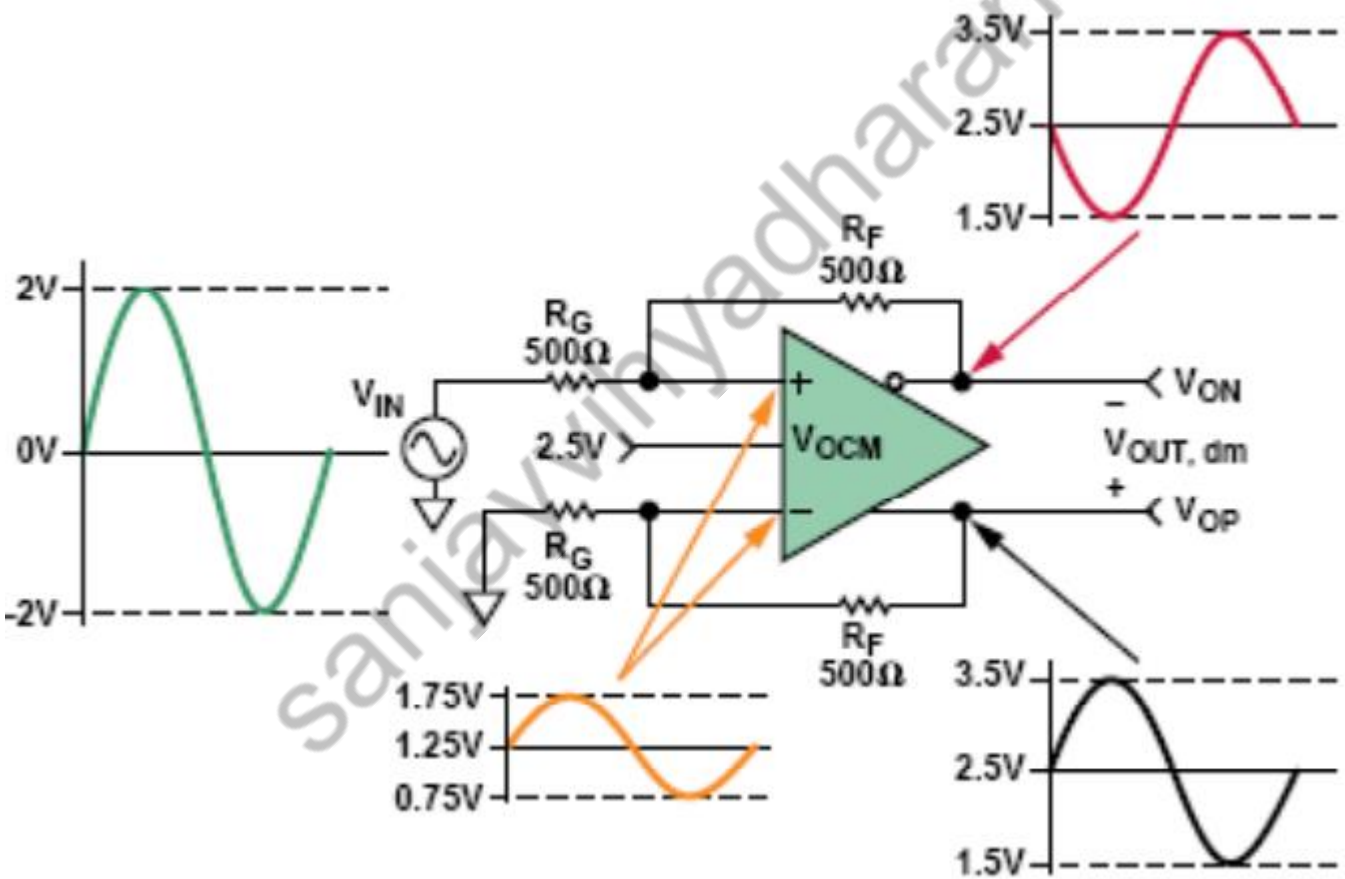


Advantages of Differential Signals

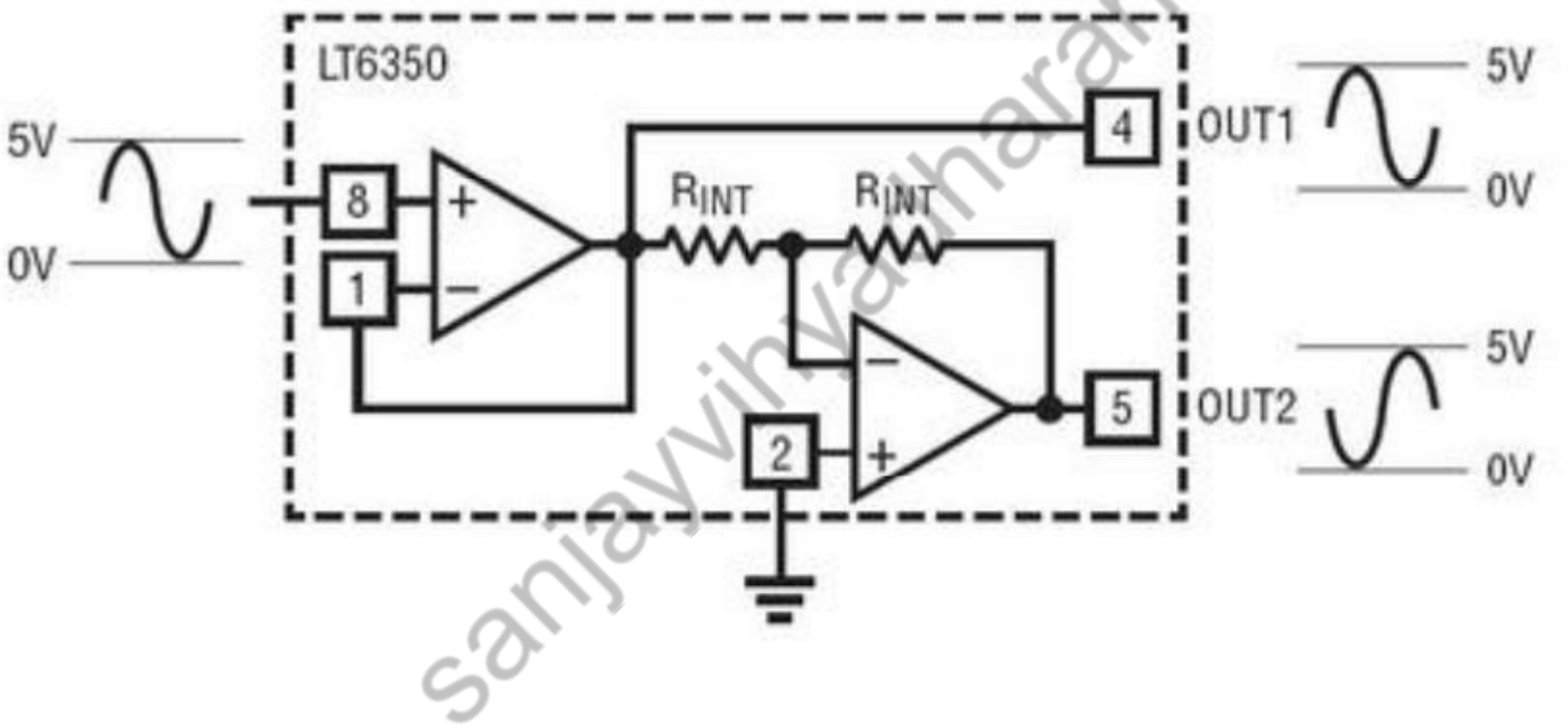
Power Supply Noise Cancellation



Converting Single Input to Differential



Converting Single Input to Differential



Differential Amplifier Definitions

- Common mode rejection rato (*CMRR*)

$$CMRR = \left|\frac{A_{VD}}{A_{VC}}\right|$$

CMRR is a measure of how well the differential amplifier rejects the common-mode input voltage in favor of the differential-input voltage.

- Input common-mode range (*ICMR*)

The input common-mode range is the range of common-mode voltages over which the differential amplifier continues to sense and amplify the difference signal with the same gain.

Typically, the *ICMR* is defined by the common-mode voltage range over which all MOSFETs remain in the saturation region.

- Output offset voltage (V_{OS}(out))

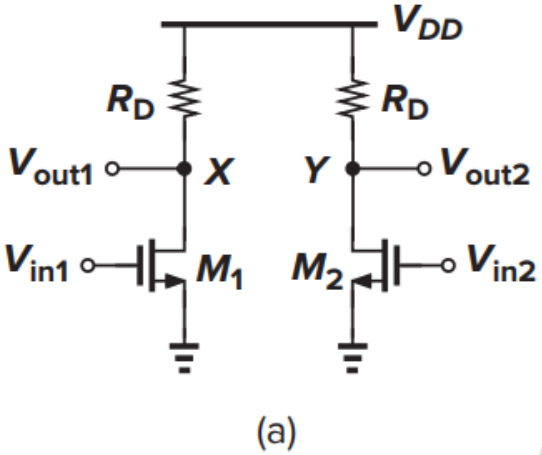
The output offset voltage is the voltage which appears at the output of the differential amplifier when the input terminals are connected together.

- Input offset voltage (V_{OS}(in) = V_{OS})

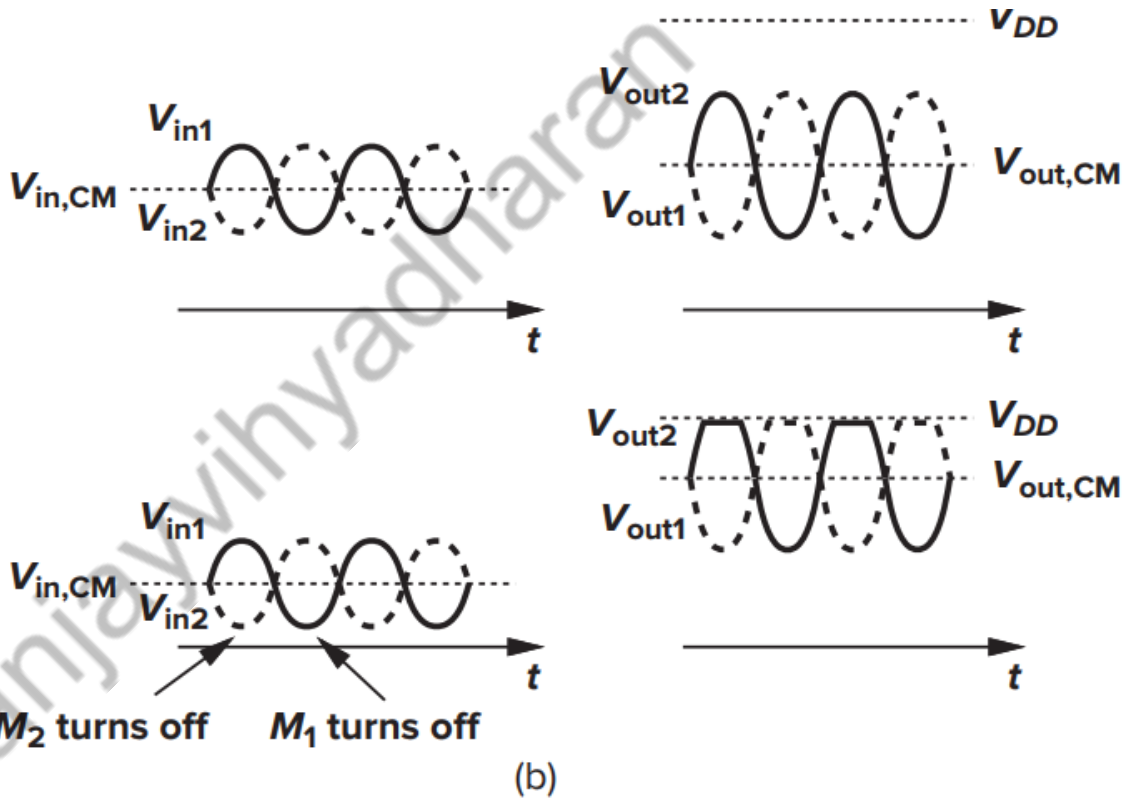
The input offset voltage is equal to the output offset voltage divided by the differential voltage gain.

$$V_{OS} = \frac{V_{OS}(\text{out})}{A_{VD}}$$

Simple Differential Circuit

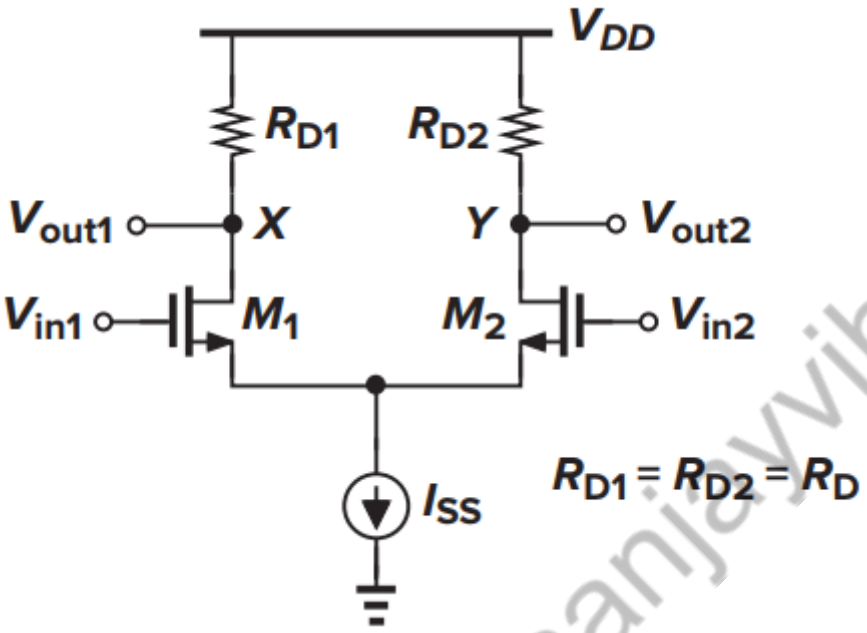


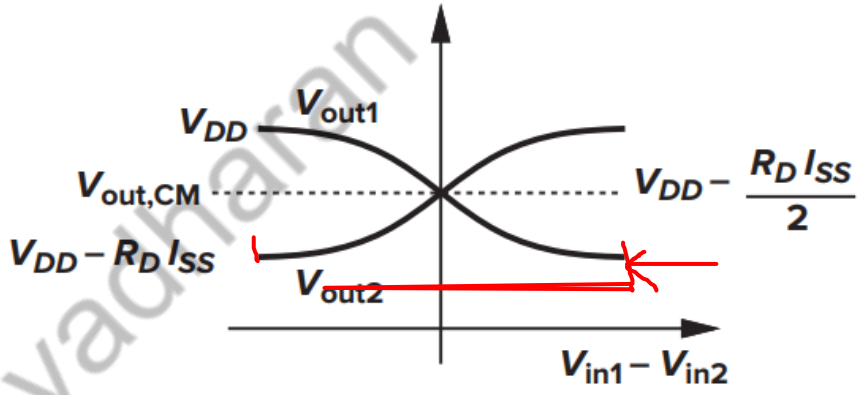
(a)

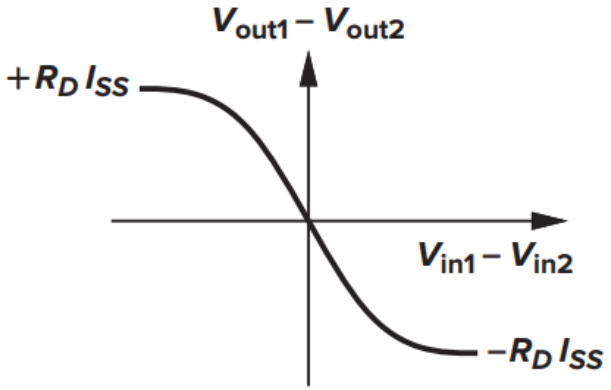


(b)

Basic MOS Differential Pair







"Current stealing " phenomenon

MOSFET Current Equation

$$k_n' = \mu_{nC_{ox}}$$

$$I_D = \frac{k_n' W (V_{GS} - V_T)^2}{2L}$$

$$k_n = k_n' (W/L)$$

$$k_n = (\mu_n C_{ox}) (W/L)$$

$$\beta = \tfrac{1}{2}\mu \cdot Cox \cdot \frac{W}{L}$$

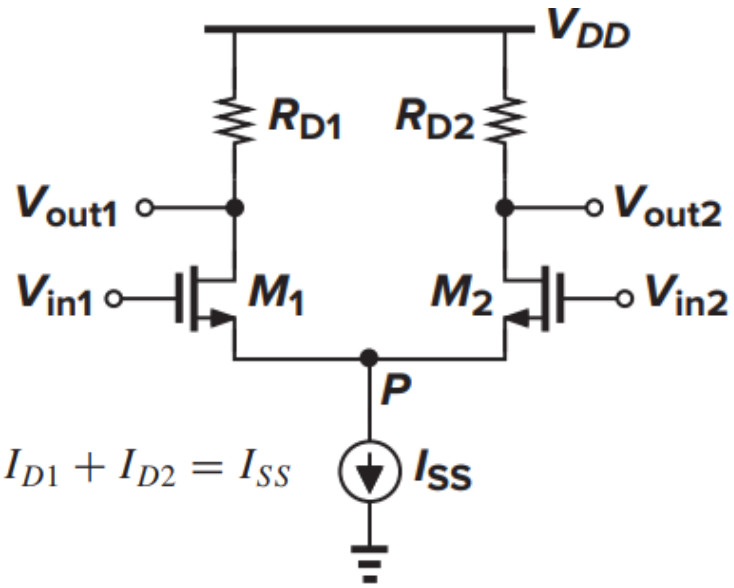
$$I_D = \boldsymbol{\beta} (V_{GS} - V_T)^2$$

$$I_D = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)(V_{GS} - V_{tn})^2$$

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(v_{GS} - V_t)^2$$

$$i_D - \frac{1}{2}k_n'\left(\frac{W}{L}\right)v_{OV}^2$$

MOS Differential Pair



$$I_{D1} + I_{D2} = I_{SS}$$

$$(V_{GS} - V_{TH})^2 = \frac{I_D}{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}}$$

$$V_{GS} = \sqrt{\frac{2I_D}{\mu_n C_{ox}\frac{W}{L}}} + V_{TH}$$

$$V_{in1} - V_{in2} = \sqrt{\frac{2I_{D1}}{\mu_n C_{ox}\frac{W}{L}}} - \sqrt{\frac{2I_{D2}}{\mu_n C_{ox}\frac{W}{L}}}$$

$$(V_{in1} - V_{in2})^2 = \frac{2}{\mu_n C_{ox}\frac{W}{L}}(I_{SS} - 2\sqrt{I_{D1}I_{D2}})$$

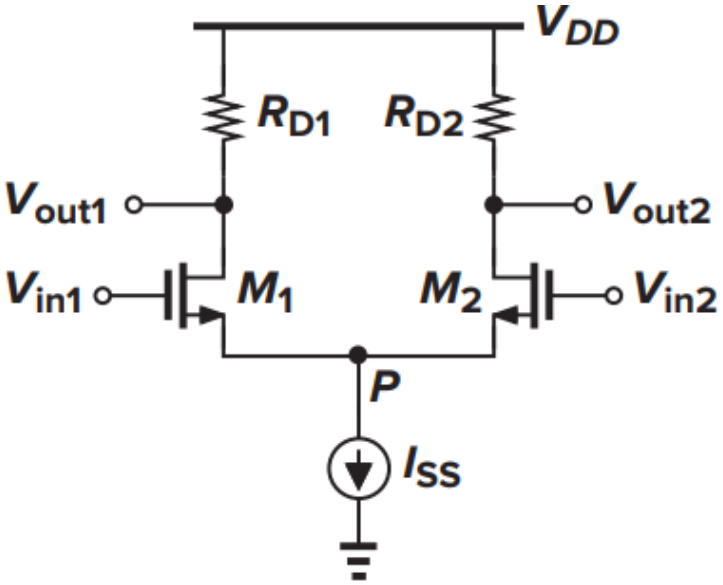
$$\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in1} - V_{in2})^2 - I_{SS} = -2\sqrt{I_{D1}I_{D2}}$$

$$4I_{D1}I_{D2} = (I_{D1}+I_{D2})^2 - (I_{D1}-I_{D2})^2 = I_{SS}^2 - (I_{D1}-I_{D2})^2,$$

$$(I_{D1} - I_{D2})^2 = \frac{1}{4}\left(\mu_n C_{ox}\frac{W}{L}\right)^2 (V_{in1} - V_{in2})^4 + I_{SS}\mu_n C_{ox}\frac{W}{L}(V_{in1} - V_{in2})^2$$

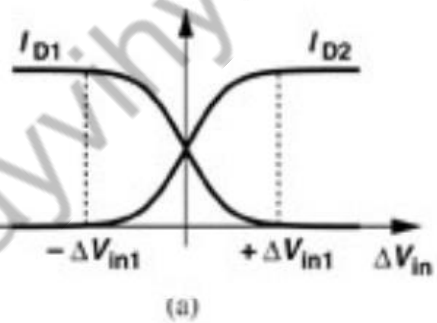
$$I_{D1} - I_{D2} = \frac{1}{2}\mu_n C_{OX}\frac{W}{L}(V_{in1} - V_{in2})\sqrt{\frac{4I_{SS}}{\mu_n C_{OX}\frac{W}{L}} - (V_{in1} - V_{in2})^2}$$

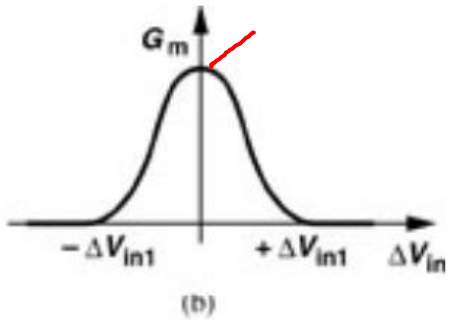
MOS Differential Pair



Differential Transconductance Gain vs. Input Voltage

$$\frac{\partial \Delta I_D}{\partial \Delta V_{in}} = G_m = \frac{\mu_n C_{ox}}{2}\frac{W}{L}\frac{\frac{4I_{SS}}{\mu_n C_{ox} W/L} - 2(V_{in1}-V_{in2})^2}{\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - (V_{in1}-V_{in2})^2}}$$



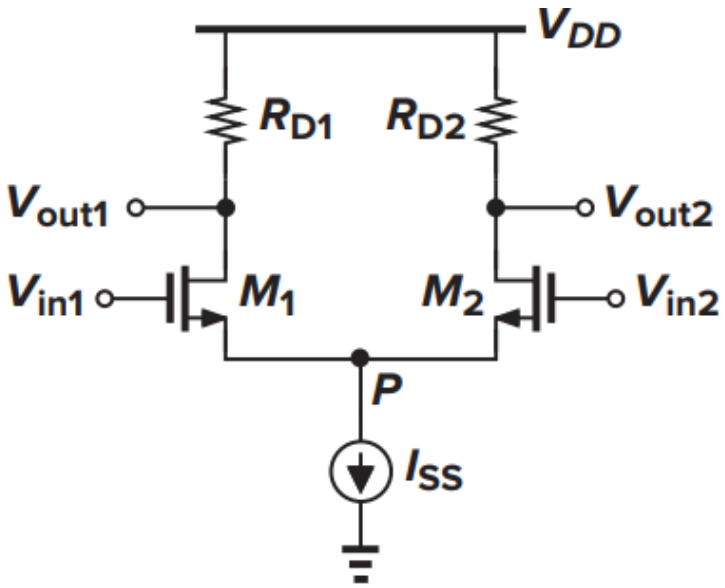


Maximum Differential Transconductance Gain Occurs at ΔVin=0

$$g_m = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)I_D}$$

$$G_{m,\max} = \sqrt{\mu_n C_{ox}\left(\frac{W}{L}\right)I_{SS}}$$

MOS Differential Pair



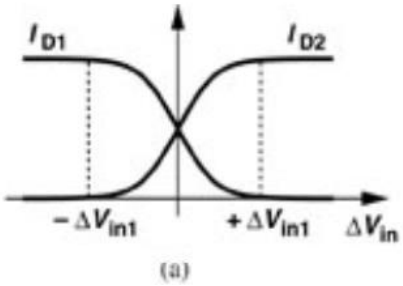
Differential Voltage Gain

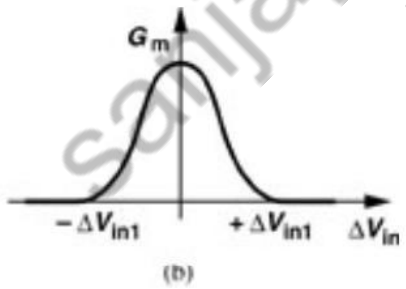
$$V_{out1} - V_{out2} = R_D \Delta I_D = R_D G_m \Delta V_{in}$$

Differential Voltage Gain near $\Delta V_{in} = 0$

$$|A_V| = \frac{\Delta V_{out}}{\Delta V_{in}} = G_{m,\max} R_D = \sqrt{\mu_n C_{ox} \frac{W}{L} I_{SS}}\, R_D$$

Differential Transconductance Gain Falls to Zero at $\Delta V_{in} = \Delta V_{in1}$





$$\frac{\partial \Delta I_D}{\partial \Delta V_{in}} = G_m = \frac{\mu_n C_{ox}}{2} \frac{W}{L} \frac{\frac{4I_{SS}}{\mu_n C_{ox} W/L} - 2(V_{in1} - V_{in2})^2}{\sqrt{\frac{4I_{SS}}{\mu_n C_{ox} \frac{W}{L}} - (V_{in1} - V_{in2})^2}}$$

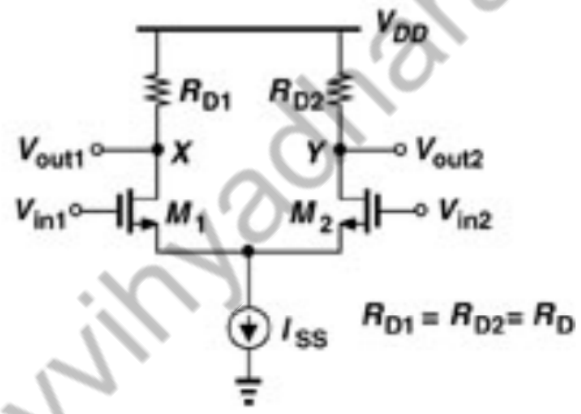
$$\Delta V_{in1} = \sqrt{\frac{2I_{SS}}{\mu_n C_{ox} \frac{W}{L}}}$$

$\Delta V_{in} = \Delta V_{in1}$ is the maximum differential input that the amplifier can "handle"

MOS Differential Pair

Two types of Differential Gains

"Single-ended": V_{out1} (or V_{out2}) with respect to ground.

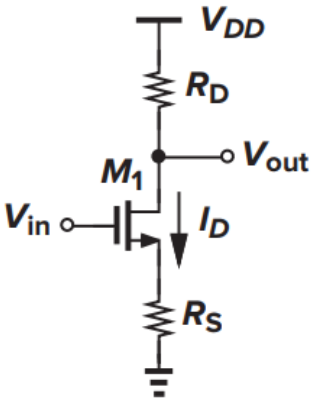


$$A_v(diff) = \frac{V_{out1} - V_{out2}}{V_{in1} - V_{in2}} = ?$$

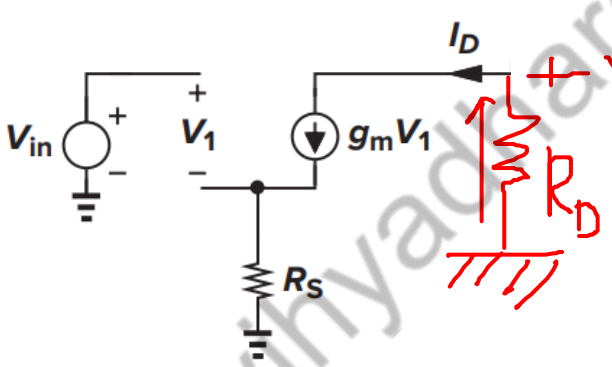
$$A_v(S.E.) = \frac{V_{out1}}{V_{in1} - V_{in2}} = ?$$

CS Amplifier

CS stage with source degeneration.



(a)



(b)

$$v_{in} = v_{gs+}\, i_d\, R_s$$

$$v_{in} = v_{gs+}\, g_m\, v_{gs}\, R_s$$

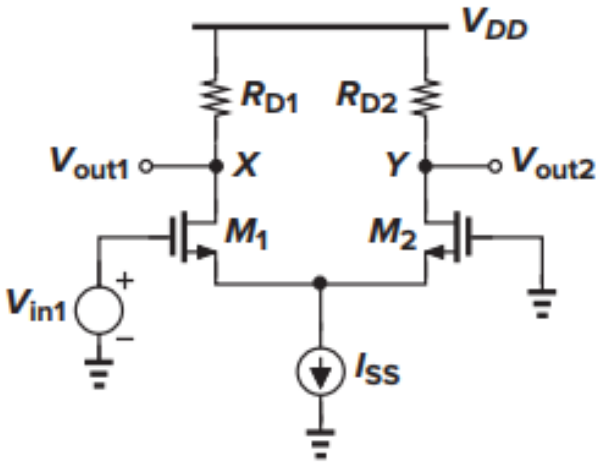
$$v_{in} = v_{gs}\ (1 + g_m\, R_s)$$

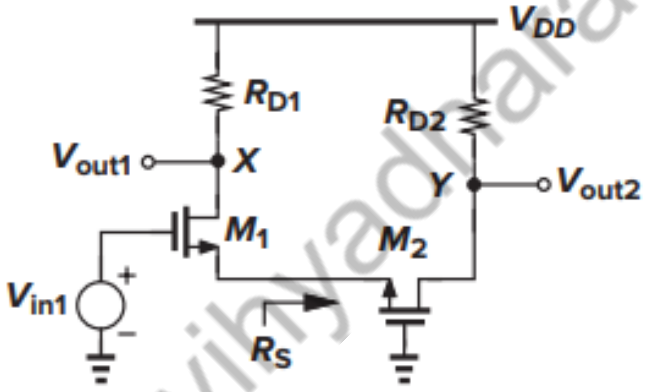
$$v_{out} = -i_d\, R_D$$

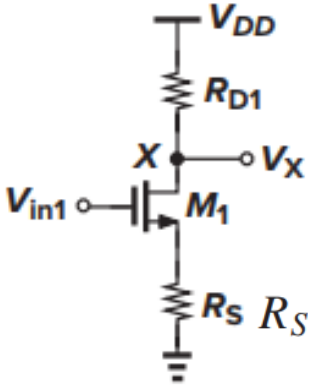
$$v_{out} = -v_{gs}\ \ g_m\, R_D$$

$$Gain = \frac{-g_m\, R_D}{1+g_m\, R_s} = \frac{-R_D}{\frac{1}{g_m}+R_s}$$

Differential Mode Response



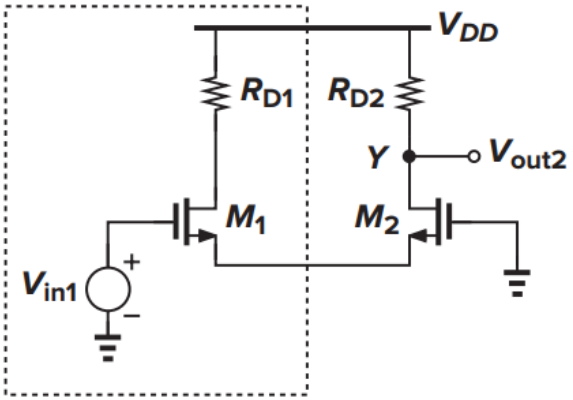


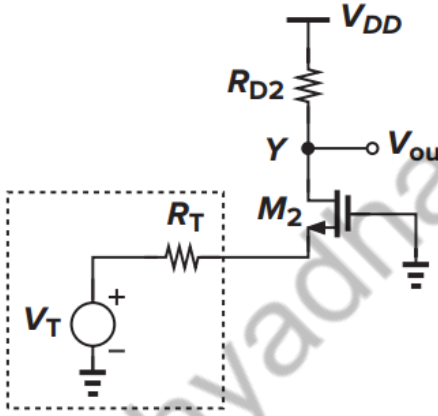


$R_S = 1/g_{m2}$

$$\frac{V_X}{V_{in1}} = \frac{-R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}}$$

Differential Mode Response





$$-v_{gs2} = \frac{-i_d}{g_{m1}} + v_{gs1}$$

$$\frac{i_d}{g_{m2}} = \frac{-i_d}{g_{m1}} + v_{gs1}$$

$$v_{gs1} = \frac{i_d}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}}$$

$$v_{out} = i_d R_{D2}$$

$$(V_X - V_Y)|_{\text{Due to } Vin1} = \frac{-2R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}} V_{in1}$$

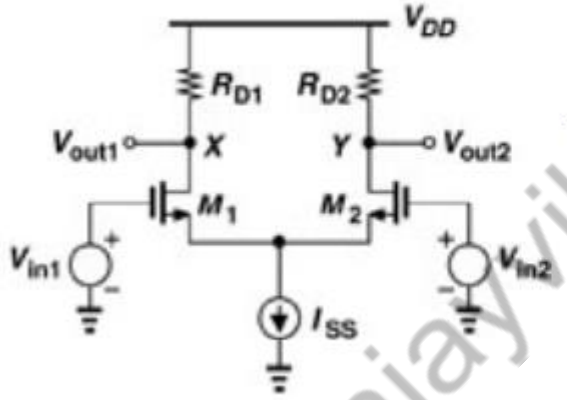
$$\frac{V_Y}{V_{in1}} = \frac{R_D}{\frac{1}{g_{m2}} + \frac{1}{g_{m1}}}$$

$$(V_X - V_Y)|_{\text{Due to } Vin1} = -g_m R_D V_{in1}$$

$$\frac{(V_X - V_Y)_{tot}}{V_{in1} - V_{in2}} = -g_m R_D$$

Differential Mode Response

Single-ended Differential Voltage Gain



$$A_{V,SE} = \frac{V_X}{V_{in1} - V_{in2}} = -\frac{g_m}{2} R_D$$

$$A_{V,SE} = \frac{V_Y}{V_{in1} - V_{in2}} = \frac{g_m}{2} R_D$$

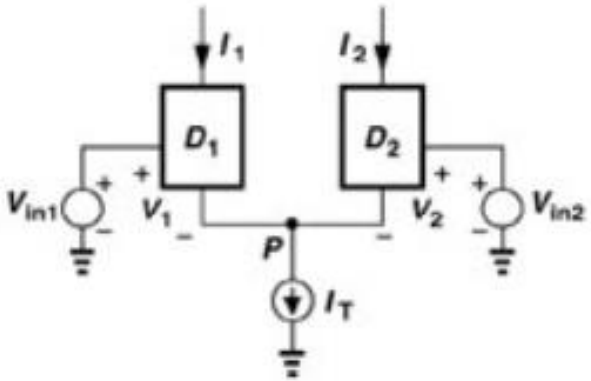
Differential Mode Response

Comparison: Differential voltage gain of a differential amplifier vs voltage gain of a CS amplifier

- If the same current source I_{SS} drives the differential amplifier and the CS, each transistor of the differential amplifier has g_m which is $1/\sqrt{2}$ of that of the CS transistor. Differential gain reduces by a factor of $1/\sqrt{2}$.

- If both amplifiers have the same W/L in each transistor and the same load, and we want the gain to be the same, then if we use I_{SS} at CS, we need to use $2I_{SS}$ at the differential amplifier.

The "Virtual Ground" Concept



$$V_p = V_{in2} + iR$$

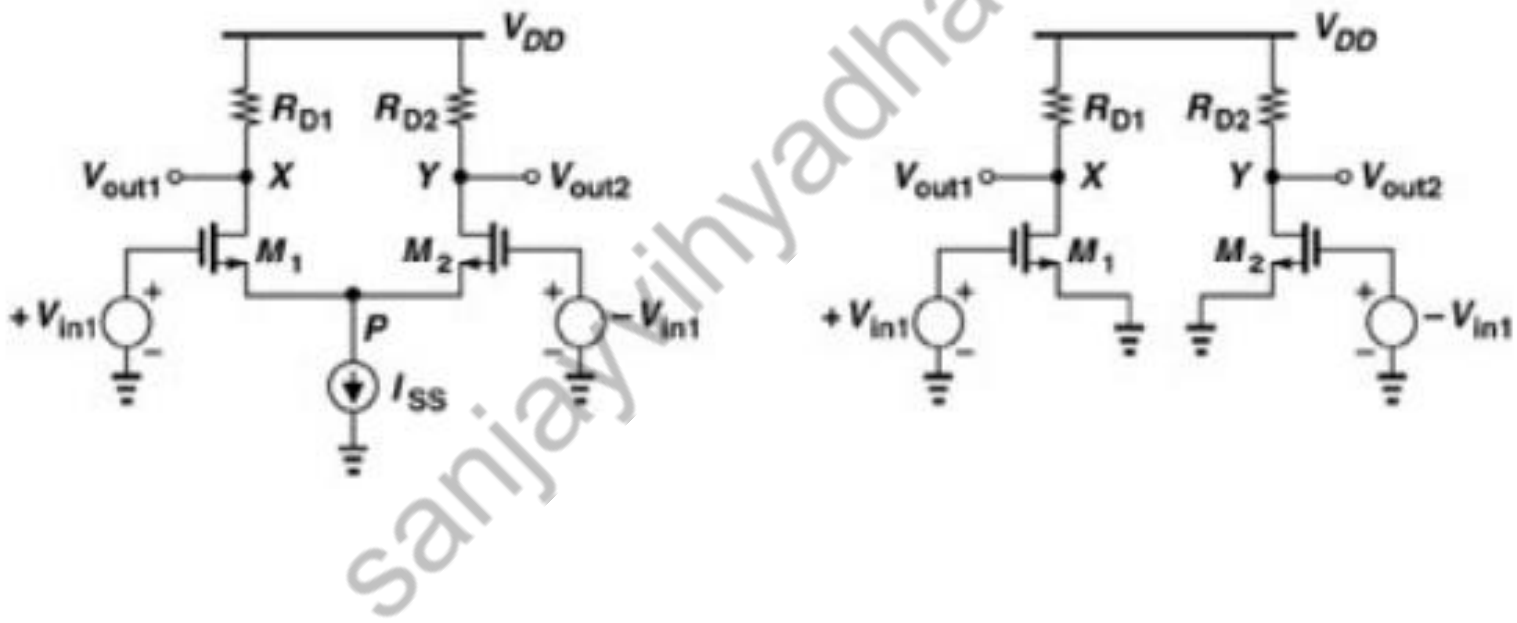
$$V_p = V_{in2} + \frac{V_{in1} - V_{in2}}{2R} R$$

$$V_p = \frac{V_{in1} + V_{in2}}{2}$$

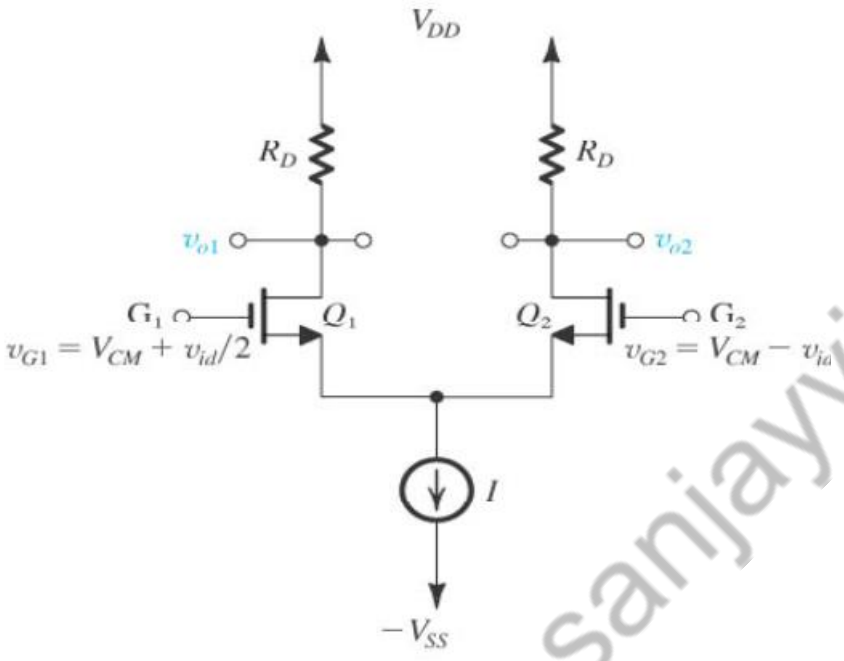
- In a symmetric device (as above), if inputs change anti-symmetrically (one goes up by a certain amount, and the other goes down by the same amount), then V_P does not change.
- For small-signal analysis point P becomes "virtual ground"

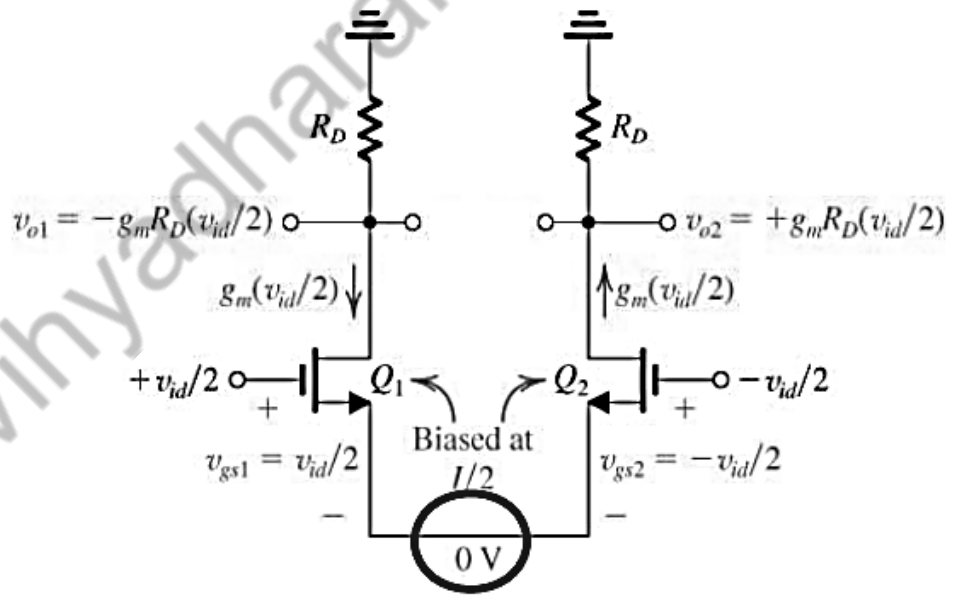
The “Virtual Ground” Concept

The “Half-Circuit” Concept



Differential Mode Response



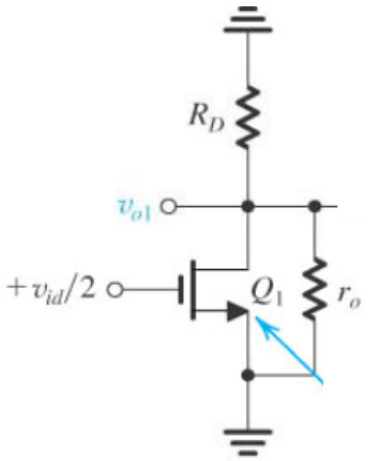


No voltage change since Left and Right are anti-symmetric (odd)

Gain = $-g_m R_D$

Differential Mode Response

Differential-mode small-signal half-circuit



$$\frac{v_{o1}}{v_{id}/2} = -g_m(R_D \| r_o)$$

For the total circuit

$$v_{od} = v_{o1} - v_{o2}$$

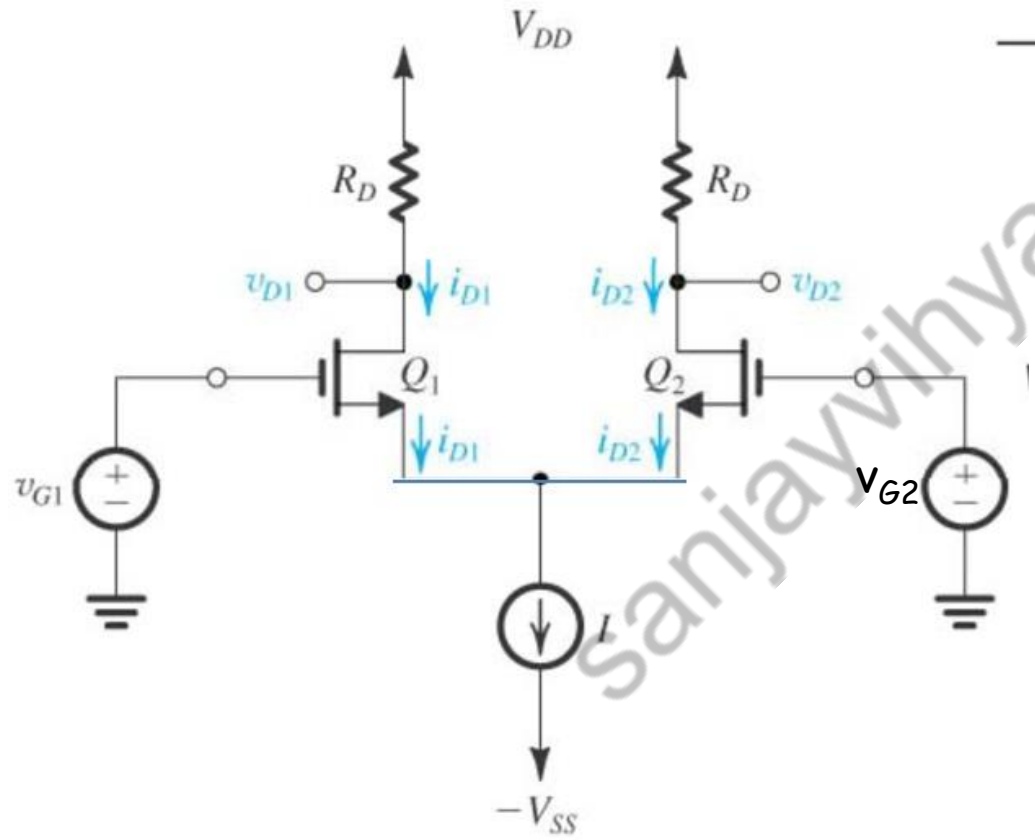
$$\text{But } v_{o2} = -v_{o1}$$

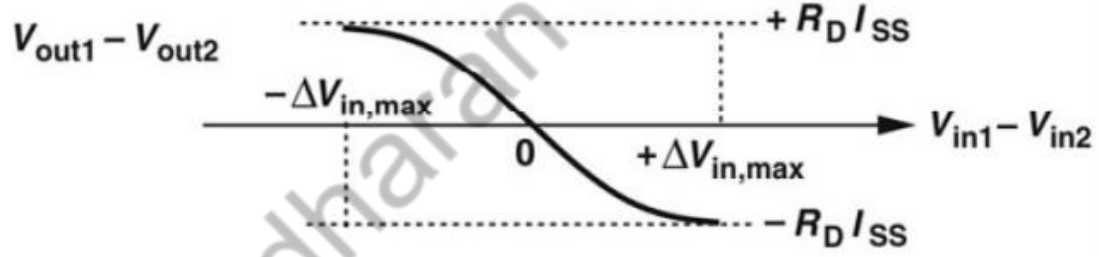
$$\therefore v_{od} = 2v_{o1}$$

CS amplifier for input difference!

$$A_d = \frac{v_{od}}{v_{id}} = \frac{2v_{o1}}{v_{id}} = -g_m(R_D \| r_o)$$

MOS Differential Pair





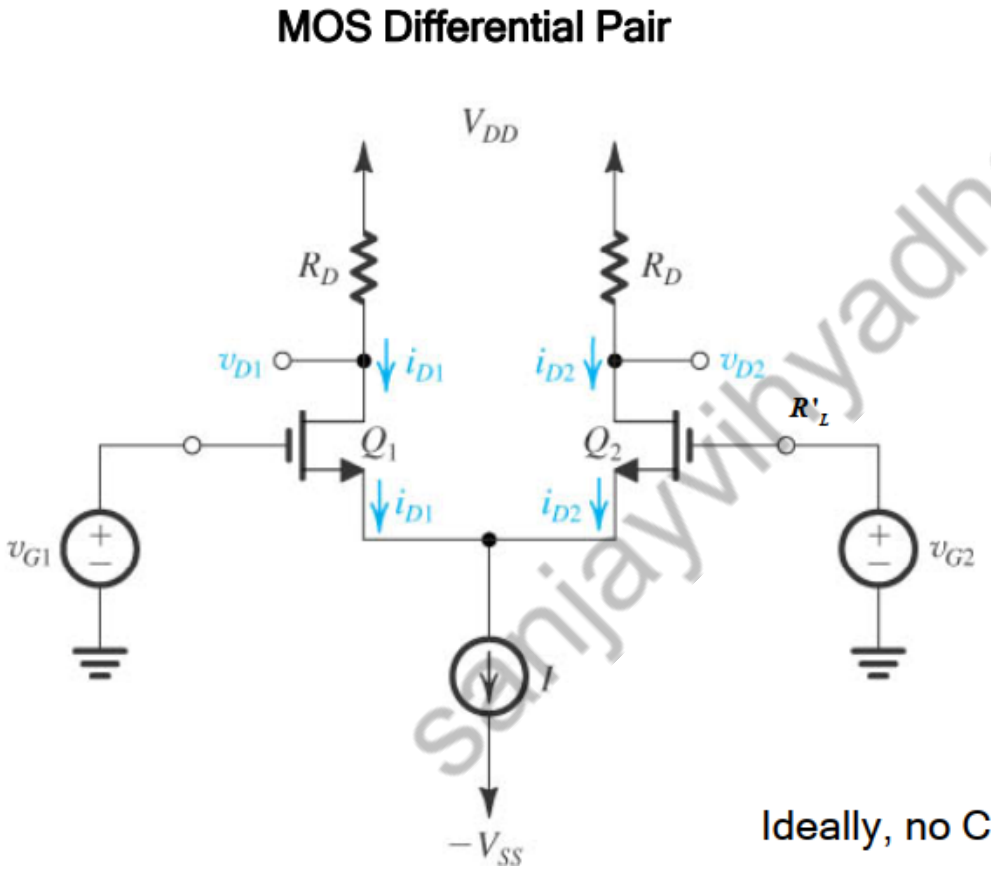
What is $\Delta v_{in,max}$?

$$v_{G1} = v_t + \sqrt{\frac{2I_{SS}}{k'_n \frac{W}{L}}}$$

$$v_{G2} = v_t$$

$$\Delta v_{in,max} = \sqrt{\frac{2I_{SS}}{k'_n \frac{W}{L}}}$$

MOS Differential Pair



V_{CM}: Common Mode

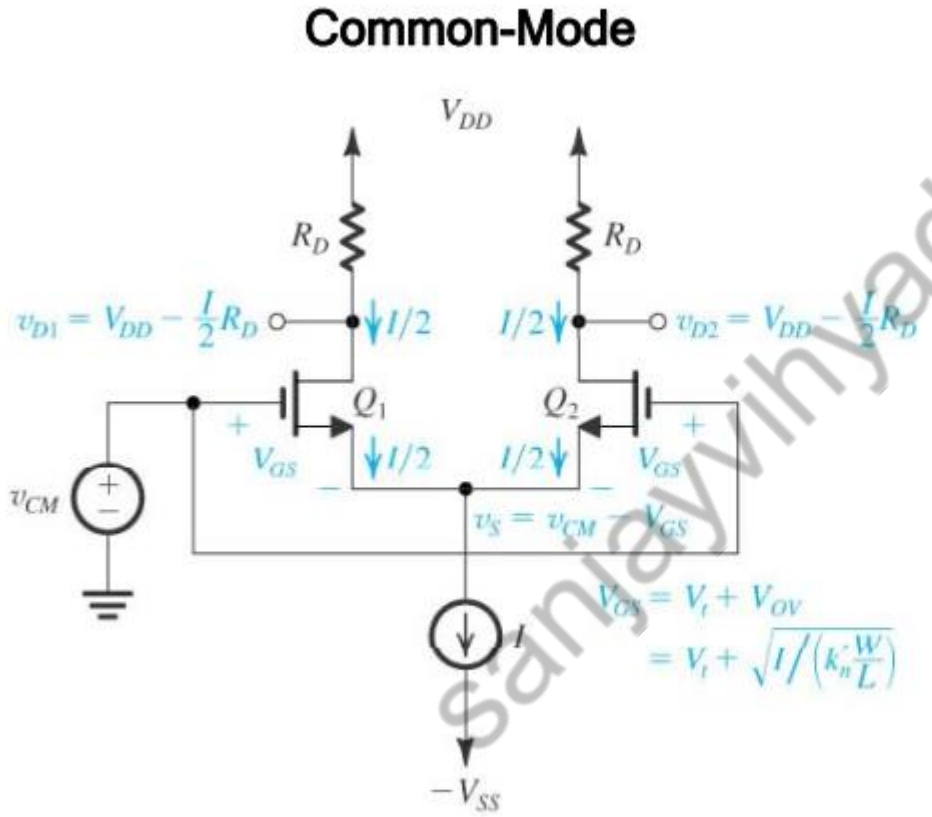
v_{id}: Differential Mode

$$v_{G1} = V_{CM} + \frac{v_{id}}{2}, \quad v_{G2} = V_{CM} - \frac{v_{id}}{2}$$

$$V_{CM} = \frac{v_{G1} + v_{G2}}{2}, \quad v_{id} = v_{G1} - v_{G2}$$

Ideally, no CM response, large DM response

MOS Differential Pair



For identical Q_1 and Q_2

$$i_{D1} = i_{D2} = \frac{I}{2}$$

$$v_{D1} = v_{D2} = V_{DD} - \frac{I}{2}R_D$$

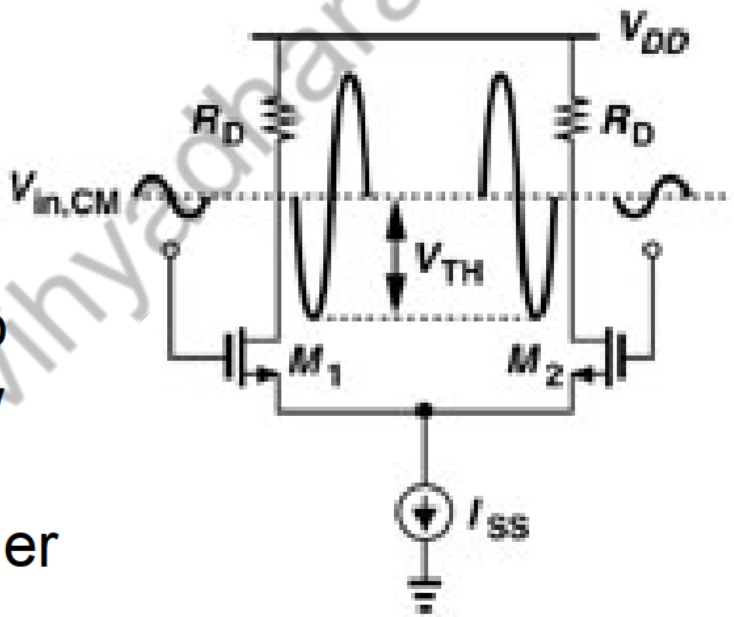
$$\therefore v_{D1} - v_{D2} = 0$$

==> No CM output

CMMR = ????

MOS Differential Pair

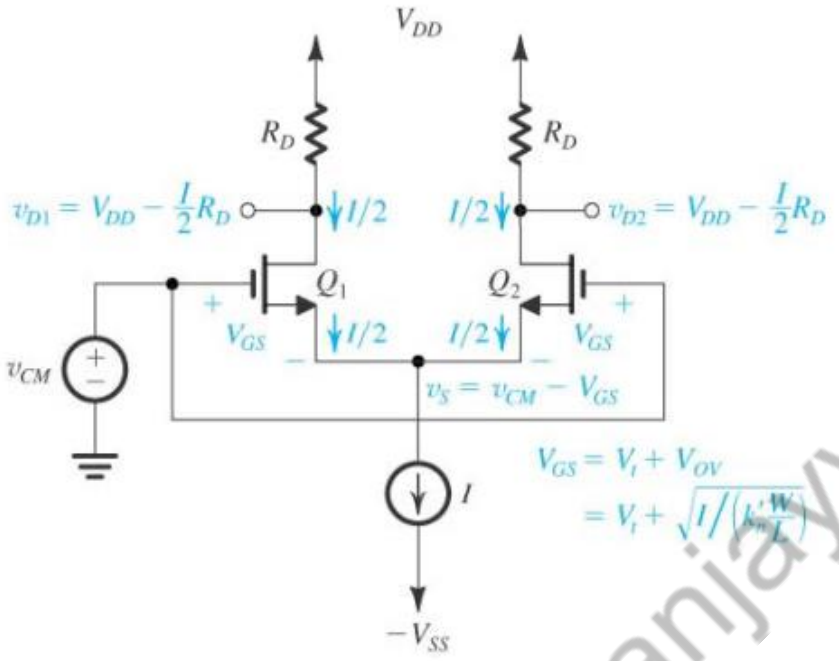
Common-Mode Input vs. Output Swing Tradeoff



Each drain voltage can go as high as V_{DD} and as low as $V_{in,CM}$-V_{TH}.
The larger $V_{in,CM}$ the smaller the swing.

MOS Differential Pair

Common-Mode



$V_{GS} = V_t + V_{OV}$

$= V_t + \sqrt{I/\left(k_n' \frac{W}{L}\right)}$

$V_{CM, max}$?

$$v_{DS} \geq v_{GS} - V_t$$

$$(V_{DD} - \frac{I}{2}R_D) - (V_{CM} - v_{GS}) \geq v_{GS} - V_t$$

$$\therefore V_{DD} - \frac{I}{2}R_D + V_t \geq V_{CM}$$

$$V_{CM,\max} = V_{DD} - \frac{I}{2}R_D + V_t$$

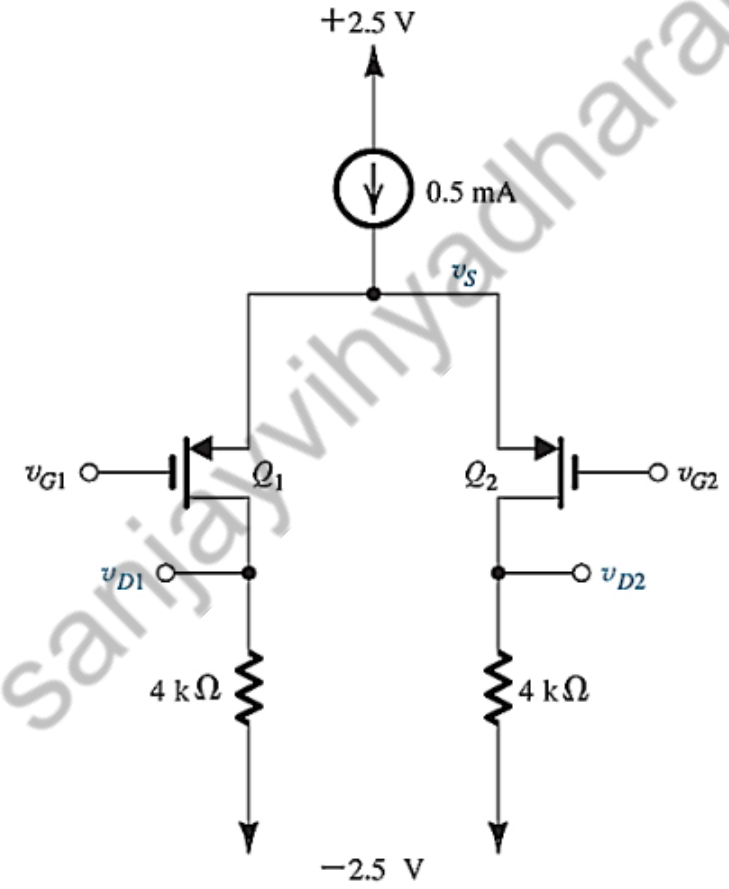
How to Maximise ?

If a voltage V_{CS} is needed across the current source, then

$V_{CMmin} = -V_{SS} + V_{CS} + V_t + V_{OV}$

How to Minimise ?

PMOS Differential Pair



Thank you