VLSI Design : 2022-23
Lecture 4
CMOS Inverter Static Characteristics

By Dr. Sanjay Vidhyadharan

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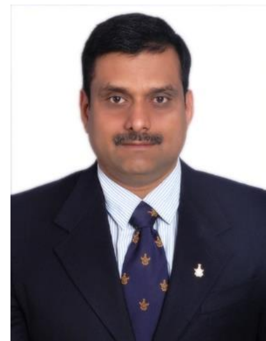
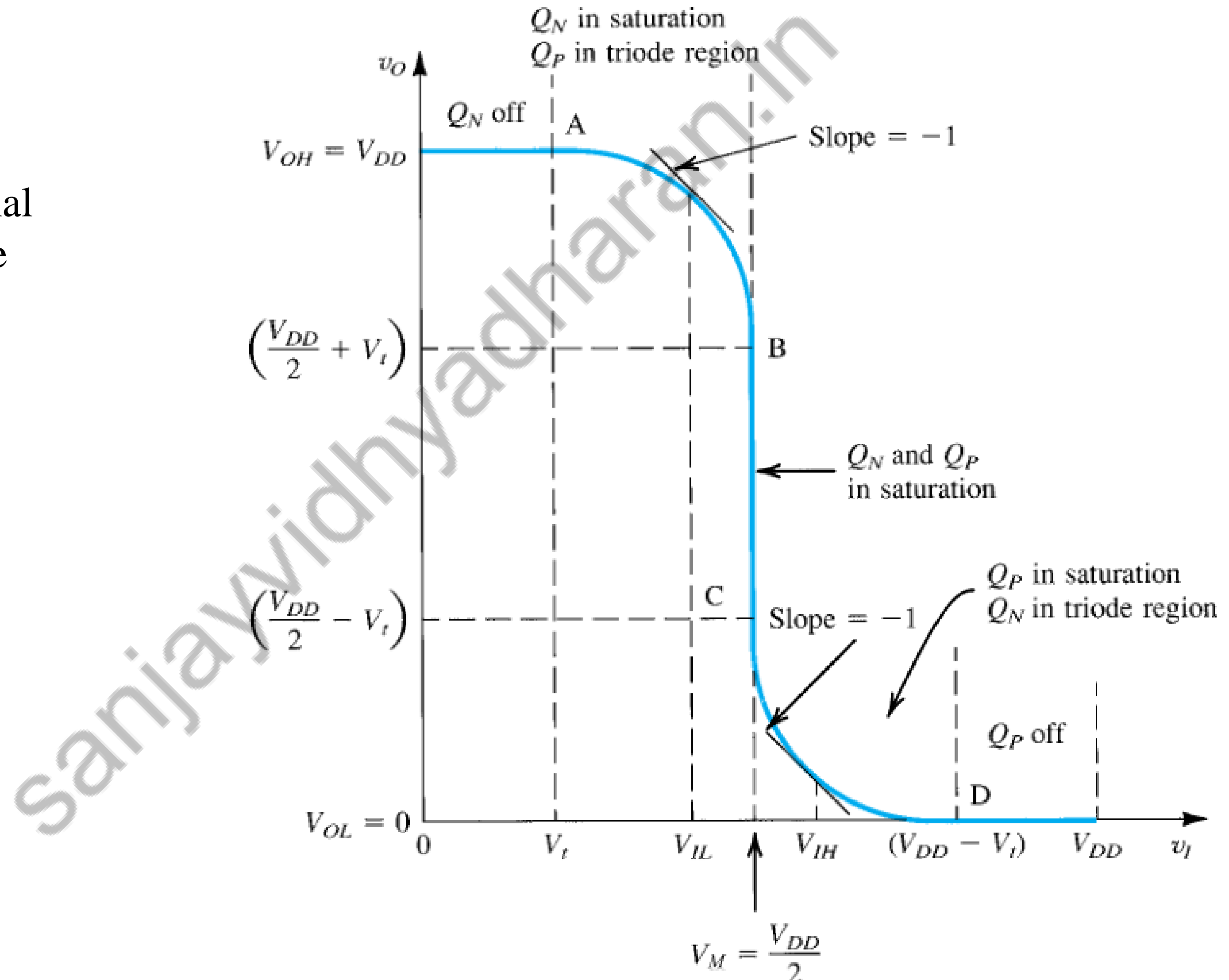


Noise Margin

For MOSFET Inverters

V_{IH} , V_{IL} are operational points of inverter where dVout /dVin = -1



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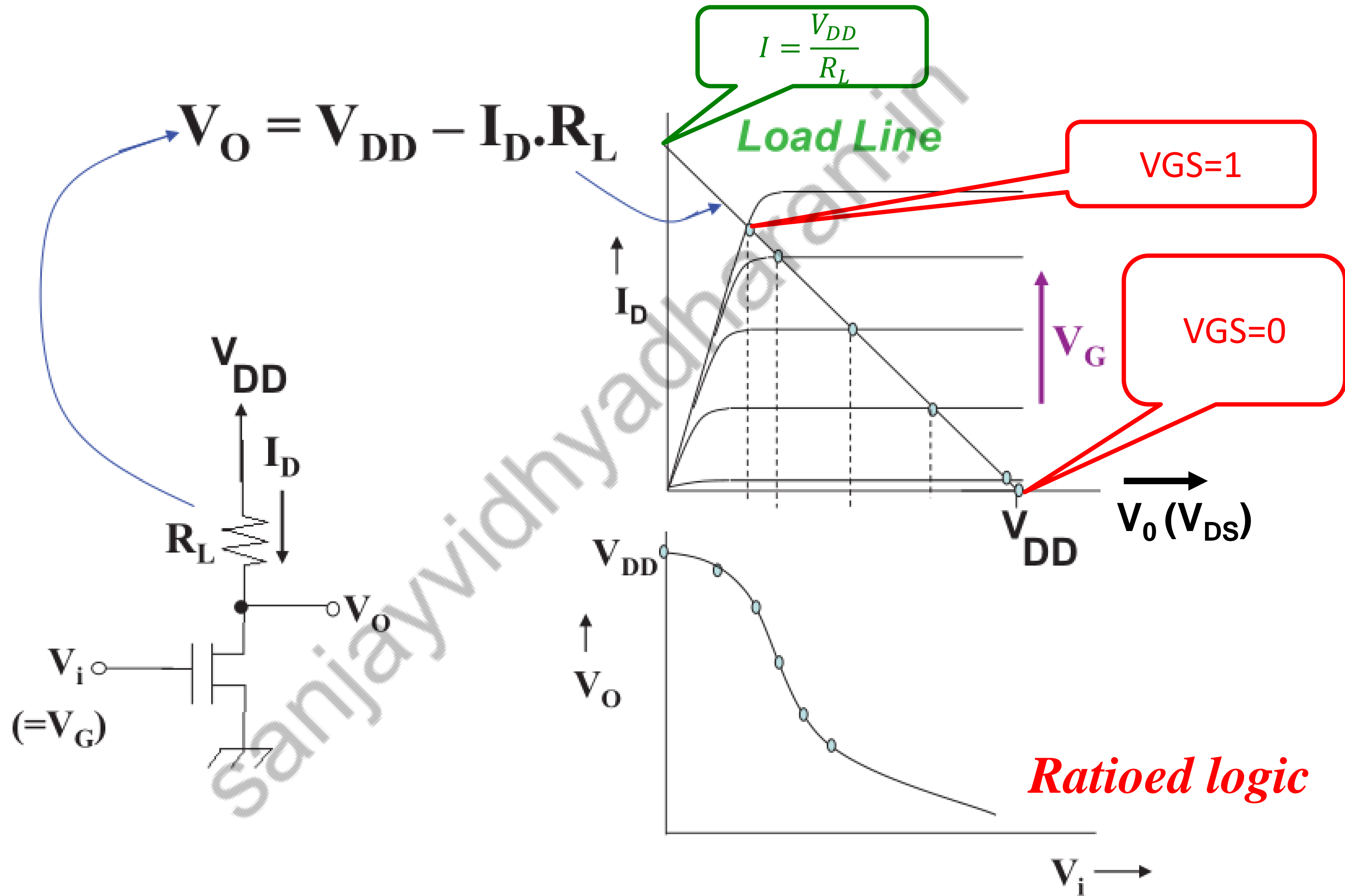
Resistive Load Inverter



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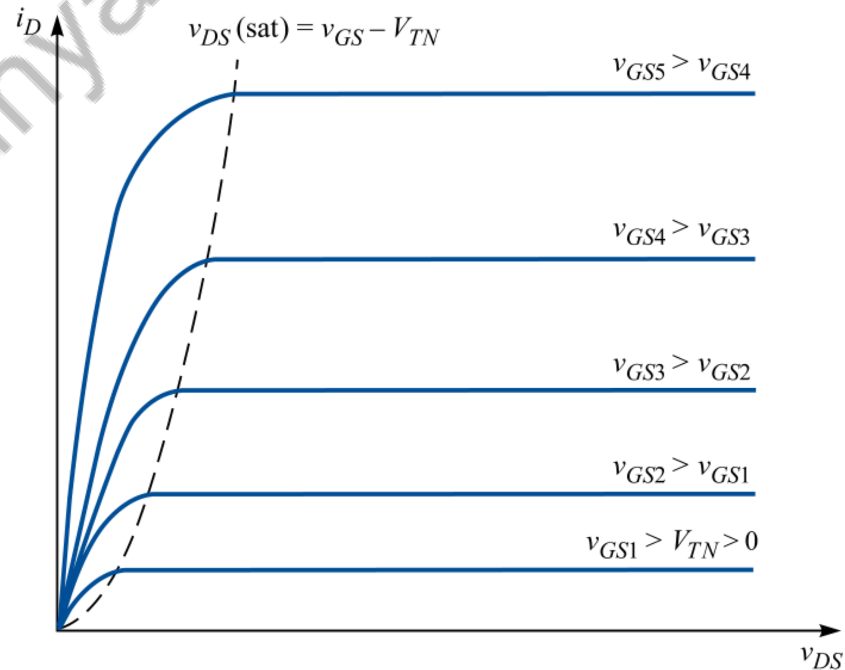
MOSFET Current Equations

1. $I_D = \frac{k_n' W V_{ov} V_{DS}}{L}$ Small V_{DS}

2. $I_D = \frac{k_n' W (V_{ov} - \frac{V_{DS}}{2}) V_{DS}}{L}$ As V_{DS} Increases ($V_{DS} < V_{GS}$-V_T) : Linear Region

3. $I_D = \frac{k_n' W (V_{GS} - V_T)^2}{2L}$ $V_{DS} \geq V_{GS}$-V_T) : Saturation Region

$K_n = \frac{k_n' W}{L}$ $I_D = \frac{K_n (V_{GS} - V_T)^2}{2}$



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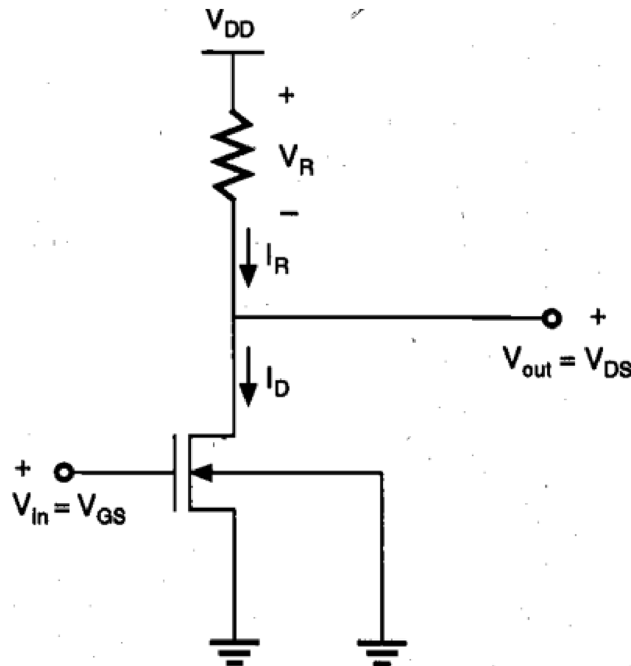
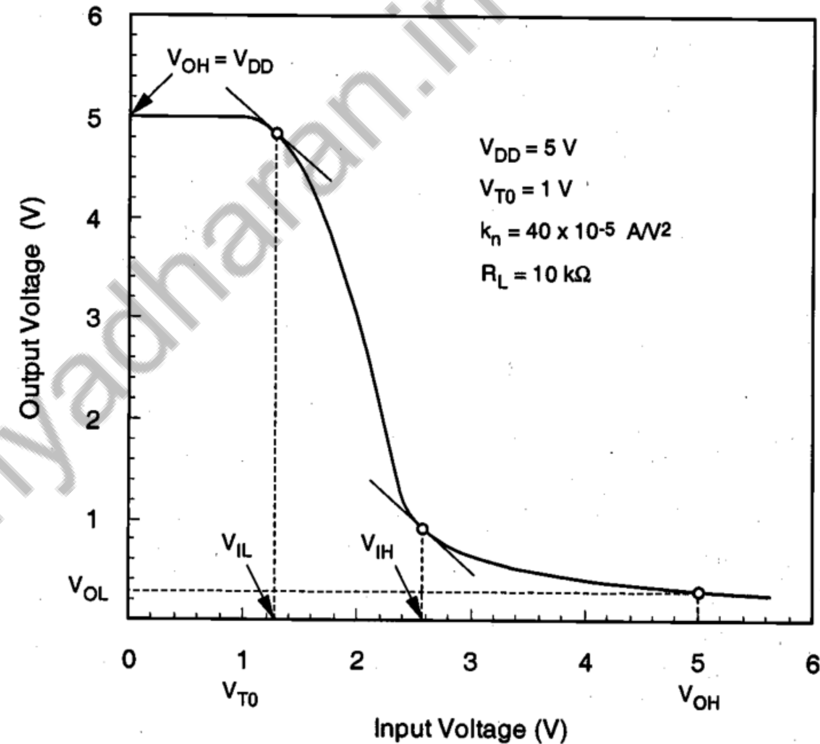
Resistive Load Inverter





Calculation of V_{OH}

$$V_{Out} = V_{DD} - R_L I_R$$

$$V_{OH} = V_{DD}$$

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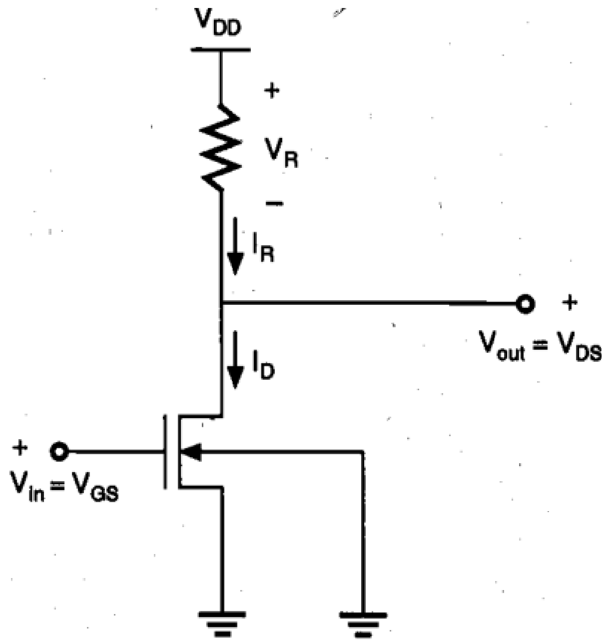
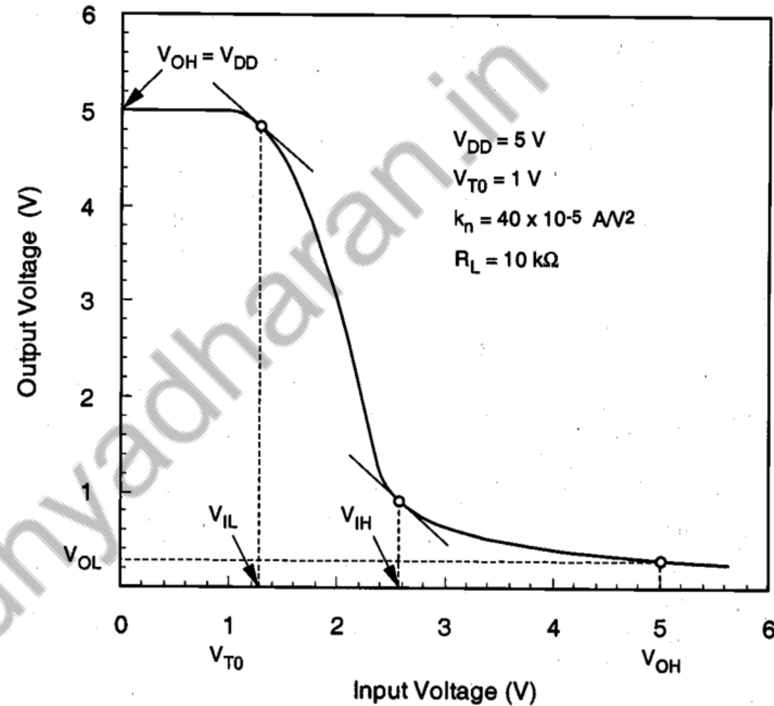
Resistive Load Inverter





$$k' = \mu_n \cdot C_{ox}$$

Calculation of V_{OL}

$$I_R = \frac{V_{DD} - V_{out}}{R_L}$$

$$k = k' \cdot \frac{W}{L}$$

$$\frac{V_{DD} - V_{OL}}{R_L} = \frac{k_n}{2} \cdot \left[2 \cdot (V_{DD} - V_{T0}) \cdot V_{OL} - V_{OL}^2\right]$$

Ratioed logic

$$V_{OL} = V_{DD} - V_{T0} + \frac{1}{k_n R_L} - \sqrt{\left(V_{DD} - V_{T0} + \frac{1}{k_n R_L}\right)^2 - \frac{2 V_{DD}}{k_n R_L}}$$

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Resistive Load Inverter

Calculation of V_{IL}

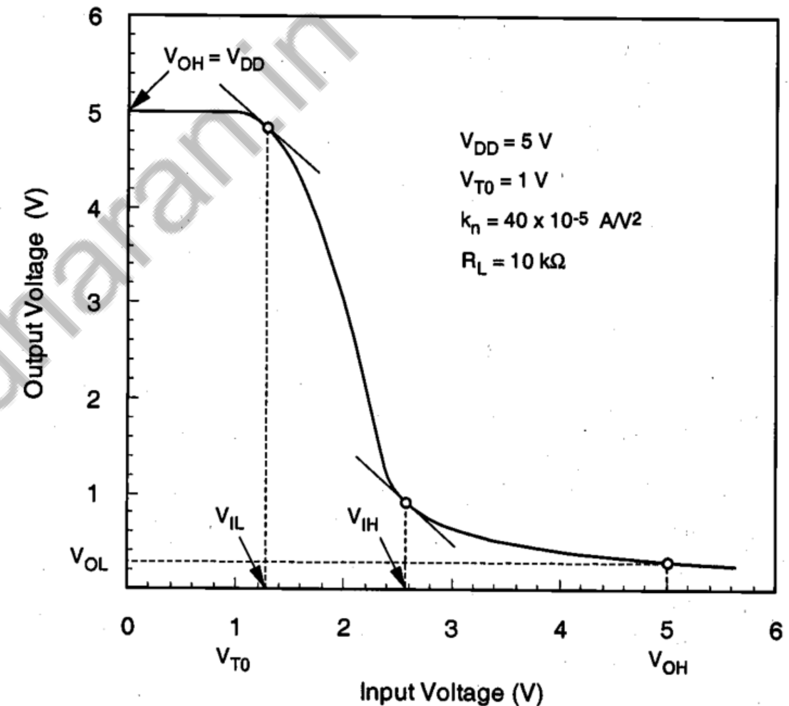
$$\frac{V_{DD}-V_{out}}{R_L}=\frac{k_n}{2}\cdot(V_{in}-V_{T0})^2$$

Differentiating both sides with respect to V_{in}

$$-\frac{1}{R_L}\cdot\frac{dV_{out}}{dV_{in}}=k_n\cdot(V_{in}-V_{T0})$$

$$-\frac{1}{R_L}\cdot(-1)=k_n\cdot(V_{IL}-V_{T0}) \qquad [\frac{dV0}{dVi}=-1]$$

$$V_{IL}=V_{T0}+\frac{1}{k_n R_L}$$



$$V_{out}(V_{in}=V_{IL}) = V_{DD}-\frac{k_n R_L}{2}\cdot\left(V_{T0}+\frac{1}{k_n R_L}-V_{T0}\right)^2$$

$$= V_{DD}-\frac{1}{2k_n R_L}$$

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Resistive Load Inverter

Calculation of V_{IH}

$$\frac{V_{DD}-V_{out}}{R_L}=\frac{k_n}{2}\cdot\left[2\cdot\left(V_{in}-V_{T0}\right)\cdot V_{out}-V_{out}^{2}\right]$$

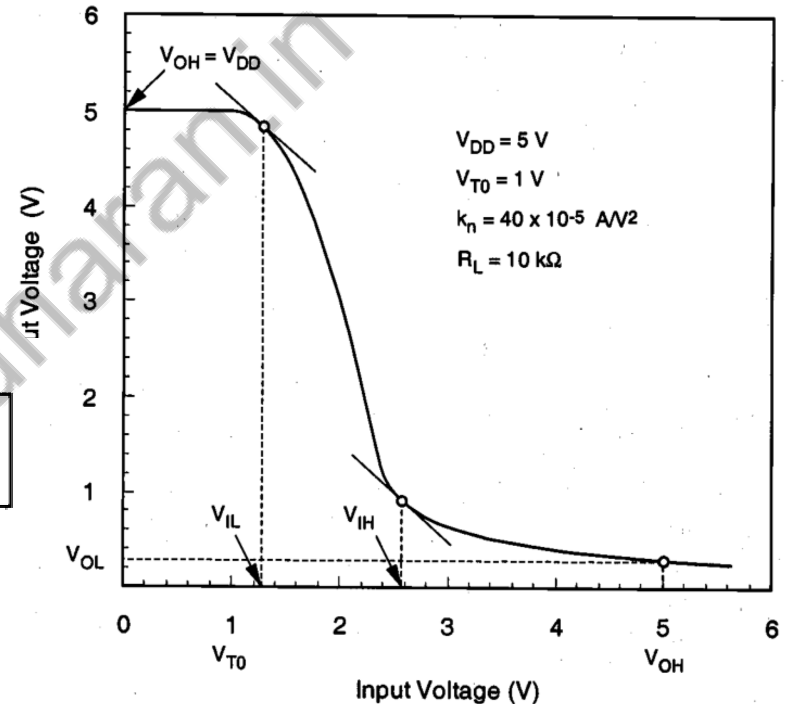
Differentiating both sides with respect to V_{in}

$$-\frac{1}{R_L}\cdot\frac{dV_{out}}{dV_{in}}=\frac{k_n}{2}\cdot\left[2\cdot\left(V_{in}-V_{T0}\right)\cdot\frac{dV_{out}}{dV_{in}}+2V_{out}-2V_{out}\cdot\frac{dV_{out}}{dV_{in}}\right]$$

$$-\frac{1}{R_L}\cdot(-1)=k_n\cdot\left[\left(V_{IH}-V_{T0}\right)\cdot(-1)+2V_{out}\right] \quad \left[\frac{dV0}{dVi}=-1\right]$$

$$V_{IH}=V_{T0}+\sqrt{\frac{8}{3}\cdot\frac{V_{DD}}{k_n R_L}}-\frac{1}{k_n R_L}$$

$$V_{out}\left(V_{in}=V_{IH}\right)=\sqrt{\frac{2}{3}\cdot\frac{V_{DD}}{k_n R_L}}$$



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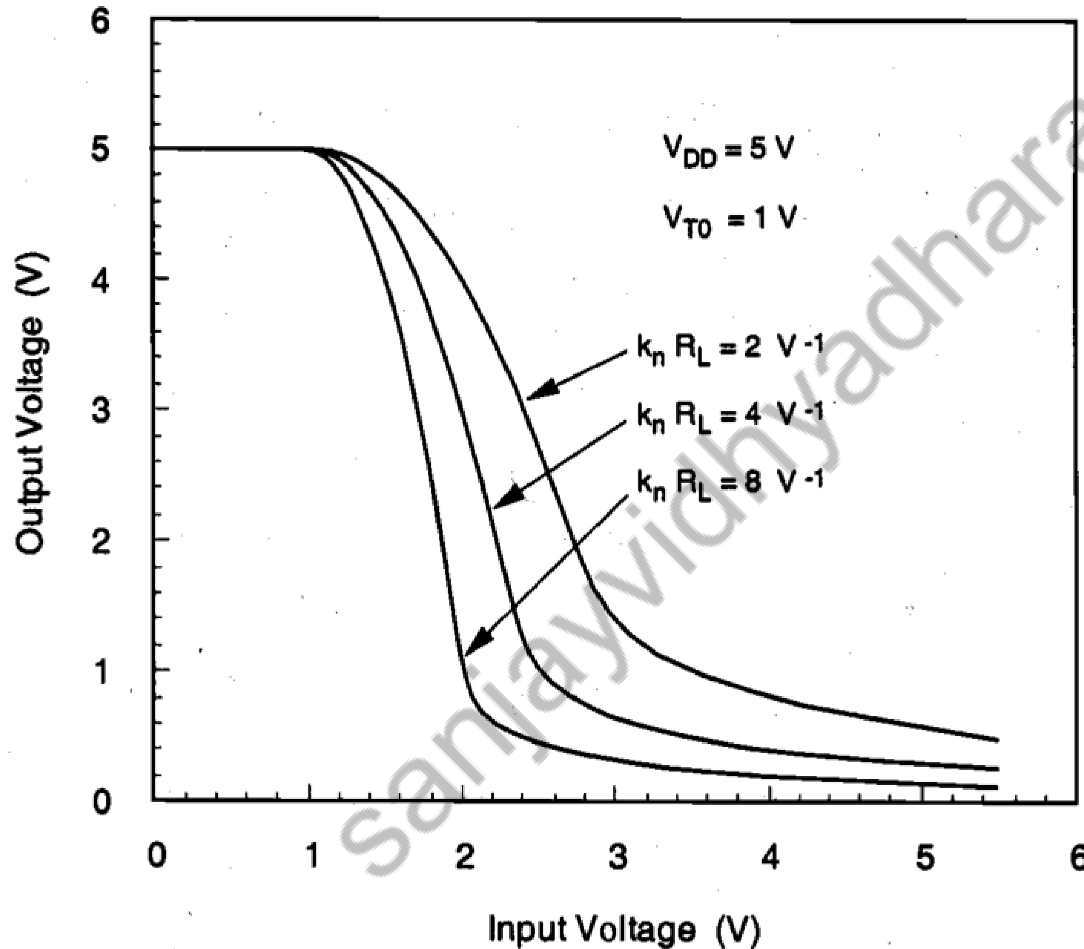
Resistive Load Inverter



$$\text{Gain} = \partial V_O / \partial V_i$$

$$V_O = V_{DD} - I_D . R_L$$

$$I_D = \frac{K_n (V_{GS} - V_T)^2}{2}$$

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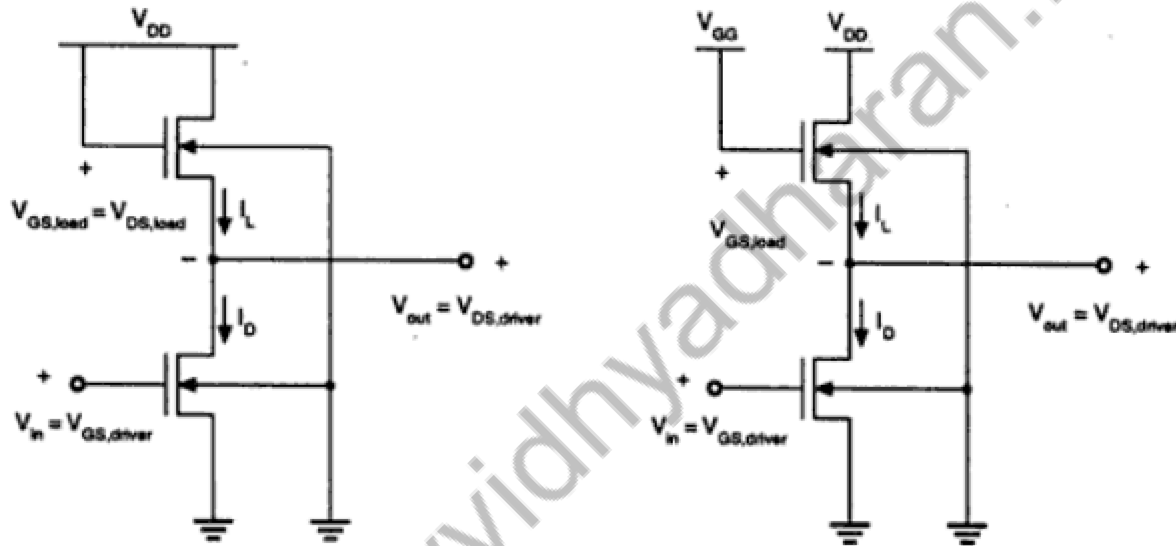
Enhancement-Load nMOS Inverter



- Relatively simple fabrication process
- V_{OH} level is limited to V_{DD} - V_T

- Two separate power supply
- $V_{OH} = V_{DD}$

- High Static Power

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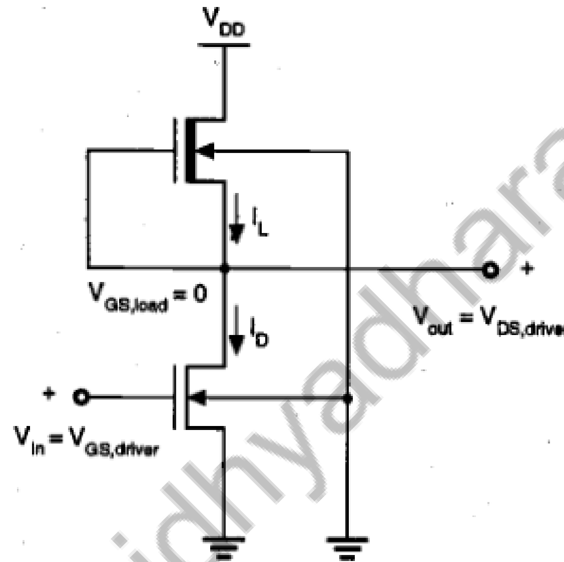
Depletion-Load nMOS Inverter



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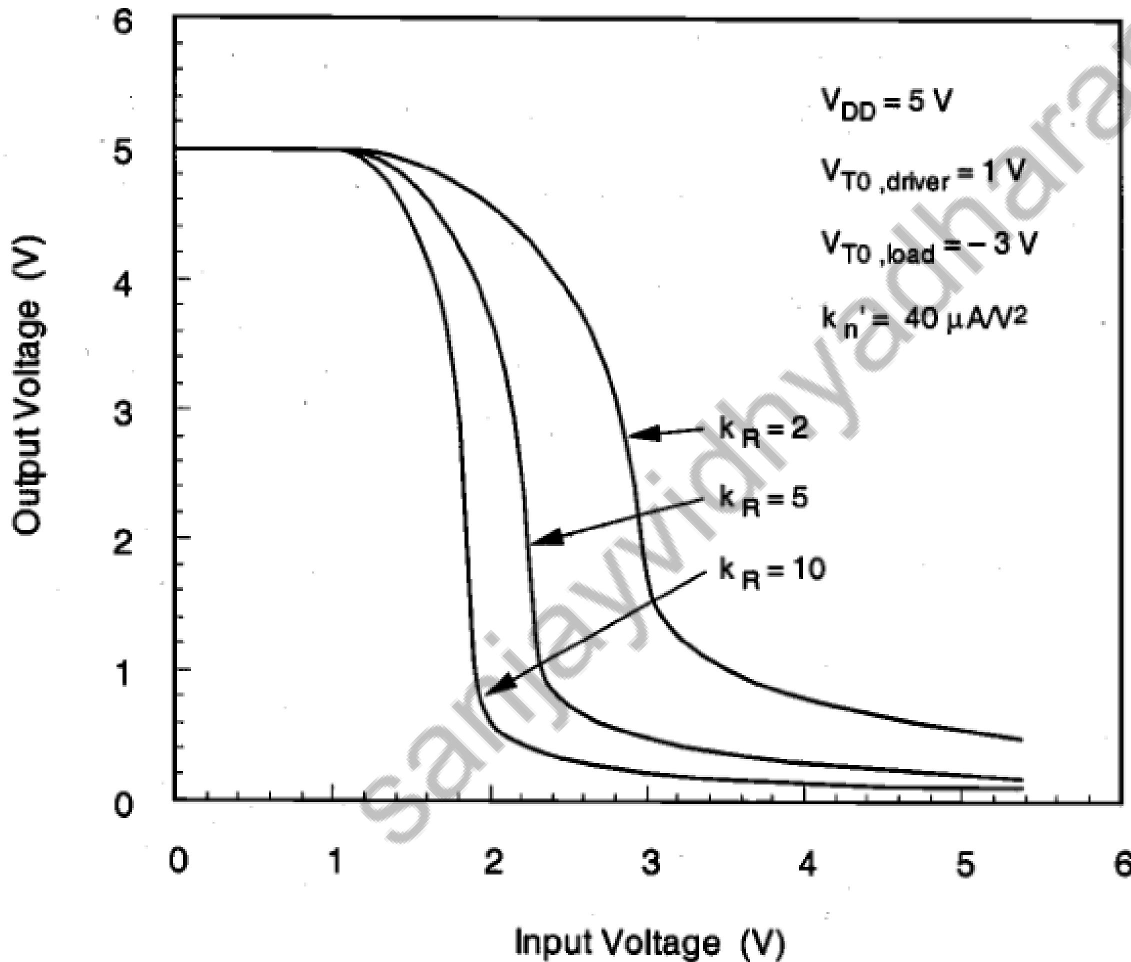
Depletion-type nMOS load is more complicated & requires additional processing steps

- $V_{OH} = V_{DD}$
- Single power supply

Depletion-Load nMOS Inverter



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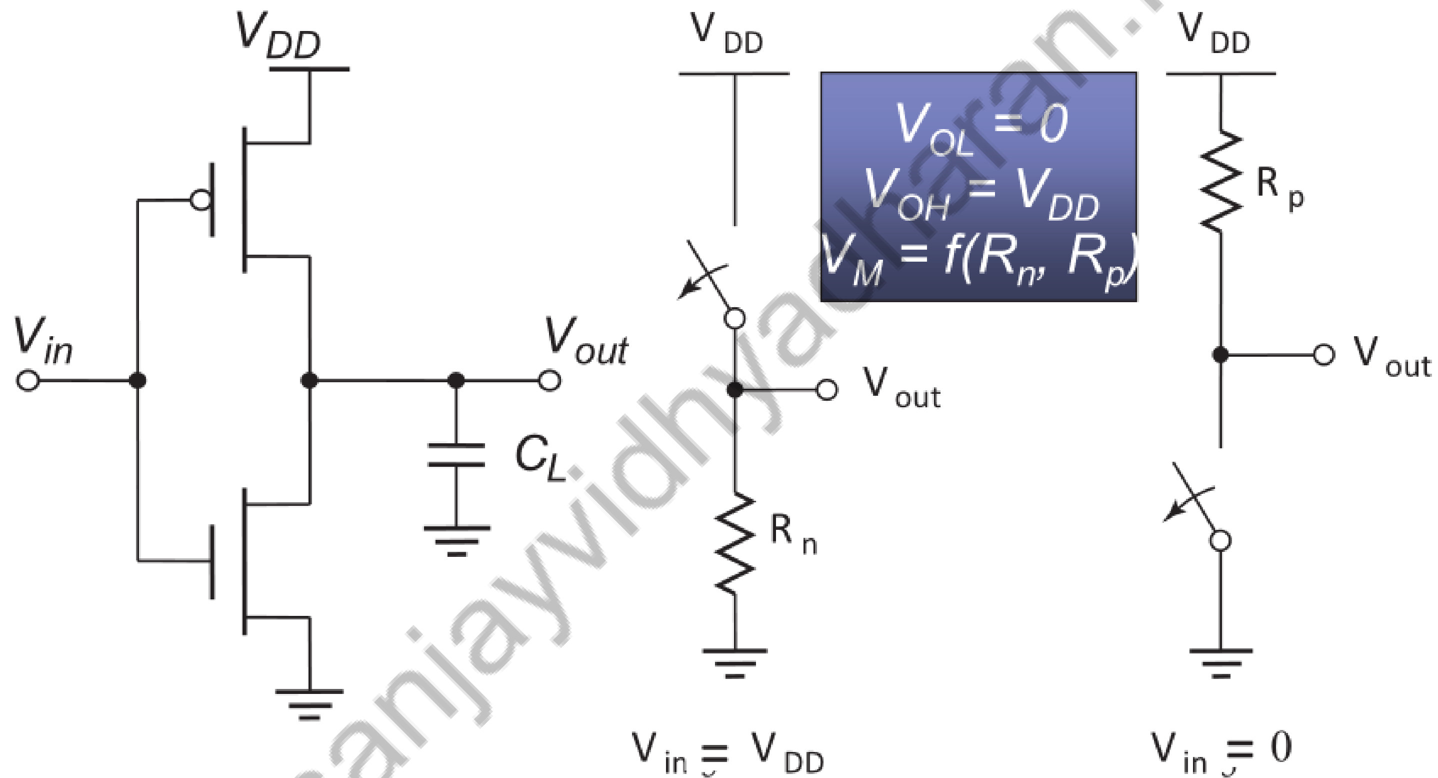
$$k_R = (k_{driver}/k_{load}).$$

The CMOS Inverter

It is the nucleus of all digital designs



Assumed infinite off-resistance for $V_{GS} < V_{TH}$ and finite on-resistance for $V_{GS} > V_{TH}$

Important properties of static CMOS

- Rail-to-Rail O/p : The high and low output levels equal V_{DD} and GND, respectively. This results in high noise margins.

- **Ratioless:** The logic levels are not dependent upon the relative device sizes, so that the transistors can be minimum size.

- In steady state, there always exists a path with finite resistance between the output and either V_{DD} or GND.

- The input resistance of the CMOS inverter is extremely high, the steady-state input current is nearly zero.

- A single inverter can theoretically drive an infinite number of gates (or have an infinite fan-out) and still be functionally operational. However, increasing the fan-out also increases the propagation delay.

- No direct path exists between the supply and ground rails under steady-state operating conditions (this is, when the input and outputs remain constant). The absence of current flow (ignoring leakage currents) means that the gate does not consume any static power.

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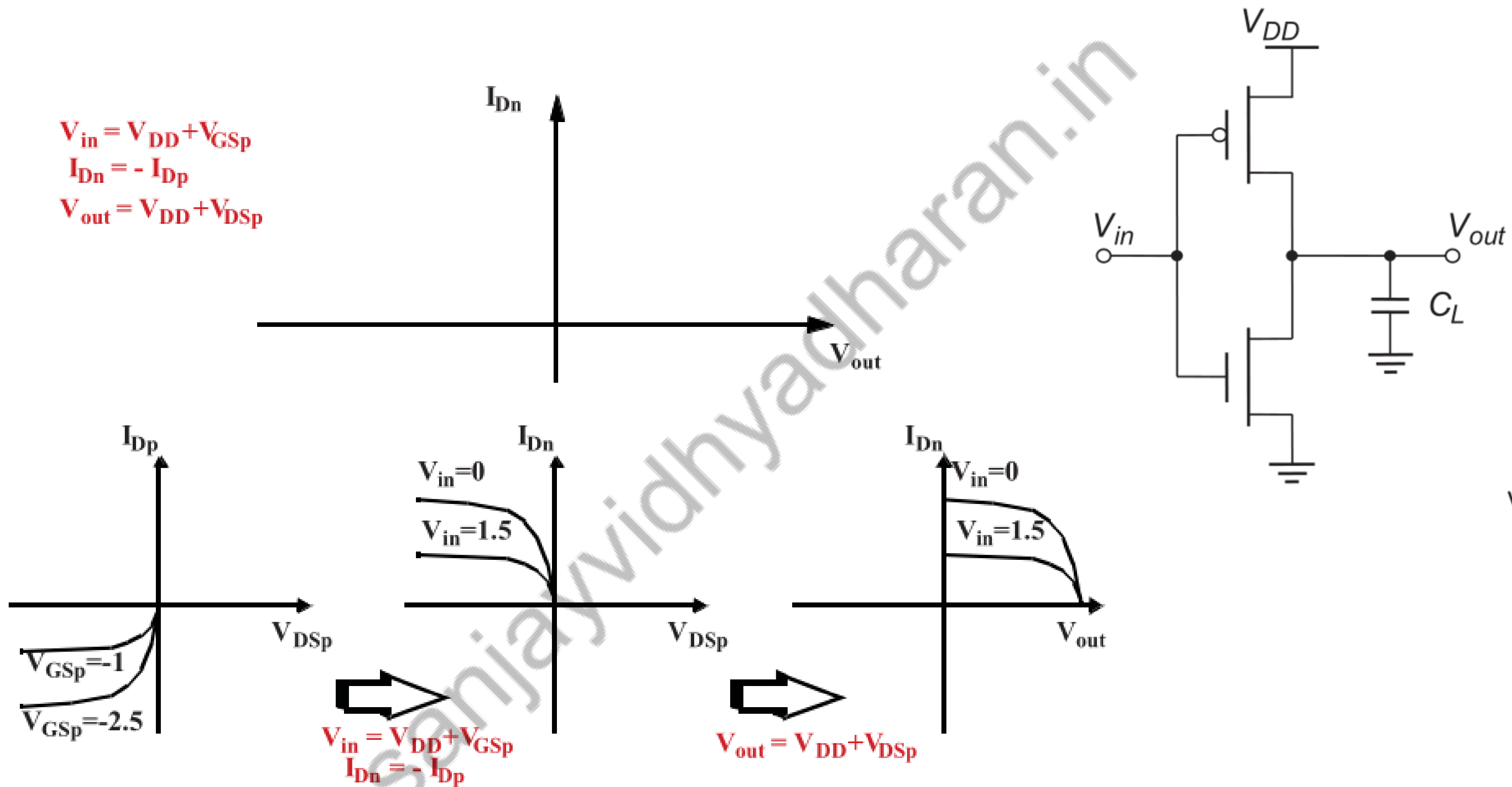
The PMOS Load Line



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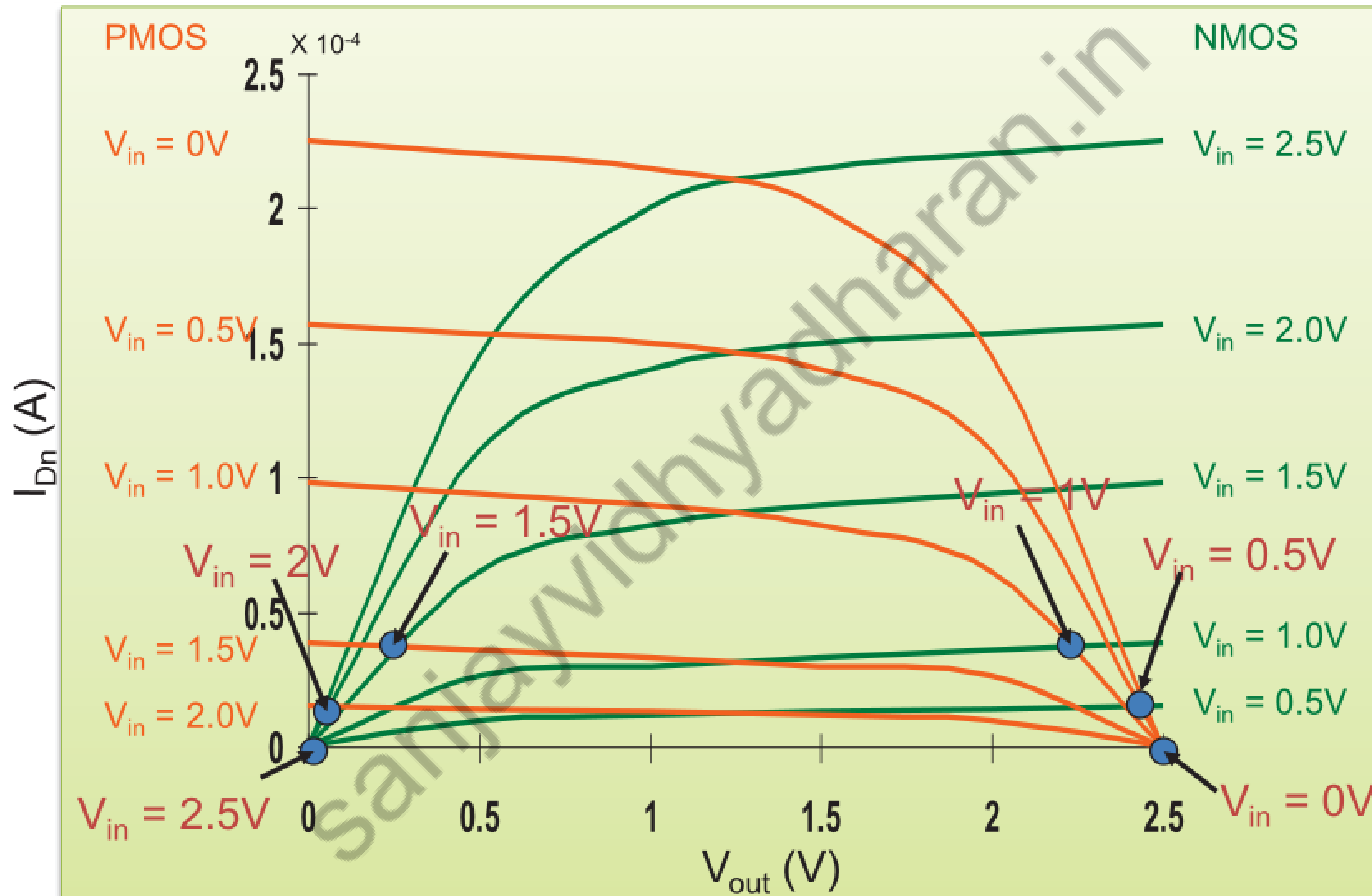
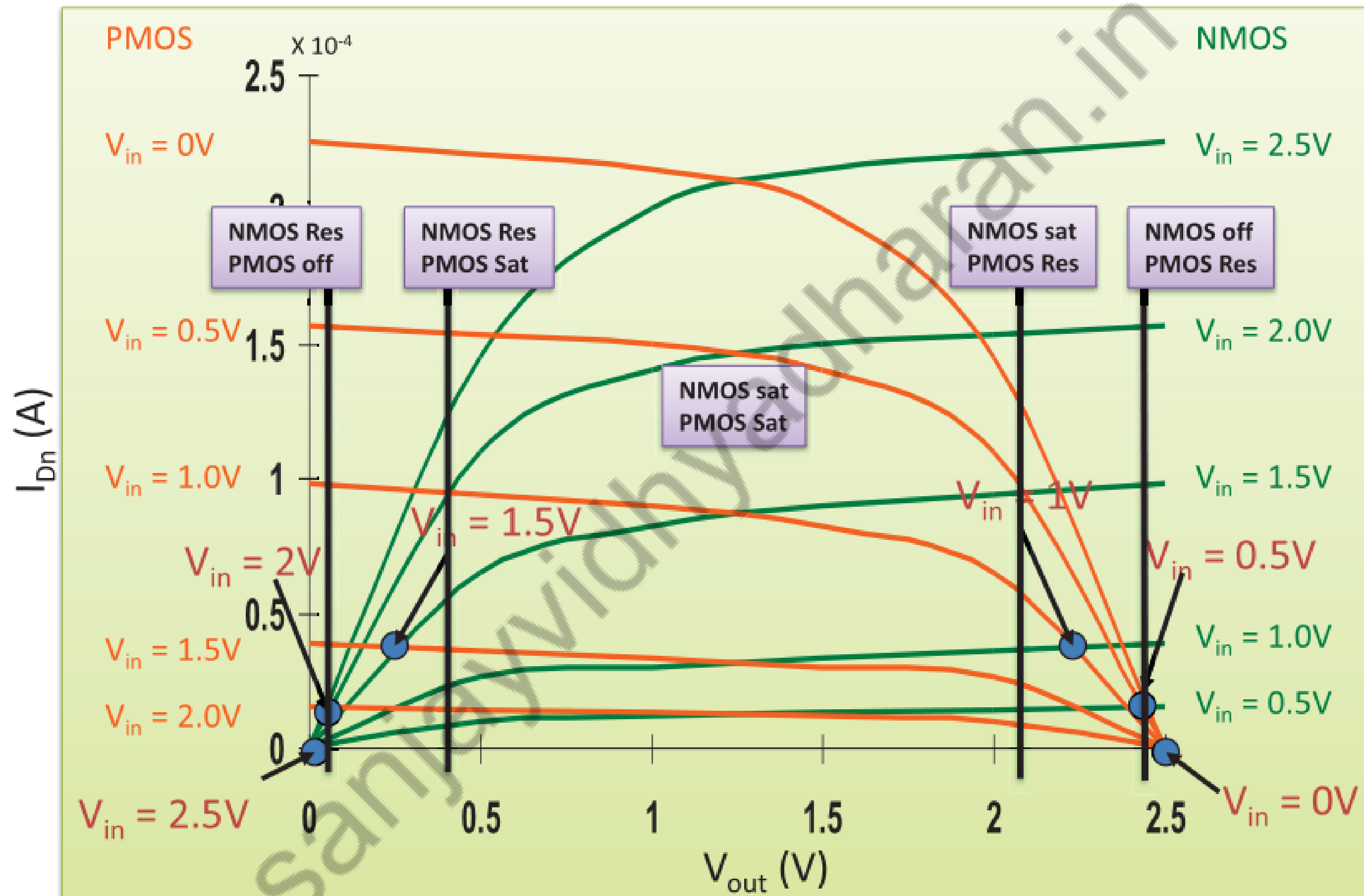
CMOS Inverter Load Characteristic



0.25um, W/L_n = 1.5, W/L_p = 4.5, V_{DD} = 2.5V, V_{Tn} = 0.4V, V_{Tp} = -0.4V

CMOS Inverter Load Characteristic



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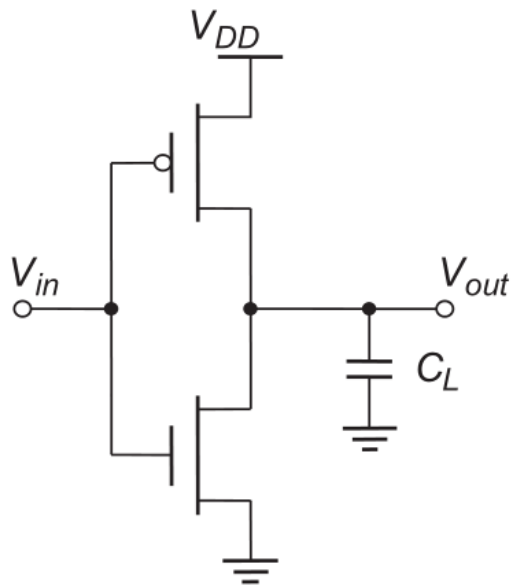
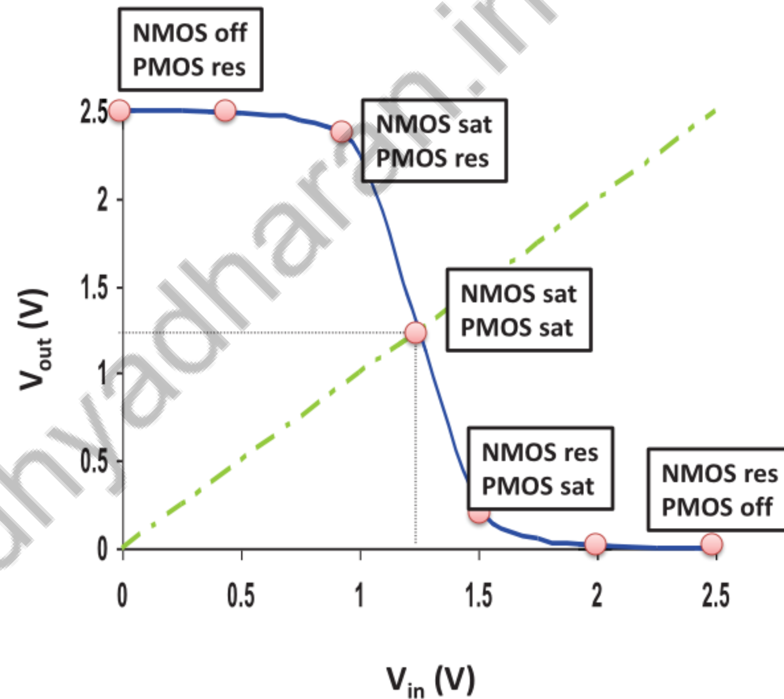
0.25um, $W/L_n = 1.5$, $W/L_p = 4.5$, $V_{DD} = 2.5V$, $V_{Tn} = 0.4V$, $V_{Tp} = -0.4V$

CMOS Inverter VTC





The VTC of the inverter hence exhibits a very narrow transition zone. This results from the high gain during the switching transient, when both NMOS and PMOS are simultaneously on, and in saturation. In that operation region, a small change in the input voltage results in a large output variation.

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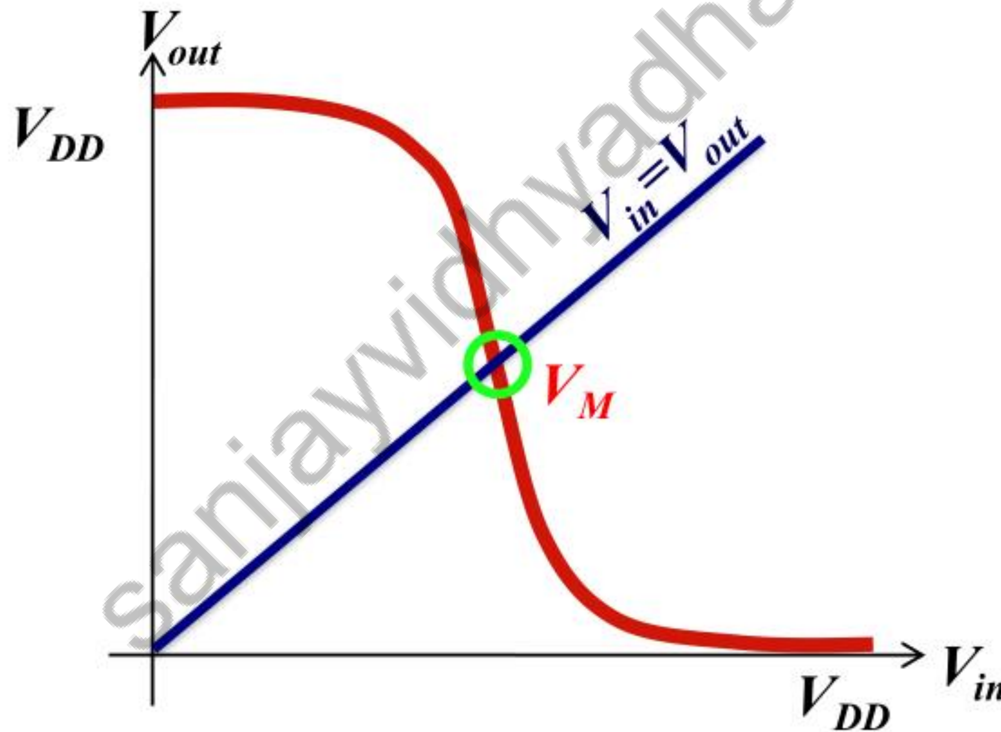
CMOS Inverter Switching Threshold

The Switching Threshold, V_M , is the point where $V_{in} = V_{out}$.
This can be calculated:

» Graphically, at the intersection of the VTC with $V_{in} = V_{out}$



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CMOS Inverter Switching Threshold

- Let's analytically compute V_M.
  - Remember, the saturation current for a MOSFET is given by:

$$I_{DS} = \frac{k}{2}\left(V_{GS} - V_T\right)^2\left(1 + \lambda V_{DS}\right)$$

  - Lets assume $\lambda = 0$ and we'll equate the two currents:

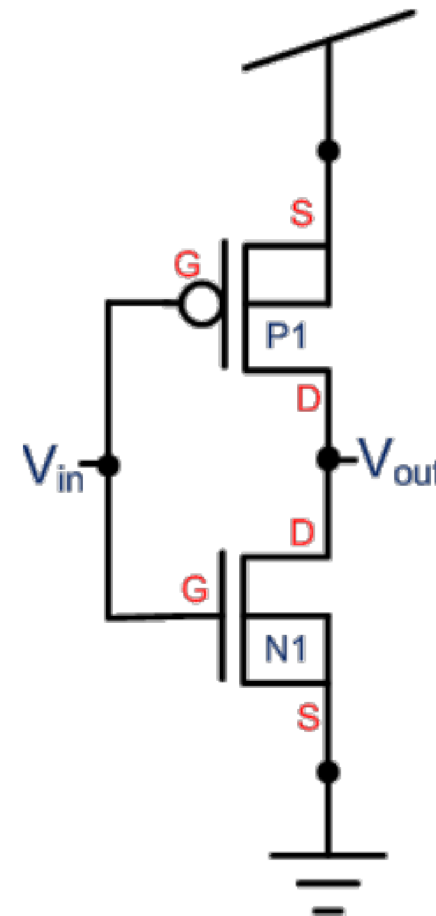
$$I_D = \frac{k_n}{2}\left(V_{GSn} - V_{Tn}\right)^2 = \frac{k_p}{2}\left(V_{SGp} - V_{Tp}\right)^2$$

  - Now we'll substitute:

$$V_{GSn} = V_{in} = V_M \qquad V_{SGp} = V_{DD} - V_{in} = V_{DD} - V_M$$

  - And we'll arrive at:

$$V_M = \frac{V_{Tn} + r\left(V_{DD} - V_{Tp}\right)}{1 + r} \qquad r \triangleq \sqrt{\frac{k_p}{k_n}}$$



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CMOS Inverter Switching Threshold

- A symmetric ***VTC*** (${V_M}={V_{DD}}/2$) is often desired. In this case:

$$V_M = \frac{V_{DD}}{2} = \frac{V_{Tn} + r\left(V_{DD} - V_{Tp}\right)}{1+r} \longrightarrow \left(\frac{W}{L}\right)_p = \frac{\mu_n}{\mu_p}\left(\frac{W}{L}\right)_n$$

- Generally, the same length (L_{min}) is taken for all transistors in digital circuits, and so for a symmetric ***VTC***:

$$\frac{\left(\frac{W}{L}\right)_n}{\left(\frac{W}{L}\right)_p} = \frac{\mu_p}{\mu_n} \approx \frac{230\ \text{cm}^2/\text{V}\cdot\text{s}}{580\ \text{cm}^2/\text{V}\cdot\text{s}}$$

$$\left(\frac{W}{L}\right)_p \approx 2.5\left(\frac{W}{L}\right)_n$$

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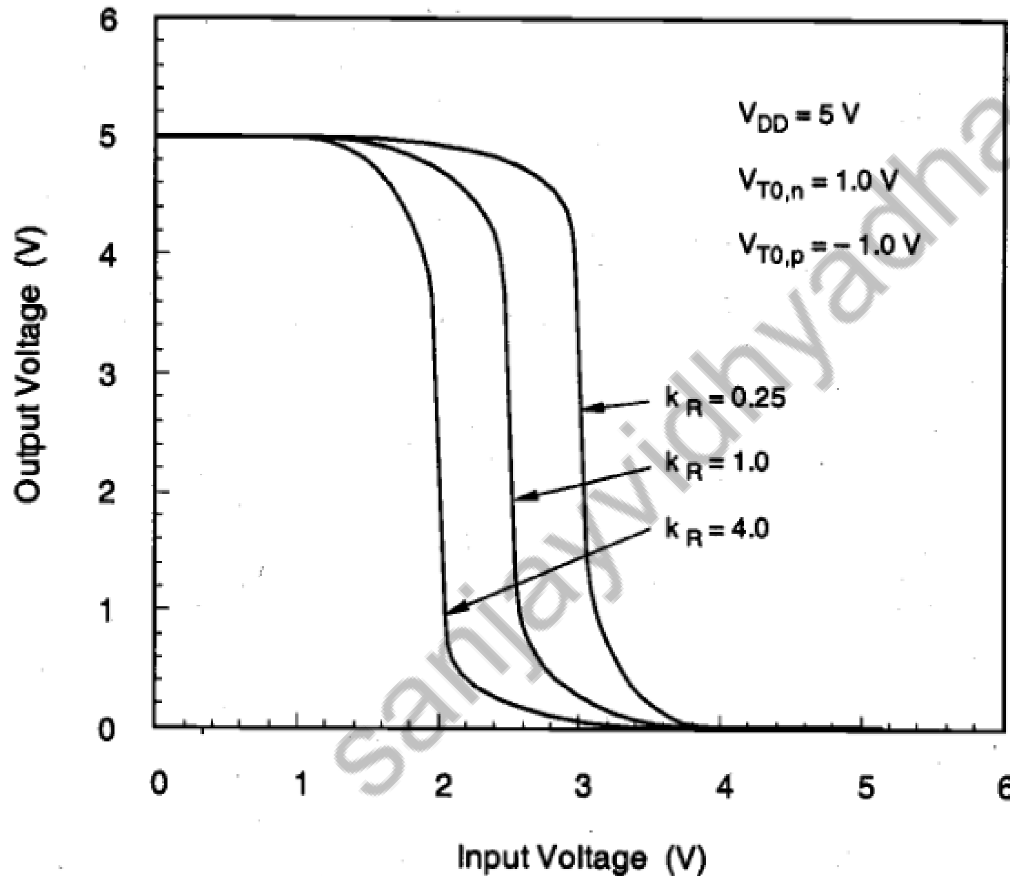
CMOS Inverter Switching Threshold



$$k_R = \frac{k_n}{k_p}$$

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CMOS Inverter Switching Threshold

For Short Channel Devices

$$k_n V_{DSATn}\left(V_M - V_{Tn} - \frac{V_{DSATn}}{2}\right) + k_p V_{DSATp}\left(V_M - V_{DD} - V_{Tp} - \frac{V_{DSATp}}{2}\right) = 0$$

$$V_M = \frac{\left(V_{Tn} + \frac{V_{DSATn}}{2}\right) + r\left(V_{DD} + V_{Tp} + \frac{V_{DSATp}}{2}\right)}{1 + r}$$

$$r = \frac{k_p V_{DSATp}}{k_n V_{DSATn}} = \frac{\upsilon_{satp} W_p}{\upsilon_{satn} W_n}$$

$$r = \frac{\beta_P V_{DSATp}}{\beta_n V_{DSATn}} = \frac{v_{satp} W_p}{v_{satn} W_n}$$

$$r \approx \beta_p / \beta_n$$

$$v_{sat} = \begin{cases} 8 \times 10^6 \text{ cm/s} & \text{for electrons in Si} \\ 6 \times 10^6 \text{ cm/s} & \text{for holes in Si} \end{cases}$$

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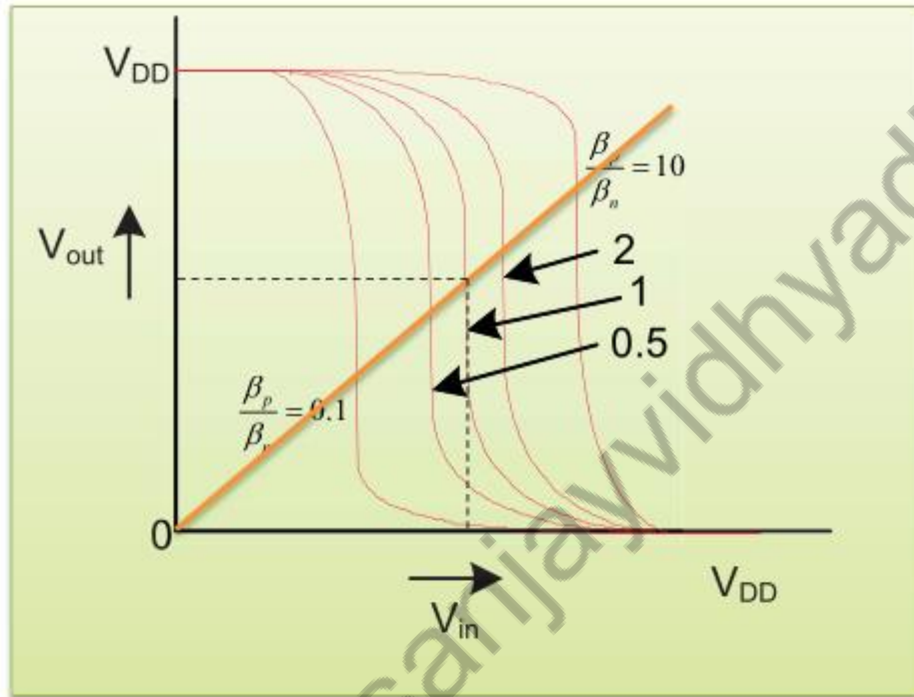
CMOS Inverter Switching Threshold



$r \approx \beta_p / \beta_n$

If $\beta_p / \beta_n \neq 1$

Then its called skewed inverter

HI-Skewed $\beta_p / \beta_n > 1$

LO-Skewed $\beta_p / \beta_n < 1$

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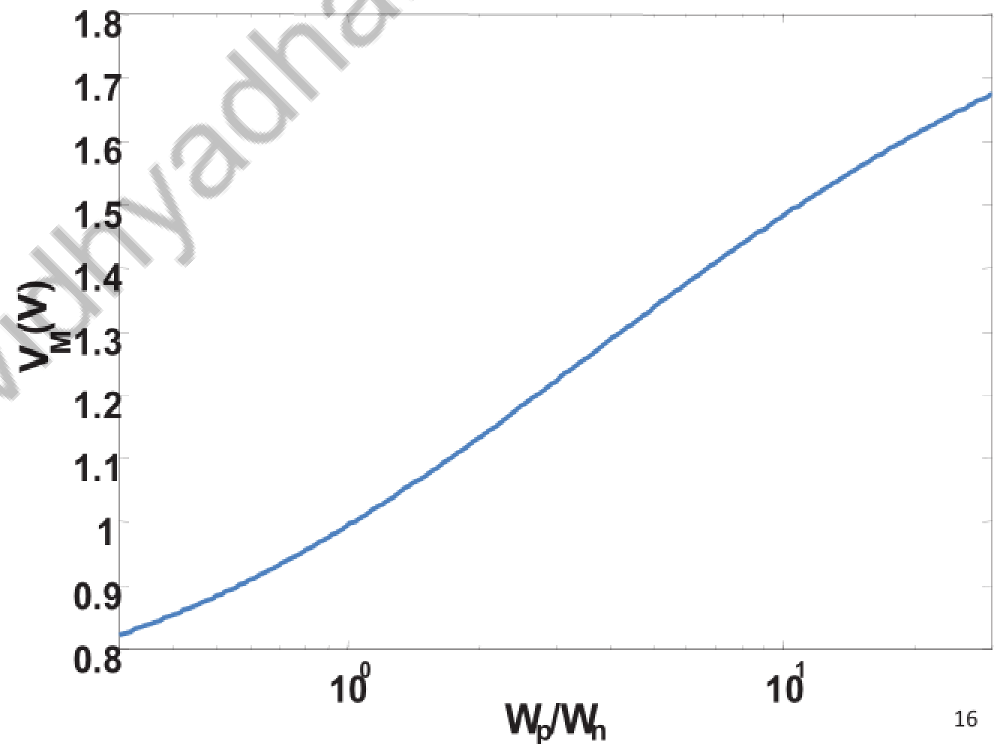
CMOS Inverter Switching Threshold

Increasing the width of the PMOS moves V_M towards V_{DD}

Increasing the width of the NMOS moves V_M towards GND

β -> V_M (250 nm V_{DD} = 2.5 V)

3 -> 1.22 V
2.5 -> 1.18 V
2 -> 1.13 V
Since it not making much difference



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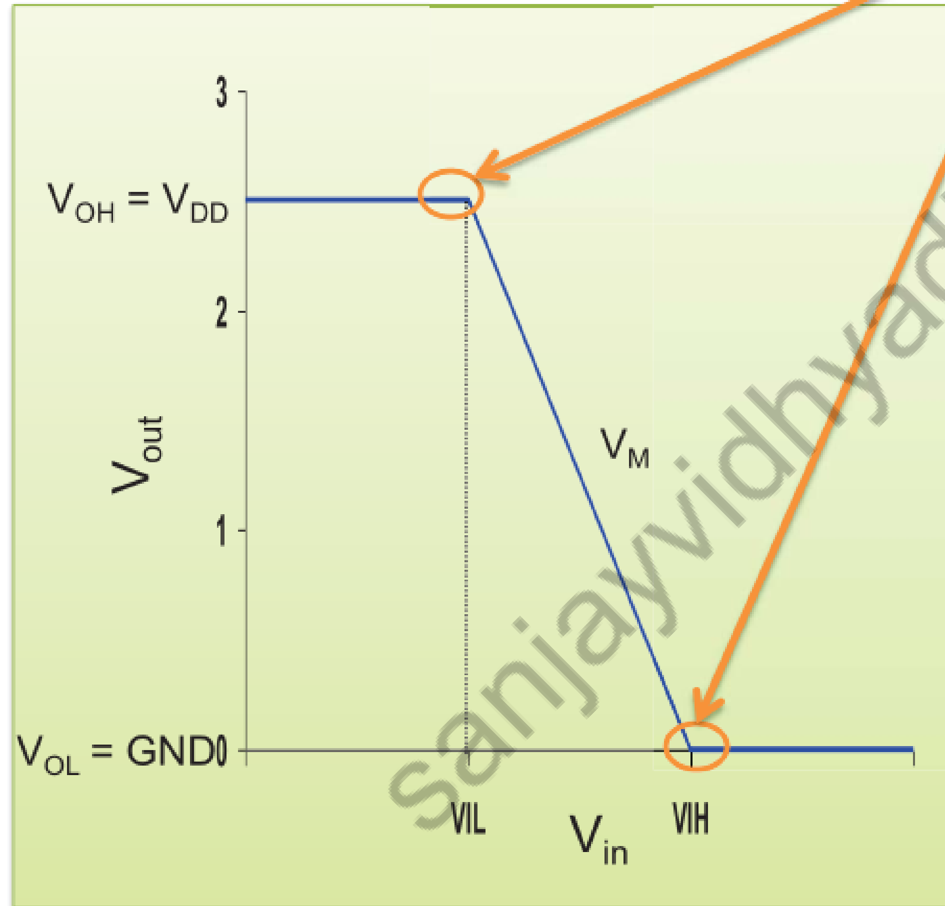
Noise Margin

$d_{Vout}/d_{vin} = -1$



$NM_H = VDD - V_{IH}$

$NM_L = V_{IL} - GND$

Assuming gain '*g*' in transition region

Find V_{IH} and V_{IL}

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Noise Margin

For V_{IL}

$$I_D = \frac{k_n}{2}(V_{gs,n} - V_{T0,n})^2 = \frac{k_n}{2}(V_{in} - V_{T0,n})^2 \quad \text{.....nMOS}$$

$$I_L = \frac{k_p}{2}\left[2\left(V_{gs,p} - V_{T0,p}\right)V_{ds,p} - {V_{ds,p}}^2\right]$$

$$I_L = \frac{k_p}{2}\left[2\left(V_{in} - V_{DD} - V_{T0,p}\right)(V_{out} - V_{DD}) - (V_{out} - V_{DD})^2\right] \quad \text{.....pMOS}$$

$$I_L = I_D$$

$$\frac{k_n}{2}(V_{in} - V_{T0,n})^2 = \frac{k_p}{2}\left[2\left(V_{in} - V_{DD} - V_{T0,p}\right)(V_{out} - V_{DD}) - (V_{out} - V_{DD})^2\right]$$

$$V_{in} = V_{IL} \quad \& \quad \frac{dV_{out}}{dV_{in}} = -1$$

$$k_n\left(V_{IL} - V_{T0,n}\right) = k_p\left[\left(V_{in} - V_{DD} - V_{T0,p}\right)\frac{dV_{out}}{dV_{in}} + (V_{out} - V_{DD}) - (V_{out} - V_{DD})\frac{dV_{out}}{dV_{in}}\right]$$

$$k_n\left(V_{IL} - V_{T0,n}\right) = k_p\left[\left(V_{in} - V_{DD} - V_{T0,p}\right)(-1) + (V_{out} - V_{DD}) - (V_{out} - V_{DD})(-1)\right]$$

$$\boxed{V_{IL} = \frac{2V_{out} + V_{T0,p} - V_{DD} + K_R V_{T0,n}}{1 + K_R}}$$

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Noise Margin

For V_{IH}

$$V_{in} = V_{IH} \quad \& \quad \frac{dV_{out}}{dV_{in}} = -1$$

$$k_p\left(V_{in} - V_{DD} - V_{T0,p}\right) = k_n\left[\left(V_{in} - V_{T0,n}\right)\frac{dV_{out}}{dV_{in}} + (V_{out}) - (V_{out})\frac{dV_{out}}{dV_{in}}\right]$$

$$k_p\left(V_{IH} - V_{DD} - V_{T0,p}\right) = k_n\left[\left(V_{IH} - V_{T0,n}\right)(-1) + (V_{out}) - (V_{out})(-1)\right]$$

$$k_p\left(V_{IH} - V_{DD} - V_{T0,p}\right) = k_n\left(V_{T0,n} - V_{IH} + 2V_{out}\right)$$

$$\frac{k_n}{k_p}\left(V_{T0,n} + 2V_{out}\right) = \frac{k_n}{k_p}V_{IH} + V_{IH} - V_{DD} - V_{T0,p}$$

$$\frac{k_n}{k_p}\left(V_{T0,n} + 2V_{out}\right) = \left(1 + \frac{k_n}{k_p}\right)V_{IH} - V_{DD} - V_{T0,p}$$

$$\boxed{V_{IH} = \frac{V_{DD} + V_{T0,p} + K_R\left(2V_{out} + V_{T0,n}\right)}{1 + K_R}}$$

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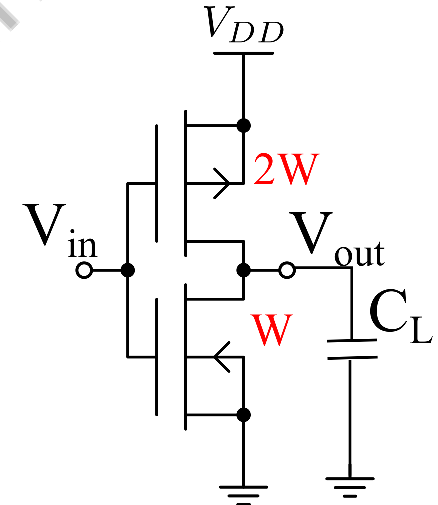
Static Loss

➢ Causes for High Static Power Consumption

Effect of Decreasing V_{DD} on Delay



$$Propagation\ Delay\ (tpd) = \frac{K_1 C_L}{I_D} = \frac{K_2 C_L}{(V_{DD} - V_{th})^2}$$

Effect of Decreasing V_{th} on Power

- Intel estimated leakage power consumption at more than 50W for a 100nm technology node.
- Leakage depends strongly on a Threshold voltage (V_{th}) of the transistor

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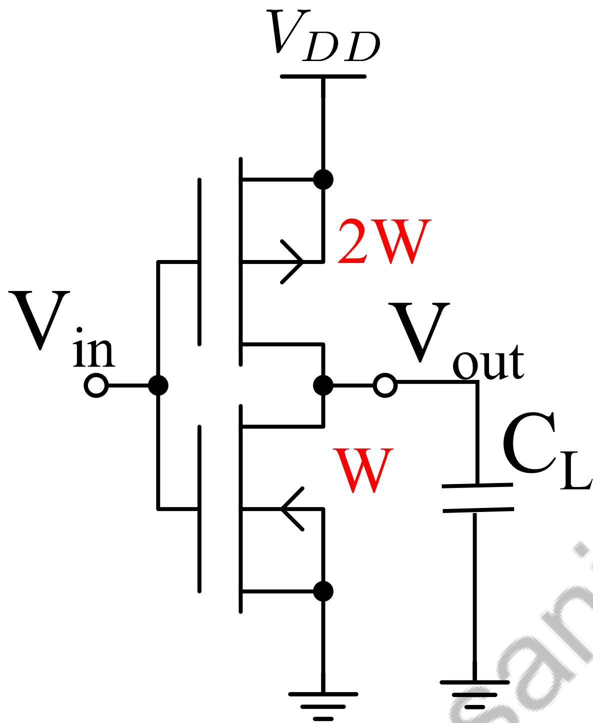
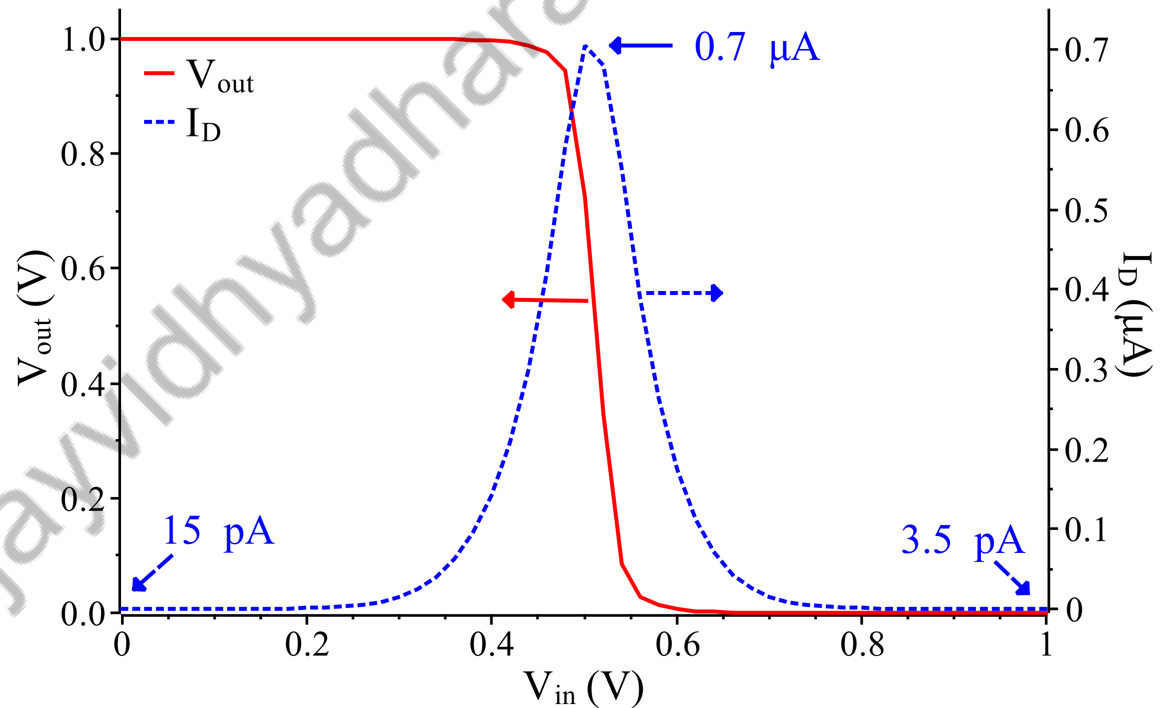
Static Loss





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Static Loss

➢ Reducing Static Loss

- Device Level Techniques
  - Tunnel Field Effect Transistors
  - CNFETs
- Circuit Level Techniques when using CMOS

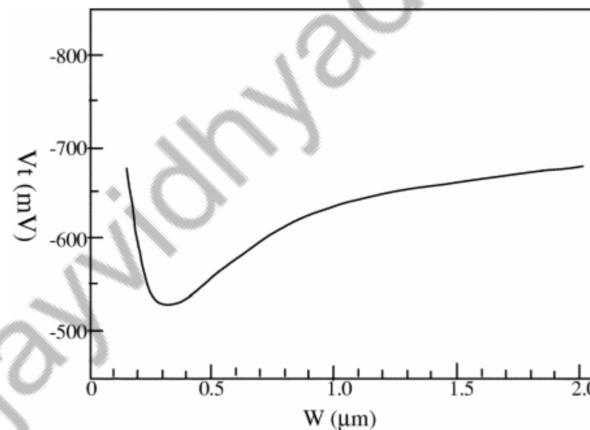

Fig. 12 Variation of threshold voltage with gate width in the case of trench isolated buried channel P-MOSFET showing the anomalous behavior [27].

[3] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," Proceedings of the IEEE, vol. 91, no. 2, pp. 305–327, Feb. 2003.

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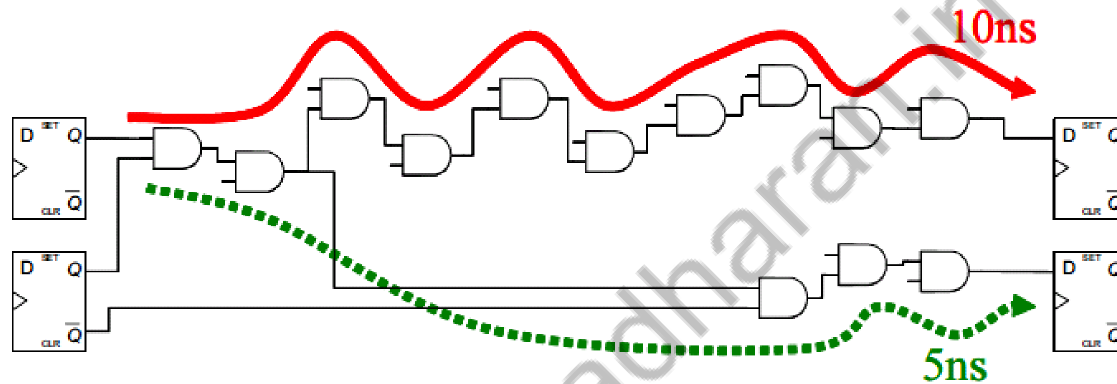
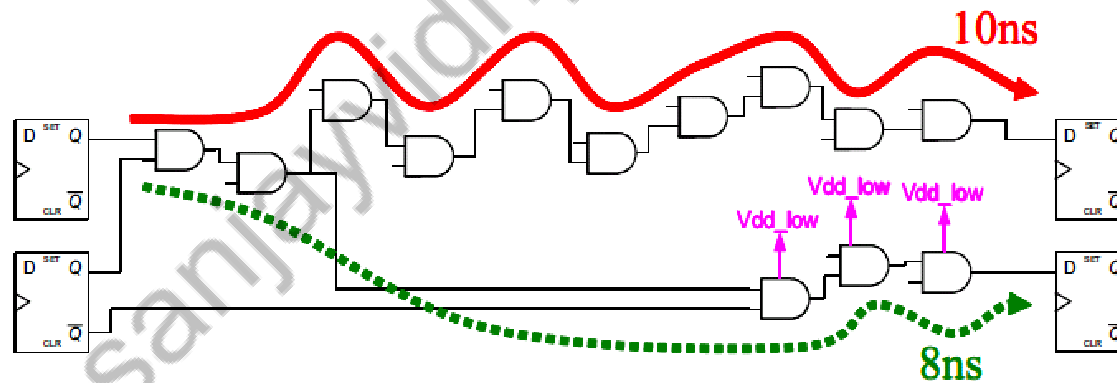
Static Loss

Multiple V_{DD} for Power Reduction





[5] M. Pedram and J.M. Rabaey, "Power aware design Methodologies," [Online]. Available: https://www.springer.com/gp/book/9781402071522

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Static Loss

Challenges of Multi-V_{DD} Design

- The additional supply voltage V_{DD} needs to be created on-chip by a dc to dc converter.
- Area overhead, and in power consumption for the converter.
- Level-shifters are required between different supply domains.
- Multiple Routing

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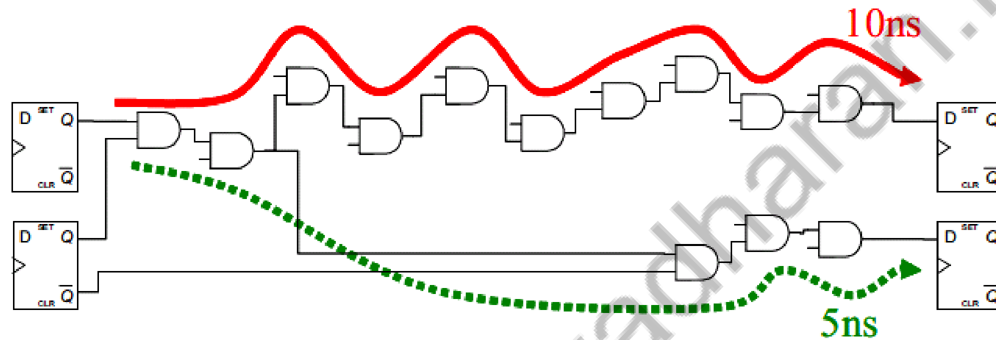
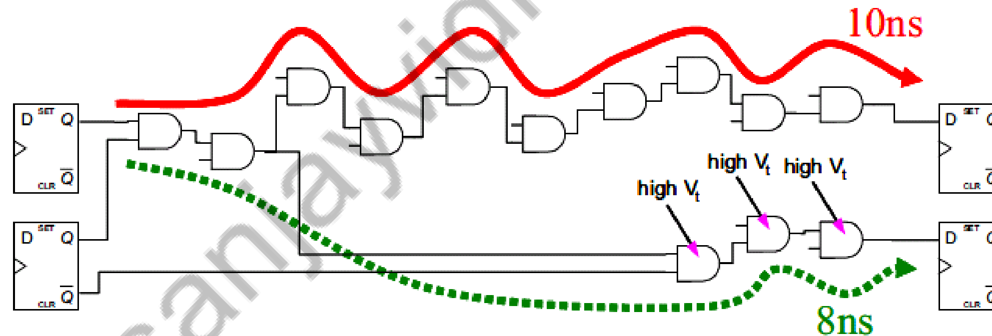
Static Loss

Multi-V_{th} Design



Non-critical path may be delayed



Non-critical path runs with increased threshold voltage

[5] M. Pedram and J.M. Rabaey, "Power aware design Methodologies," [Online]. Available: https://www.springer.com/gp/book/9781402071522

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Static Loss

Challenges of Multi-V_{th} Design

- **ADDITIONAL MASKS**

- **FOR EACH SUCH OPTION, THE DESIGN LIBRARY MUST BE ELECTRICALLY CHARACTERIZED, MODELED FOR ALL DESIGN TOOLS**

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Thank you

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