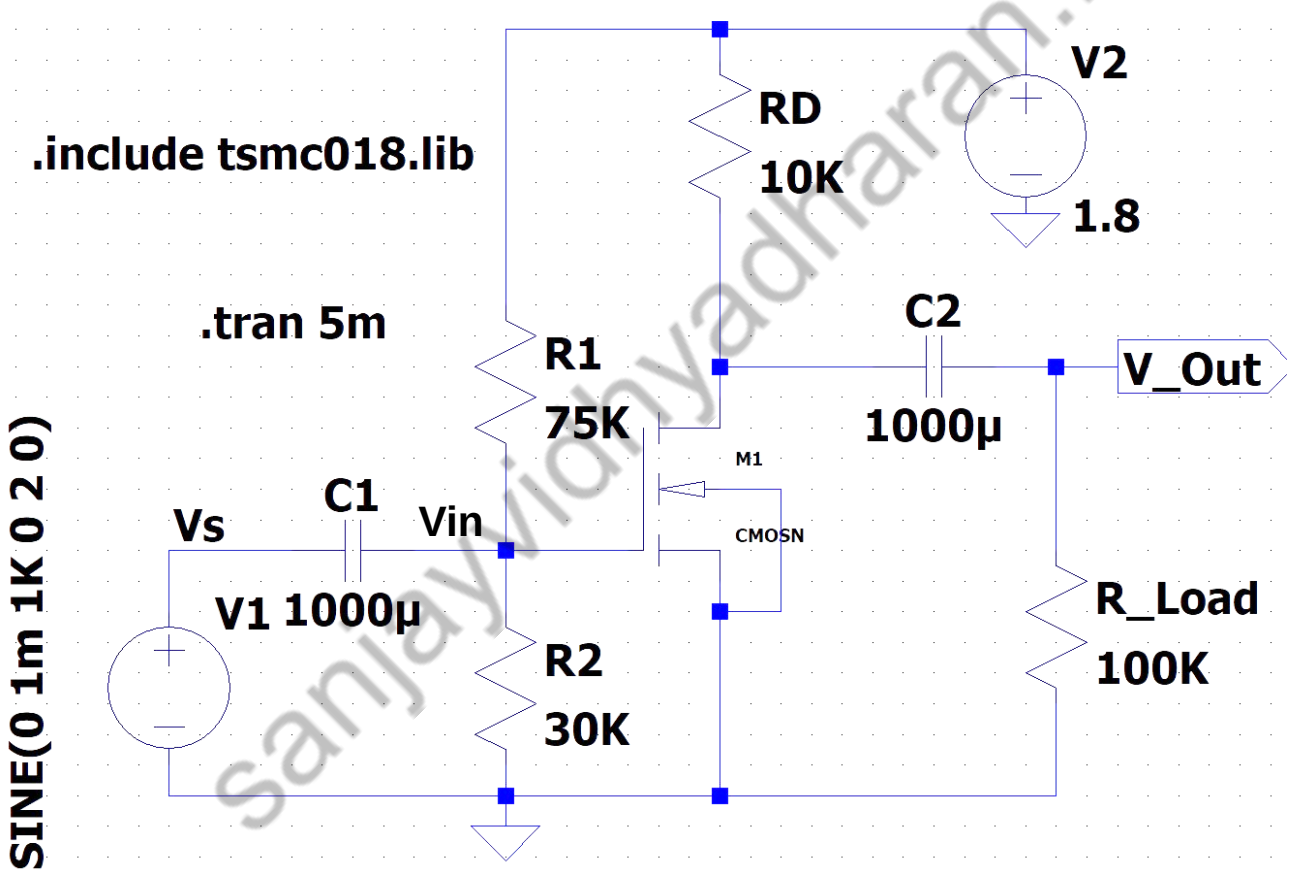
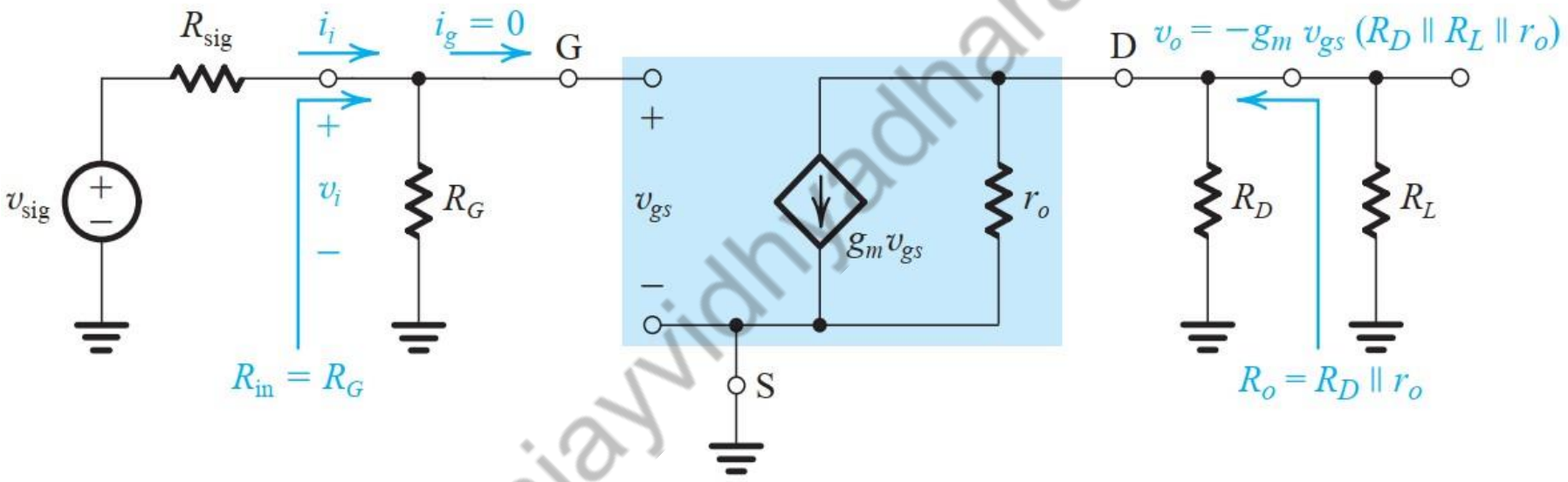
Analog IC Design : 2022-23
Lecture 3
MOSFET Single Stage Amplifiers Part-2

By Dr. Sanjay Vidhyadharan

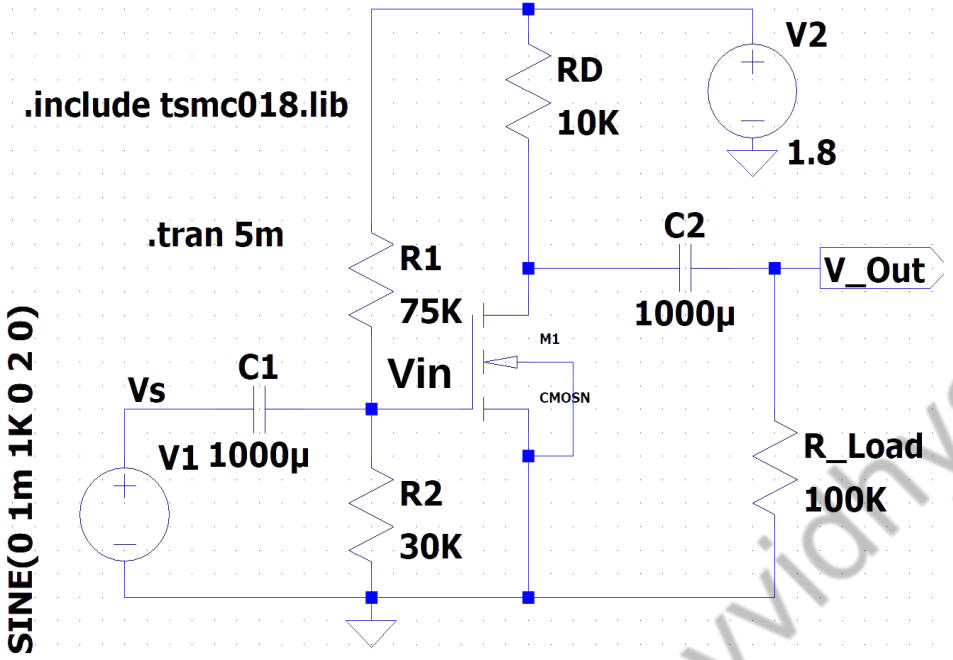
CS Amplifier



CS Amplifier



CS Amplifier



Design Steps

1. Fix I_{DQ} Meeting following conditions

(a) $I_{DQ} * V_{DD}$ < Max Power Constraint

(b) SR= dVo / dt maximum V/µs

SR= I_D / C_{Load}

2. Fix R_D for Max Symmetrical Output swing

$R_D = (V_{DD} - V_{ov})/2I_{DQ}$

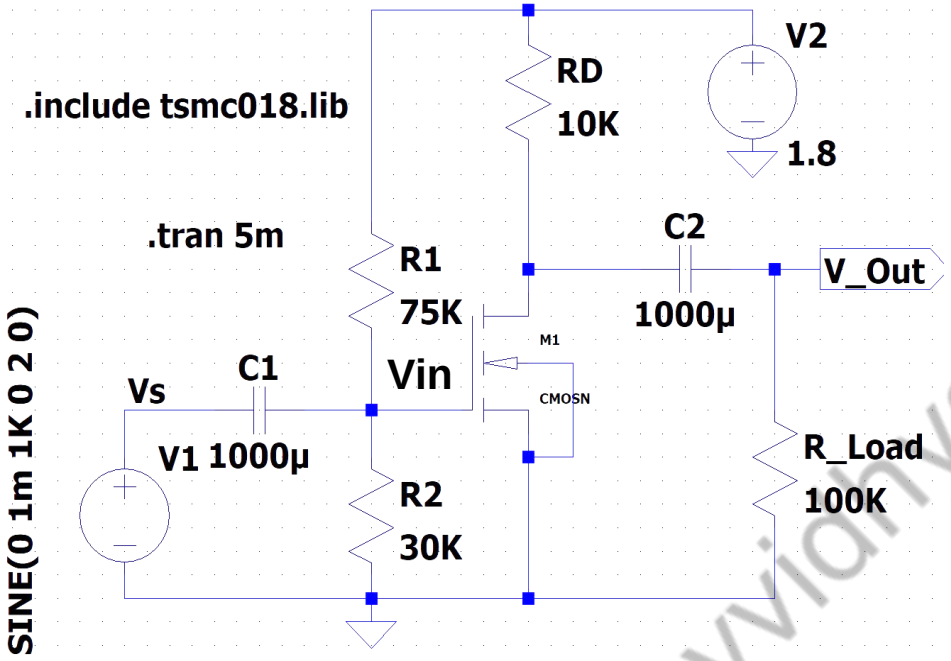
3. Fix (W/L) for required gain

$$Gain = -g_m * (R_D || r_0 || RL)$$

$$g_m = 2I_D / V_{ov}$$

$$g_m = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right) I_D}$$

CS Amplifier



Design Steps

4. Design issues with R1 and R2
   Set for V-overdrive (V_{GS})

$$g_m = \mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{Tn})\,(1 + \lambda_n V_{DS})$$

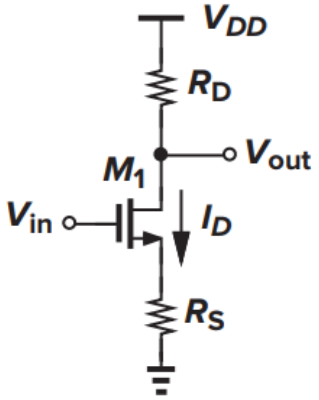
5. Values of C1 and C2

Gain is a function of Load Resistance
High Input Impedence
High Miller Capacitance
Current , Voltage and Power Gain

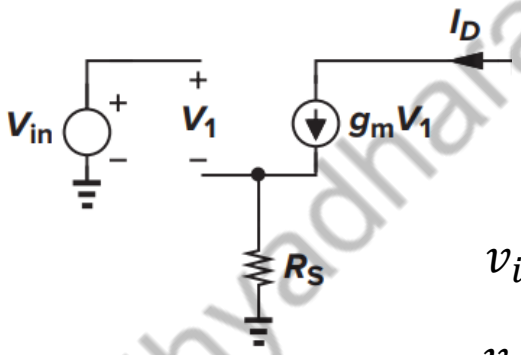
$$Gain = -g_m * (R_D || r_0 || RL)$$

CS Amplifier

CS stage with source degeneration.



(a)



(b)

$$V_{IN} = V_{GS} + I_D\ R_S$$

$$\Delta I_D = \Delta(V_{IN} - V_{GS})/R_S$$

$$v_{in} = v_{gs+}\ i_d\ R_s$$

$$v_{in} = v_{gs+}\ g_m\ v_{gs}\ R_s$$

$$v_{in} = v_{gs}\ \ (1 + g_m\ )R_s$$

$$v_{out} = i_d\ R_D$$

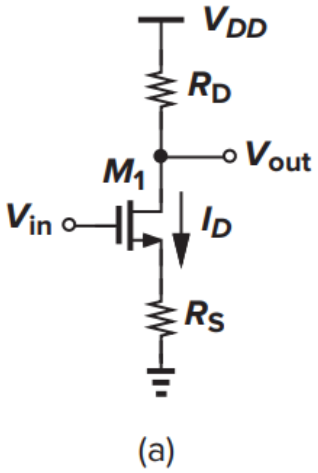
$$v_{out} = -v_{gs}\ \ g_m\ R_D$$

$$Gain = -\frac{g_m\ R_D}{(1 + g_m\ )R_s}$$

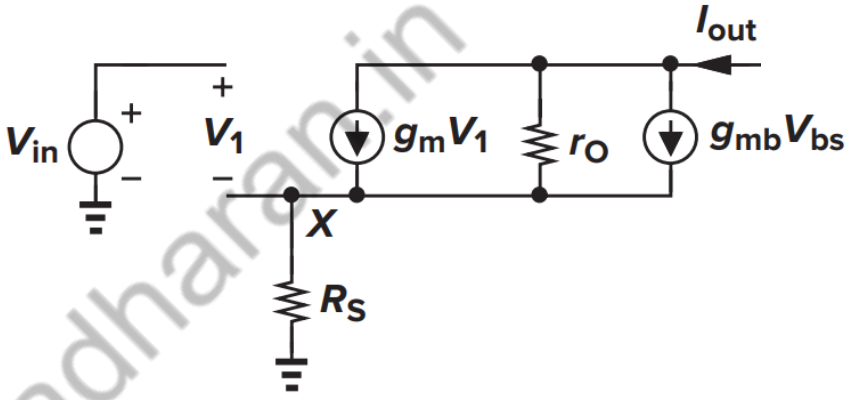
$$Gain \sim -\frac{R_D}{R_s}$$

CS Amplifier

CS stage with source degeneration.



(a)



$$v_{in} = v_{gs+} V_X \qquad v_{out} = - i_{out} R_D$$

$$v_{in} = v_{gs+} i_{out} R_s$$

$$i_{out} = g_m (v_{in} - i_{out} R_S) - (g_{mb} i_{out} R_s) + \frac{- i_{out} R_D - i_{out} R_S)}{r_o}$$

$$i_{out}(1 + (g_m + g_{mb})R_S + \frac{R_D + R_S}{r_o})) = g_m \; v_{in}$$

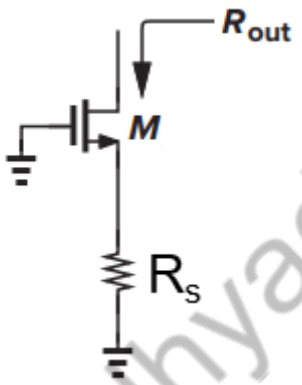
$$Gain = \frac{-g_m R_D}{1 + (g_m + g_{mb})R_S + \frac{R_D + R_S}{r_o}}$$

$$Gain = \frac{-g_m R_D r_o}{R_D + R_S + r_o + (g_m + g_{mb})R_S r_o}$$

$$Gain \sim - \frac{R_D}{R_S}$$

CS Amplifier

CS Amplifier Output Resistance



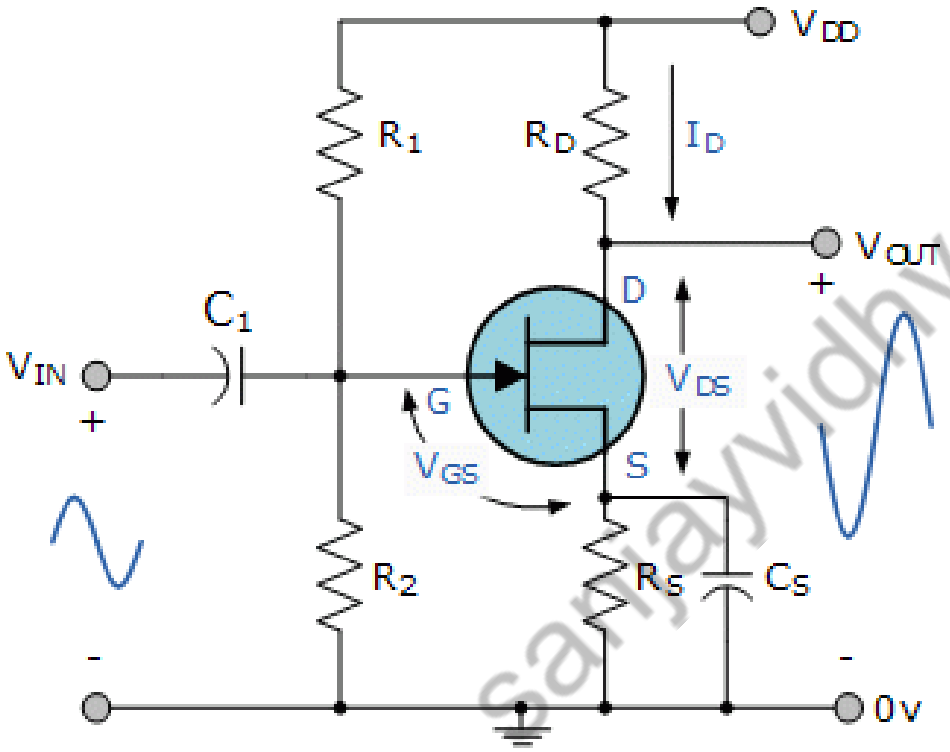
$$i_{out} = -g_m\, i_{out} R_S - g_{mb}\, i_{out} R_S + \frac{v_{out} - i_{out} R_S)}{r_o}$$

$$i_{out}((g_m + g_{mb})\, r_o R_S + r_o + R_S) = v_{out}$$

$$R_{out} \approx r_o + g_m\, r_o R_S$$

CS Amplifier

CS stage with source degeneration and bypass capacitor.



$$Gain \sim -g_m R_D$$

Design Steps

1. Fix I_{DQ} Meeting following conditions

(a) $I_{DQ} * V_{DD} <$ Max Power Constraint

(b) SR= dVo / dt maximum V/µs

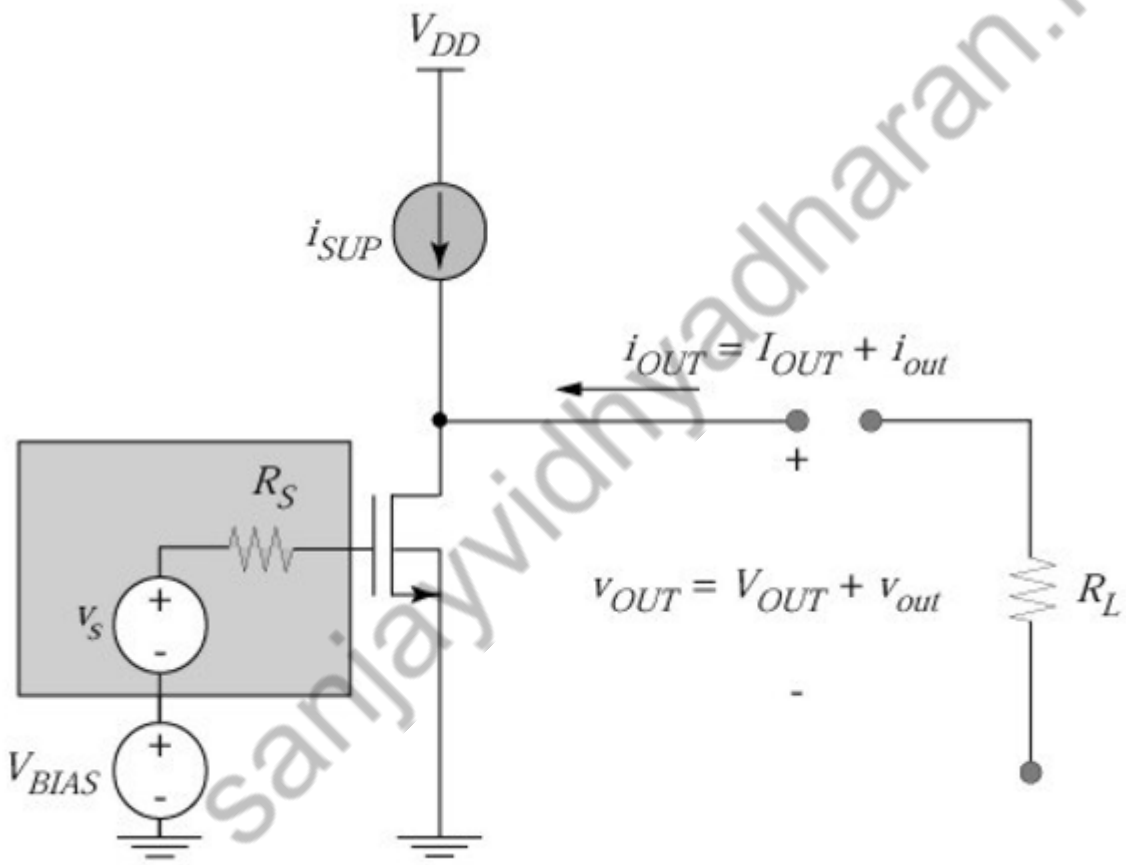
SR= I_{DQ} / C_{Load}

2. Fix R_D for Max Symmetrical Output swing

$R_D = (0.9\ V_{DD} - V_{ov}) / 2I_{DQ}$

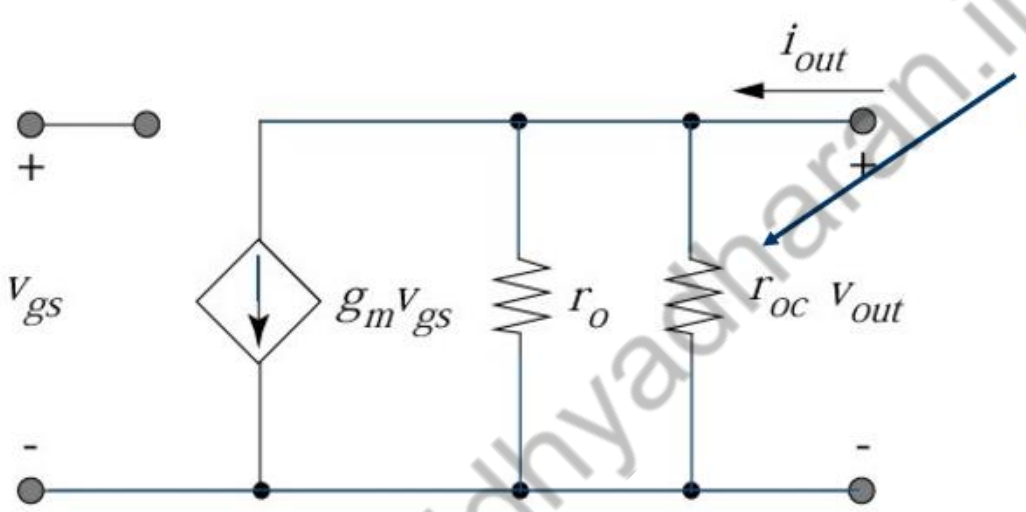
3. $R_S = 0.1\ V_{DD} / I_{DQ}$

CS Amp with Current Source Supply



Gain = ?

CS Amp with Current Source Supply

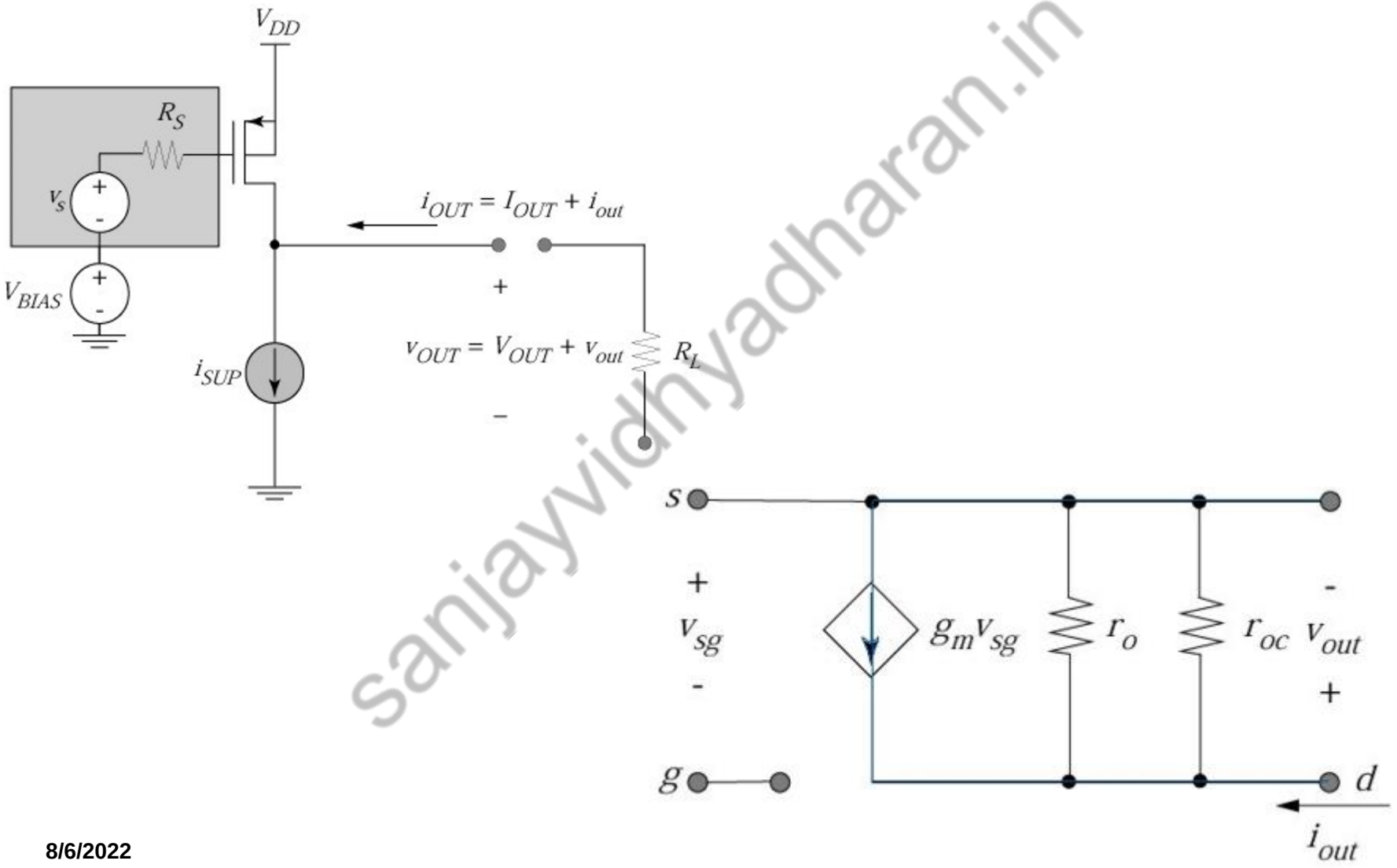


$$R_{in} = \infty$$

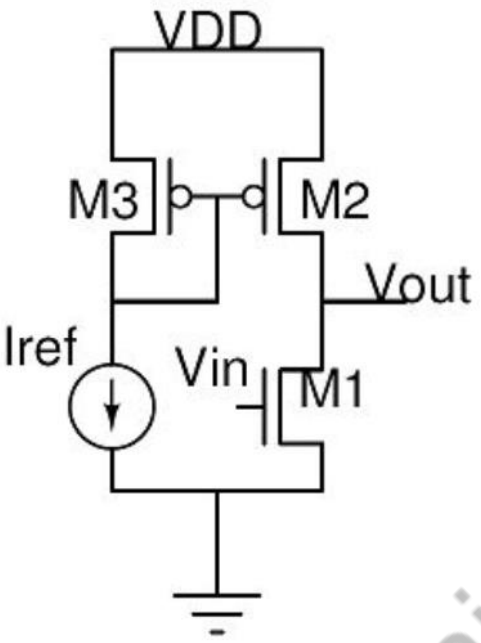
$$G_m = g_m$$

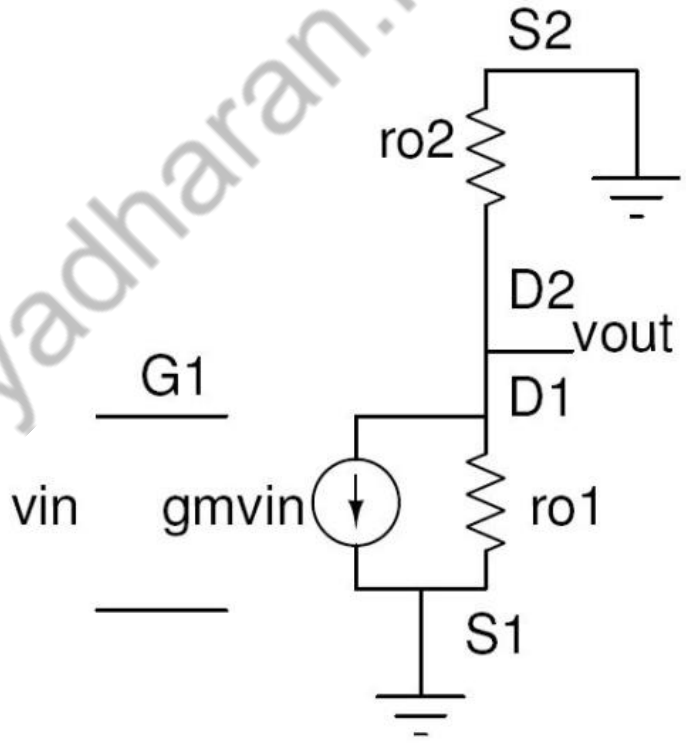
$$R_{out} = r_o \,||\, r_{oc}$$

P-Channel CS Amplifier



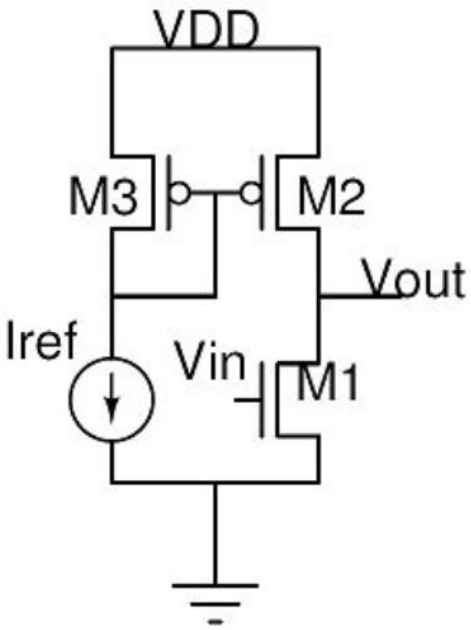
CS Amplifier with Active Load





$$v_{out} = g_{m1} v_{in} * (r_{01} || r_{o2})$$

CS Amplifier with Active Load



Design Steps

1. Fix I_{DQ} Meeting following conditions

(a) $I_{DQ} * V_{DD} <$ Max Power Constraint

(b) SR= dVo / dt maximum V/µs

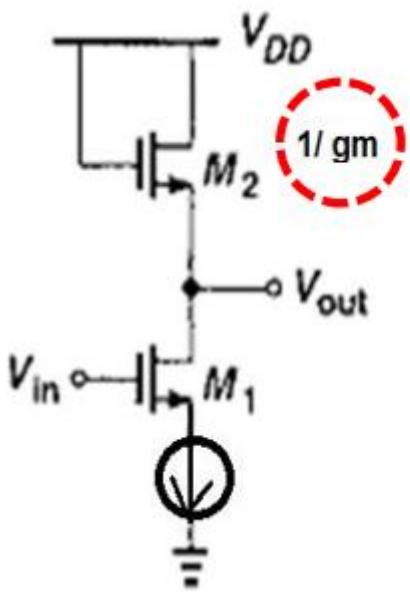
SR= I_{DQ} / C_{load}

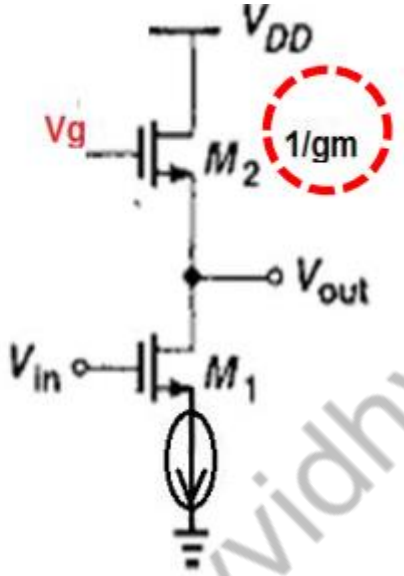
2. $Gain = g_m(r_{01} || r_{02} || R_L)$

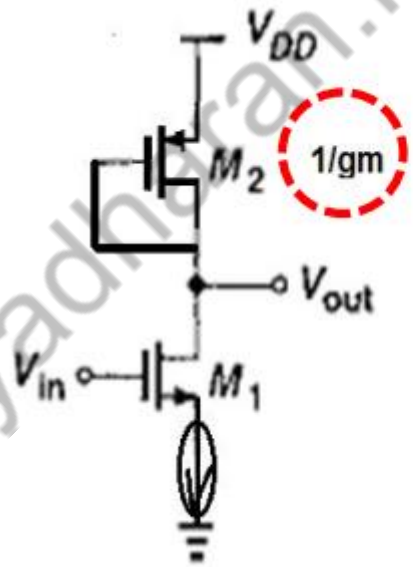
$$g_m = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right) I_D}$$

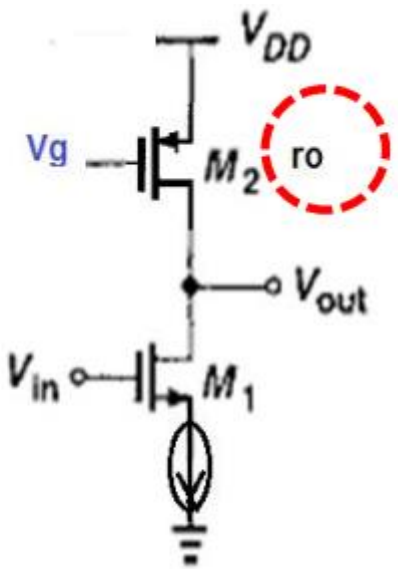
$$g_m = \mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{Tn})\,(1 + \lambda_n V_{DS})$$

Active Loads

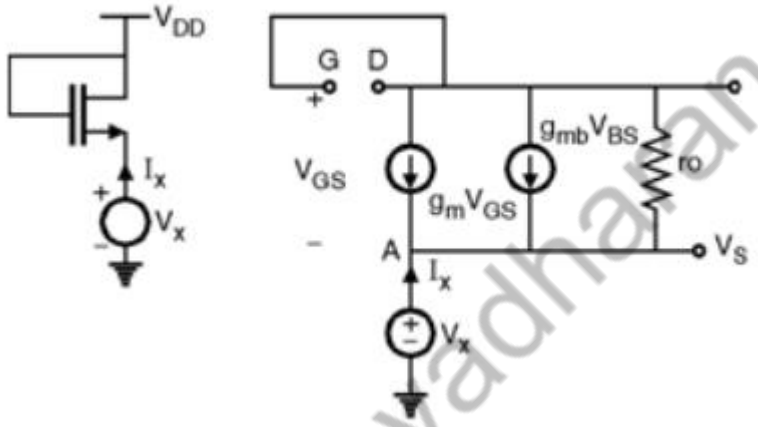








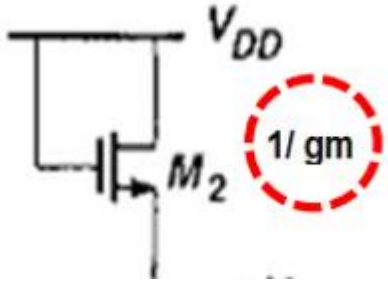
Active Loads



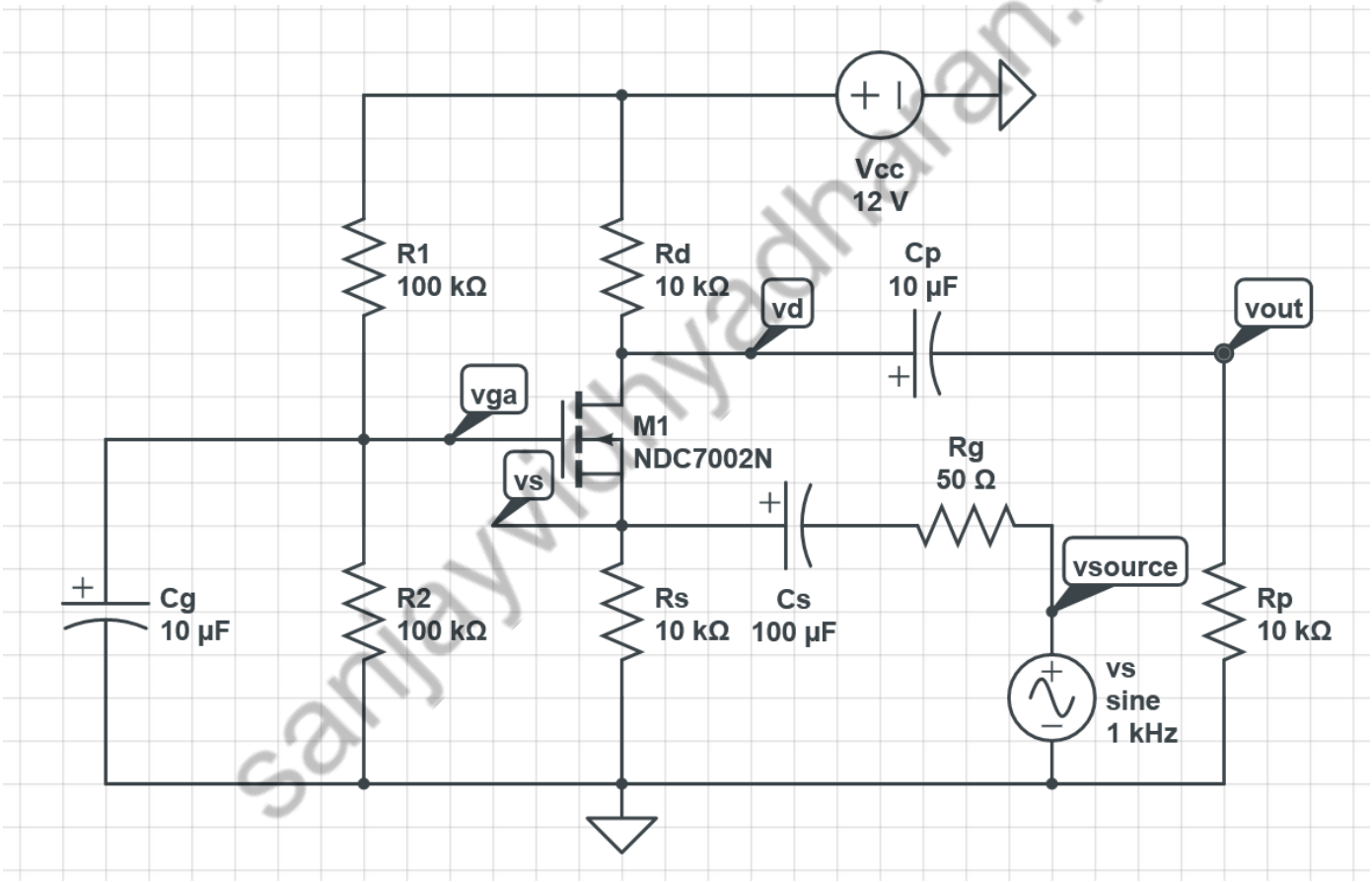
By applying KVL,.
We have, $V_{GS} = V_G - V_S = - V_x$
$V_{BS} = V_B - V_S = - V_x$ [Body is connected to ground]

By applying KCL at Node A, We get,
$I_x + g_m V_{GS} + g_{mb} V_{BS} - V_x/r_o = 0$

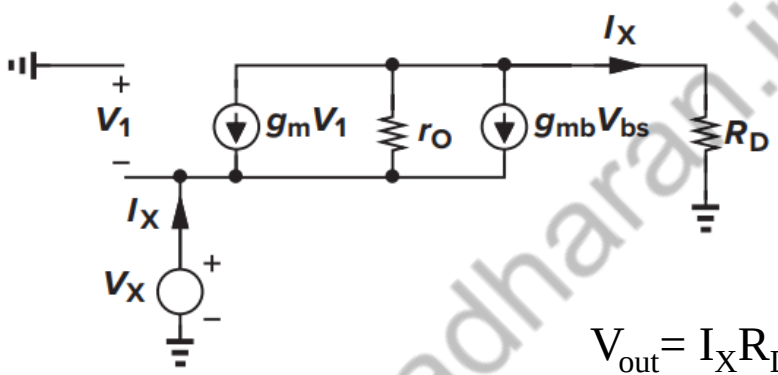
i.e. $I_x = g_m V_x + g_{mb} V_x + V_x/r_o$



Common Gate Amplifier



Common Gate Amplifier



$$V_1 = -V_X$$

$$R_D I_X + r_O[I_X - (g_m + g_{mb})V_X] = V_X$$

$$\frac{V_X}{I_X} = \frac{r_O}{1 + (g_m + g_{mb})r_O}$$

$$= \frac{1}{\frac{1}{r_O} + g_m + g_{mb}}$$

$V_{out} = I_X R_D$

Gain $= R_D (1/r_o + g_m + g_{mb})$

Gain $\simeq R_D (g_m + g_{mb})$

Advantages ??

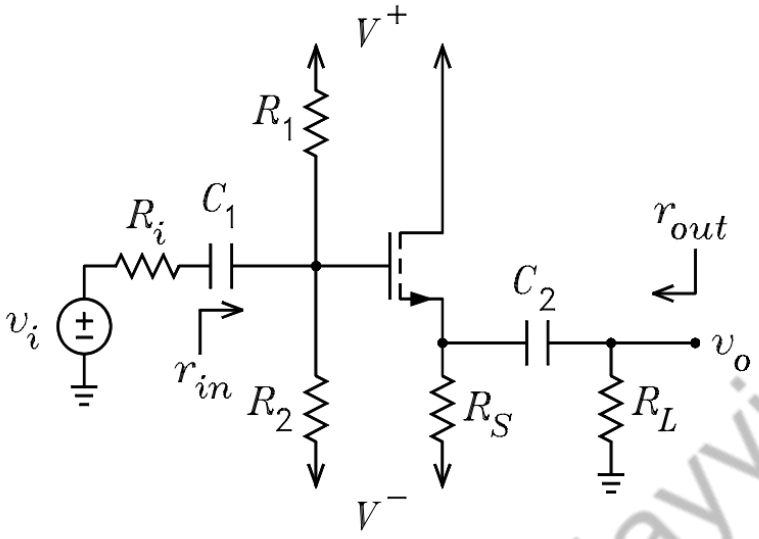
Low I/P Impedance

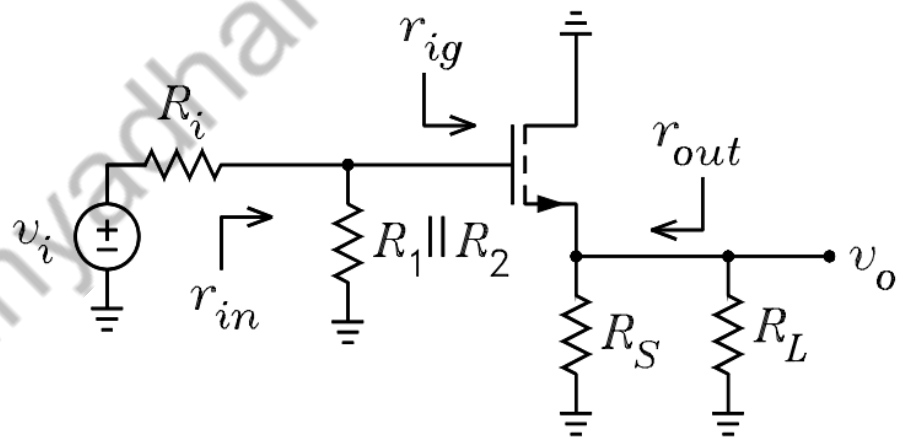
High Frequency Applications

Gain is a function of Load Resistance
Low Input Impedence
Low Miller Capacitance
~~Current~~, Voltage and Power Gain

Simulation

Common Drain Amplifier





Assuming $R_1||R_2 >> r_{in}$

$V_{in} = V_{gs} + V_{out}$

Common Drain Amplifier

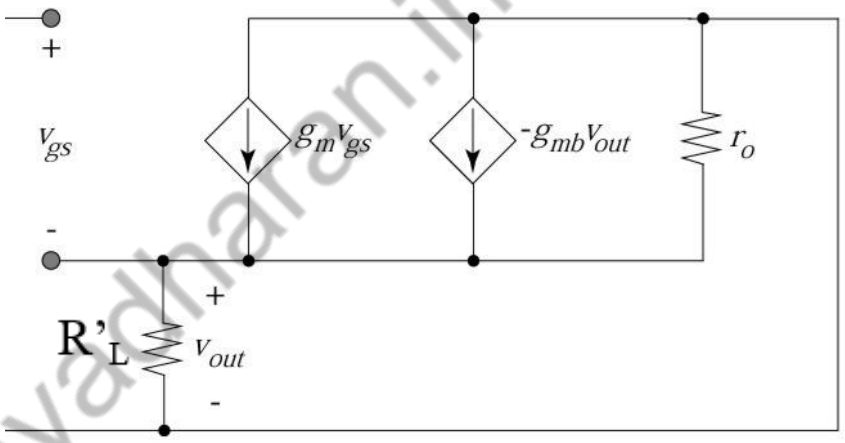
$$V_{in} = V_{gs} + V_{out}$$

$$\frac{v_{out}}{R_L' || r_o} = g_m v_{gs} - g_{mb} v_{out}$$

$$\frac{v_{out}}{R_L' || r_o} = g_m (v_{in} - v_{out}) - g_{mb} v_{out}$$

$$\frac{v_{out}}{v_{in}} = \frac{g_m}{\frac{1}{R'_L || r_o} + g_{mb} + g_m}$$

$$\frac{v_{out}}{v_{in}} \approx \frac{g_m}{g_{mb} + g_m} \approx 1$$



Advantages ??

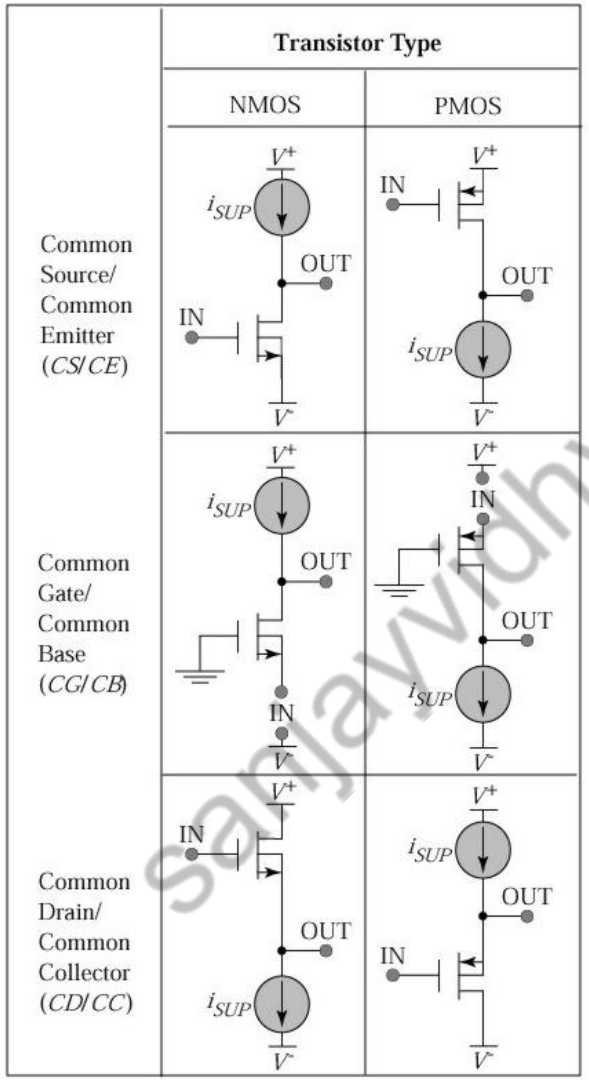
Low O/P Impedance

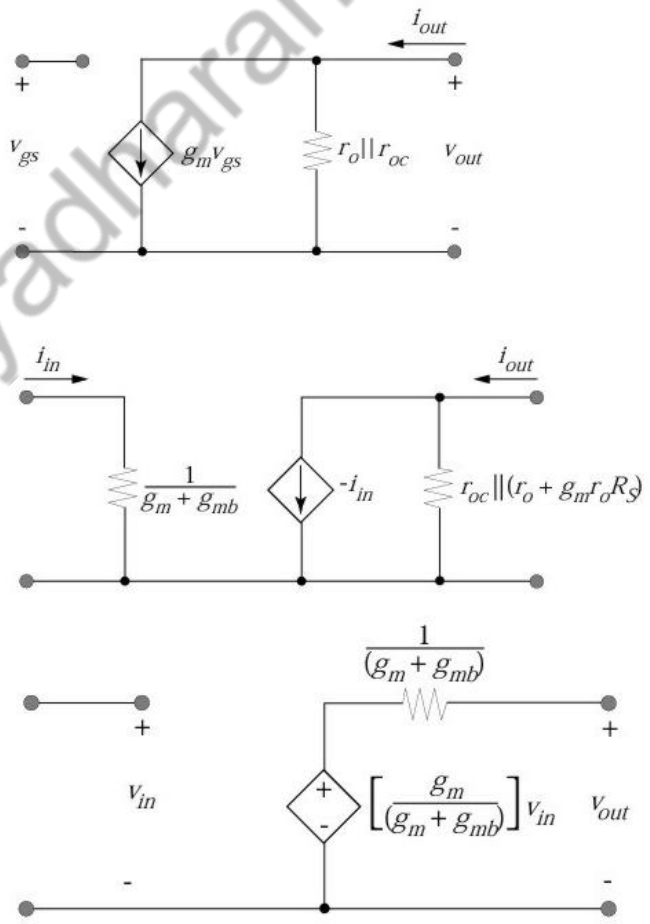
$$R_{out} \approx \frac{1}{g_m + g_{mb}}$$

*Gain is a **NOT** function of Load Resistance*
~~Current~~, ~~Voltage~~ and Power Gain

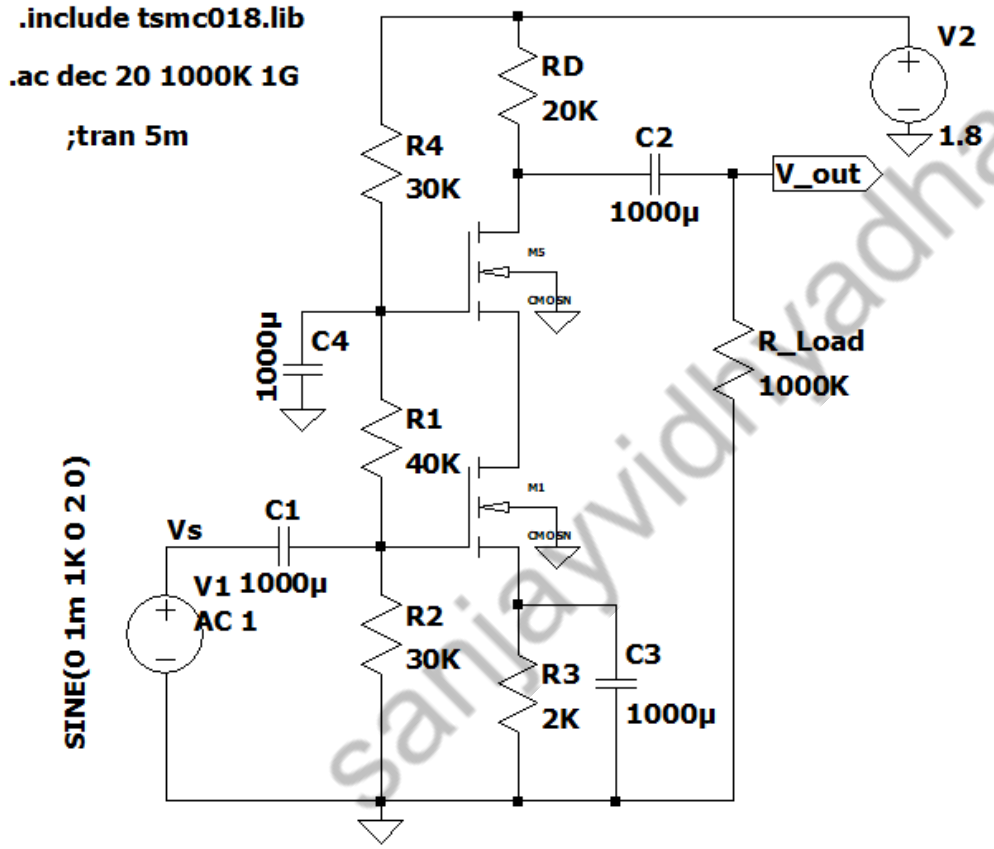
Simulation

Summary of CS, CG & CD Amplifiers with Current Source Bias





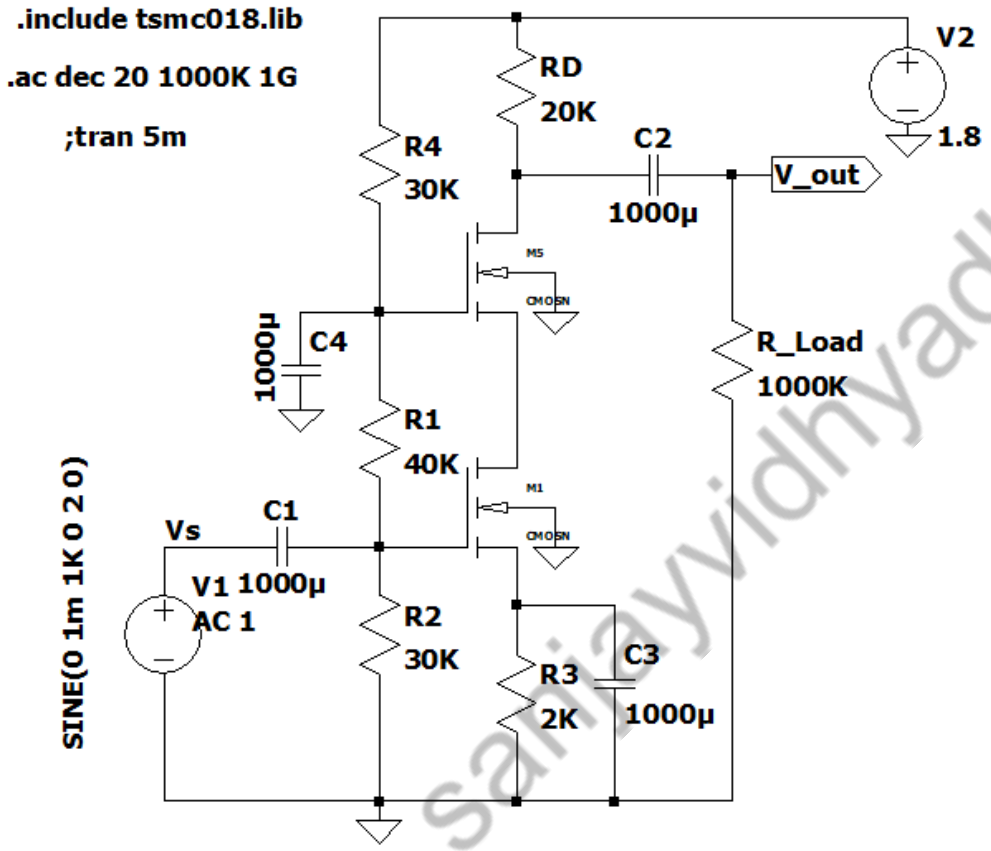
Telescopic Cascode Amplifier

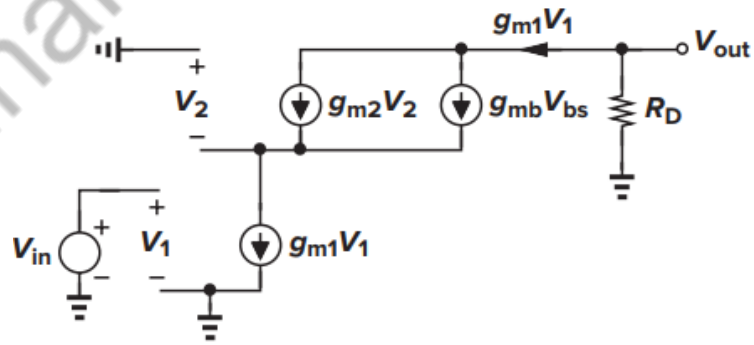


$Gain \sim -g_m R_D$

Advantages ??

Telescopic Cascode Amplifier





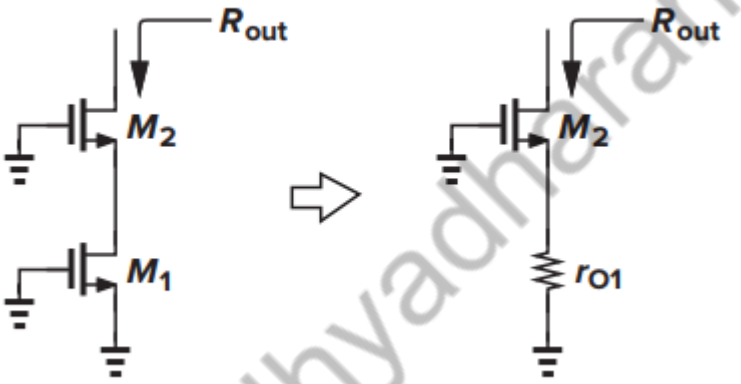
$Gain \sim -g_m R_D$

Advantages ??

Simulation

Telescopic Cascode Amplifier

Cascode Amplifier Output Resistance



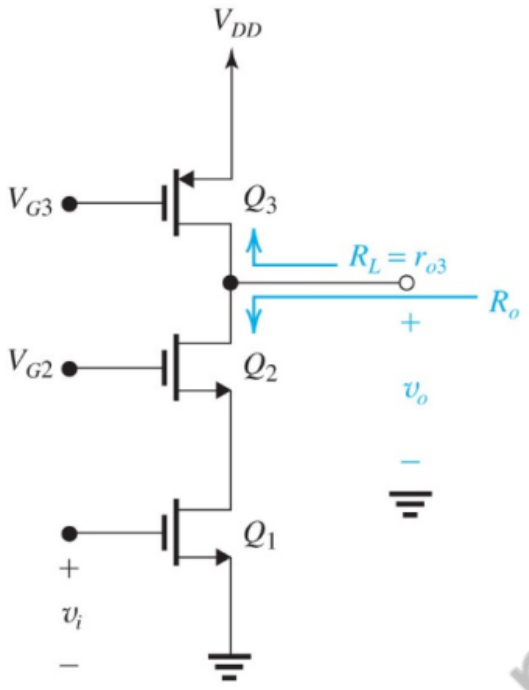
$$i_{out} = -g_{m2}\, i_{out} r_{o1} - -g_{mb2}\, i_{out} r_{o1} + \frac{v_{out} - i_{out}\, r_{o1})}{r_{o2}}$$

$$i_{out}((g_{m2} + g_{mb2})\, r_{o1}\, r_{o2} + r_{o1} + r_{o2}) = v_{out}$$

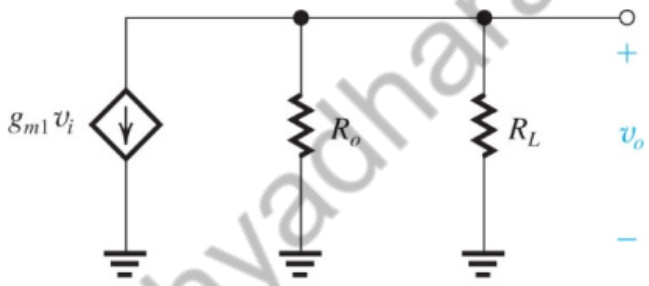
$$R_{out} \approx (g_{m2} + g_{mb2}) r_{O2} r_{O1}$$

Telescopic Cascode Amplifier

Cascode Amplifier with Simple Active Load



(a)



(b)

$$A_v = -g_{m1}(R_o \parallel R_L)$$

$$R_o \approx (g_{m2}r_{o2})r_{o1}$$

$$R_L = r_{o3} << R_o$$

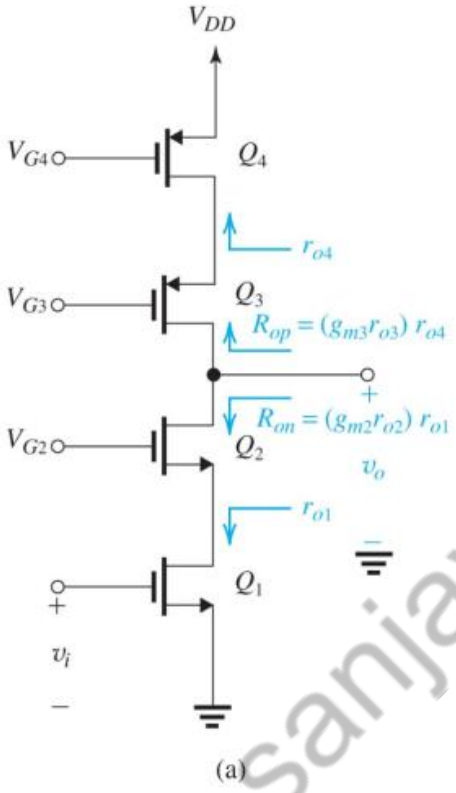
$$A_v = -g_{m1}r_{o3}$$

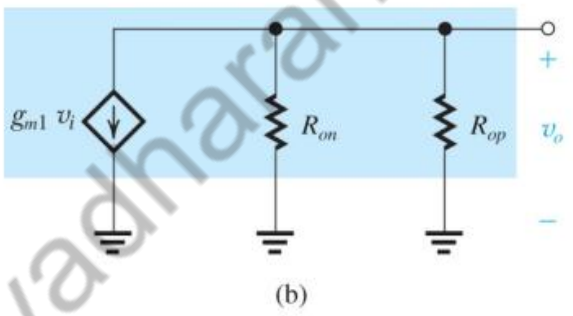
Similar gain as CS amplifier.

No gain boosting.

Telescopic Cascode Amplifier

Cascode Amplifier with Cascode Current-Source Load





$$A_v = -g_{m1}(R_{on} \parallel R_{op})$$

$$R_{on} \approx (g_{m2}r_{o2})r_{o1}$$

$$R_{op} \approx (g_{m3}r_{o3})r_{o4}$$

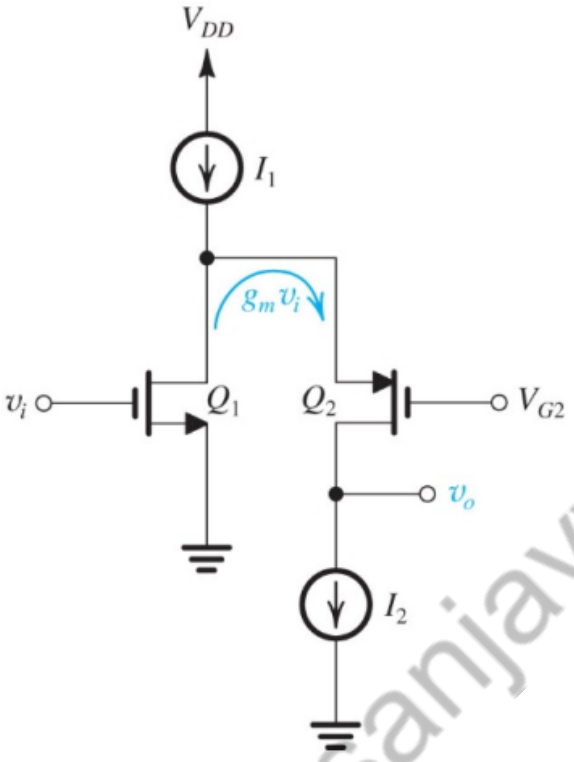
If all transistors are similar :

$$A_v = -\frac{1}{2}(g_m r_o)^2$$

--> High gain !

Disadvantages ??

Folded Cascode Amplifier



"Folding" the CG stage using PMOS.

Q_1 is biased with $I_1 - I_2$

Q_2 is biased with I_2

Folded cascode avoids stacking too many transistors vertically, which will be difficult for low power supply voltage V_{DD}

Folded Cascode Amplifier

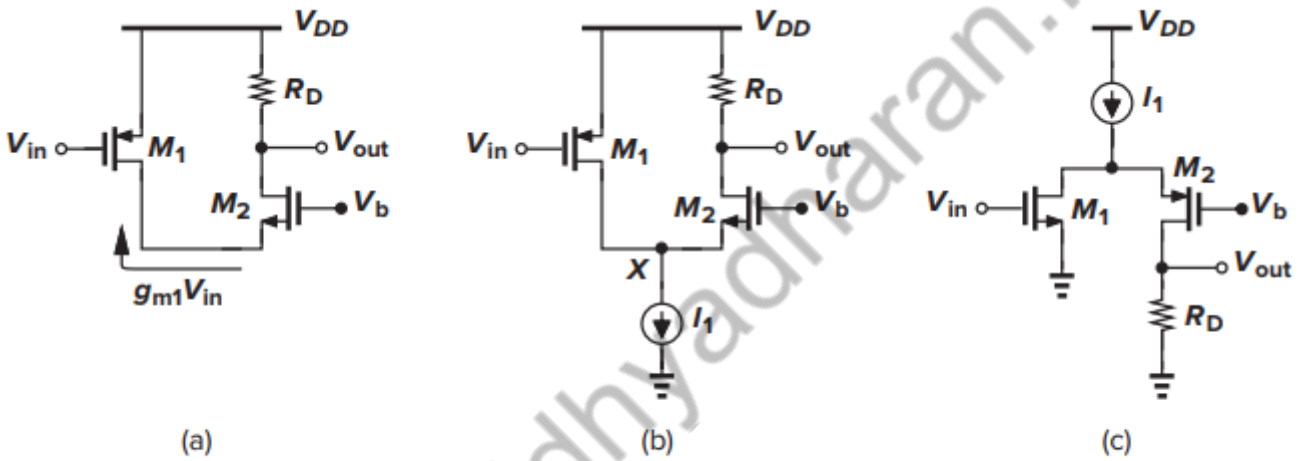
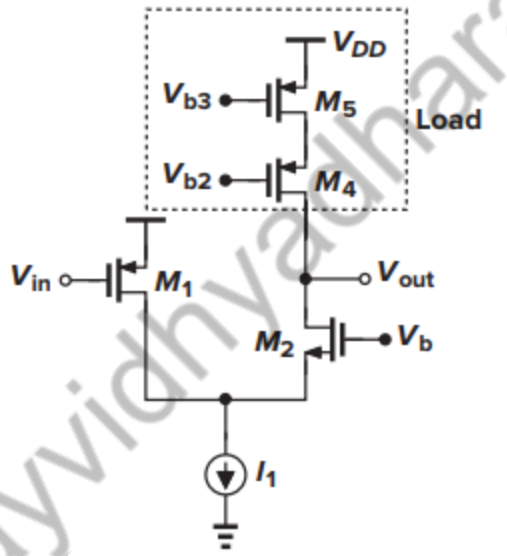


Figure 3.74 (a) Simple folded cascode; (b) folded cascode with proper biasing; (c) folded cascode with NMOS input.

Source: Design of Analog CMOS Integrated Circuits by Behzad Razavi

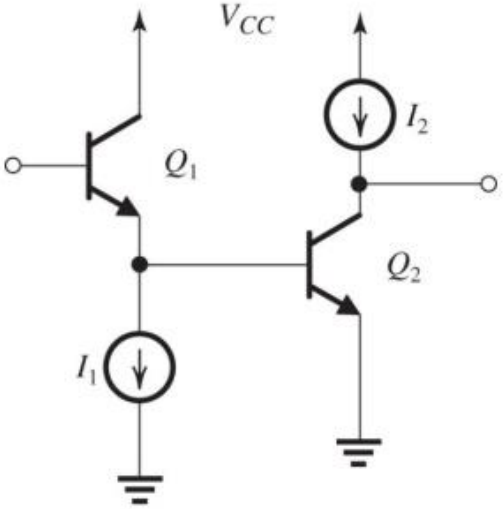
Folded Cascode Amplifier

Folded cascode with cascode load.



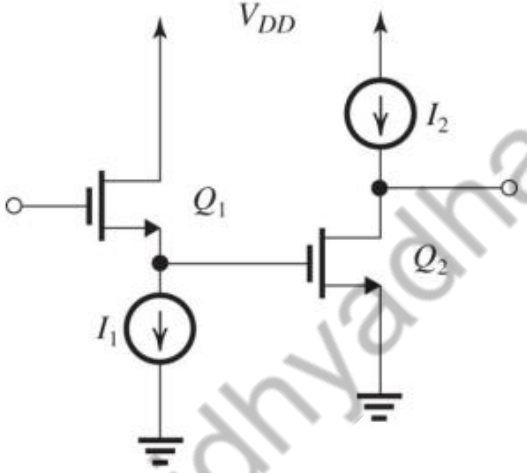
Source: Design of Analog CMOS Integrated Circuits by Behzad Razavi

Useful Transistor Pairings



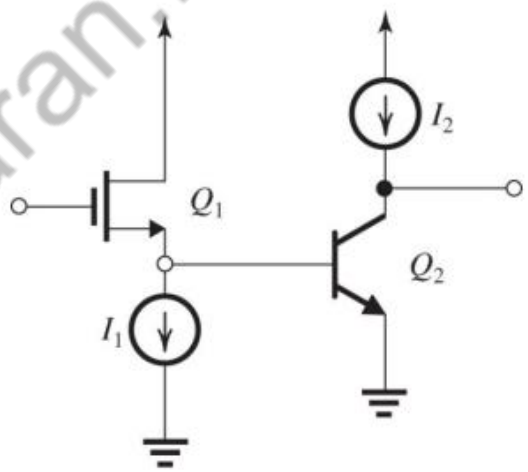
CC + CE

- **High input resistance**
- **Much wider bandwidth than single CE amplifier (To be discussed later)**



CD + CS

- **Main benefit is wider bandwidth than single CE amplifier**



CD + CE
in BiCMOS technology (BJT+CMOS)

- **Similar to MOS version but use BJT for higher g_m**

Thank you