



Analog IC Design : 2022-23

Lecture 2

MOSFET Single Stage Amplifiers Part-1

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MOSFET Large Signal Equivalent

Based on content from
Sedra/Smith “Microelectronic Circuits” -
Fifth Edition

MOSFET Large Signal Equivalent

Cut-off Region

For $V_{GS} < V_T$ $I_D = 0$

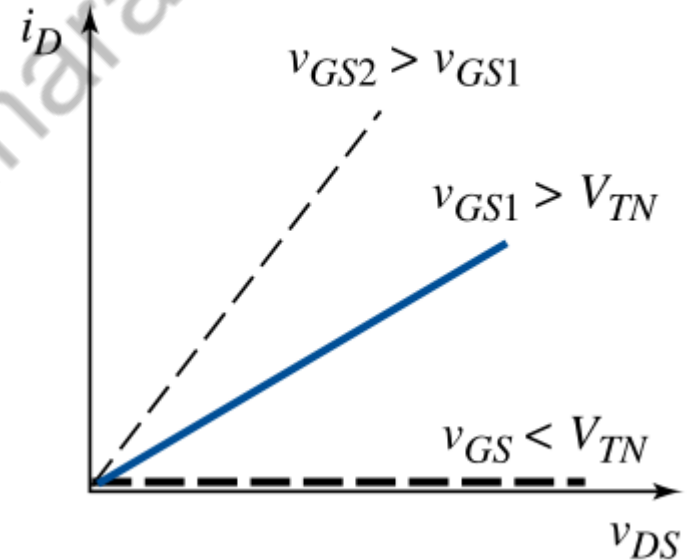
Linear Region- Small V_{DS}

$$I_D = \frac{\mu_n C_{ox} W (V_{GS} - V_T) V_{DS}}{L}$$

$$\text{Transconductance of Channel } g_{DS} = \frac{\mu_n C_{ox} W V_{ov}}{L}$$

Process transconductance parameter $k'_n = \mu_n C_{ox}$

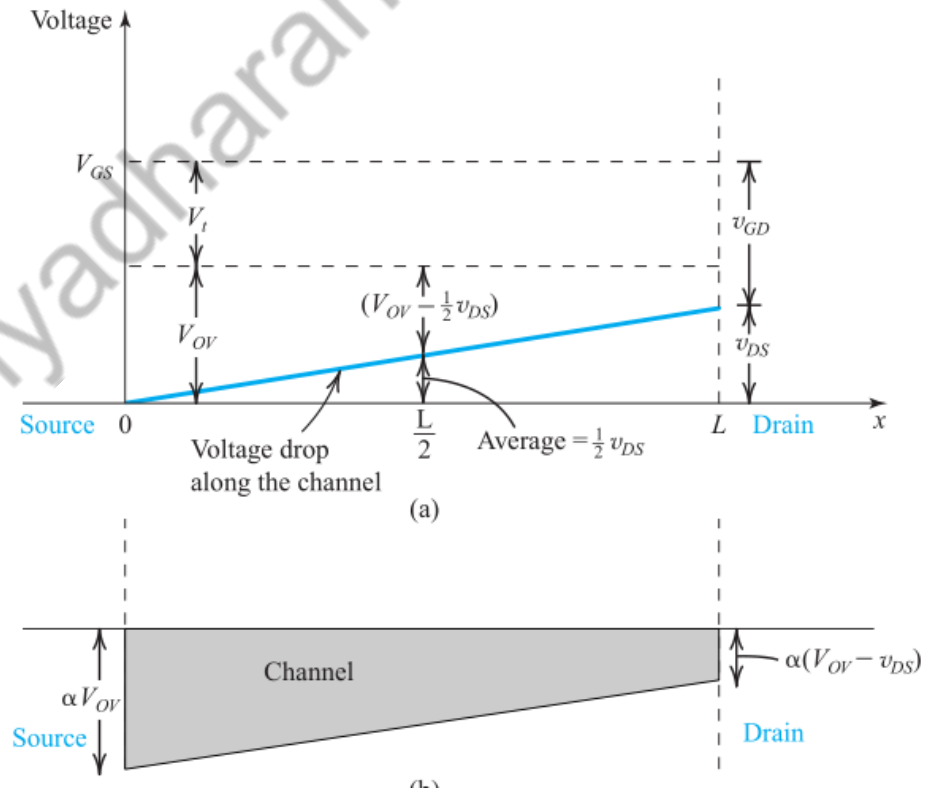
$$I_D = \frac{k'_n W V_{ov} V_{DS}}{L}$$



MOSFET Large Signal Equivalent

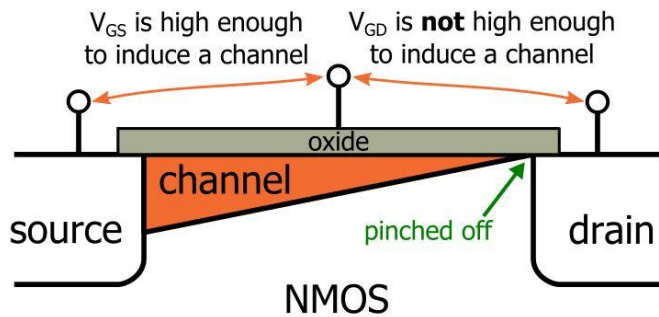
Linear Region as V_{DS} is Increased

$$I_D = \frac{k'_n W (V_{ov} - \frac{V_{DS}}{2}) V_{DS}}{L}$$



MOSFET Large Signal Equivalent

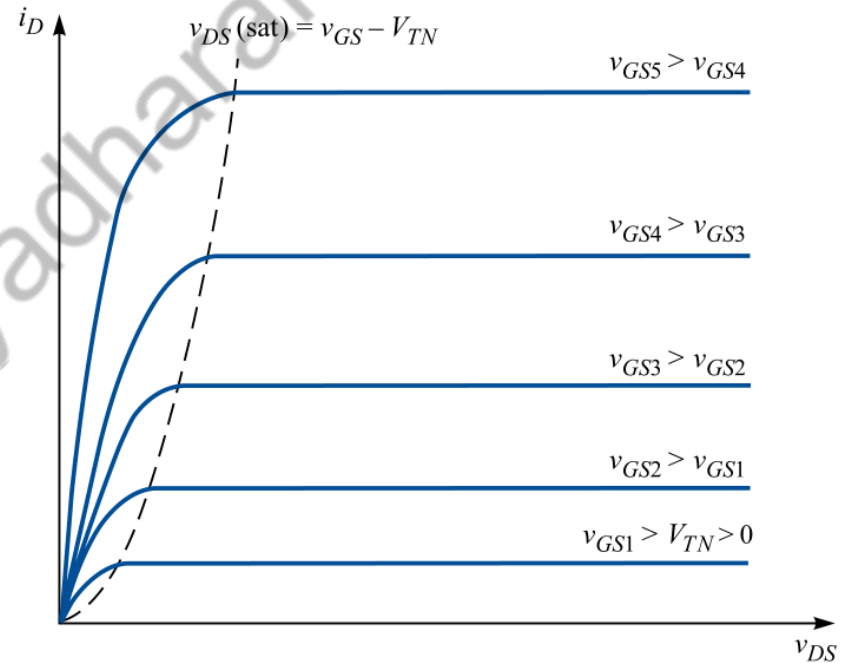
Saturation Region



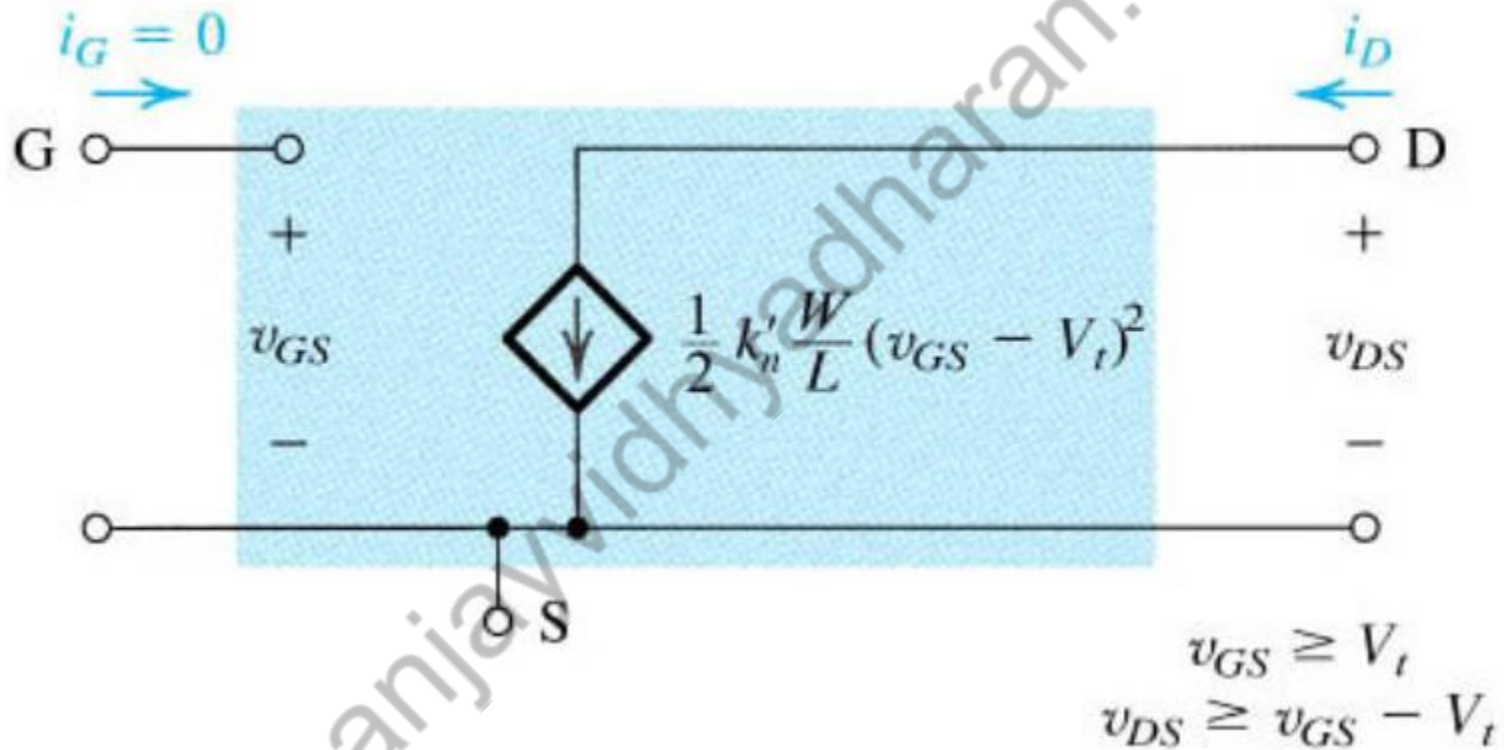
$$V_{DS} = V_{ov} = V_{GS} - V_T$$

$$I_D = \frac{k'_n W (V_{ov} - \frac{V_{DS}}{2}) V_{DS}}{L}$$

$$I_D = \frac{k'_n W (V_{GS} - V_T)^2}{2L}$$

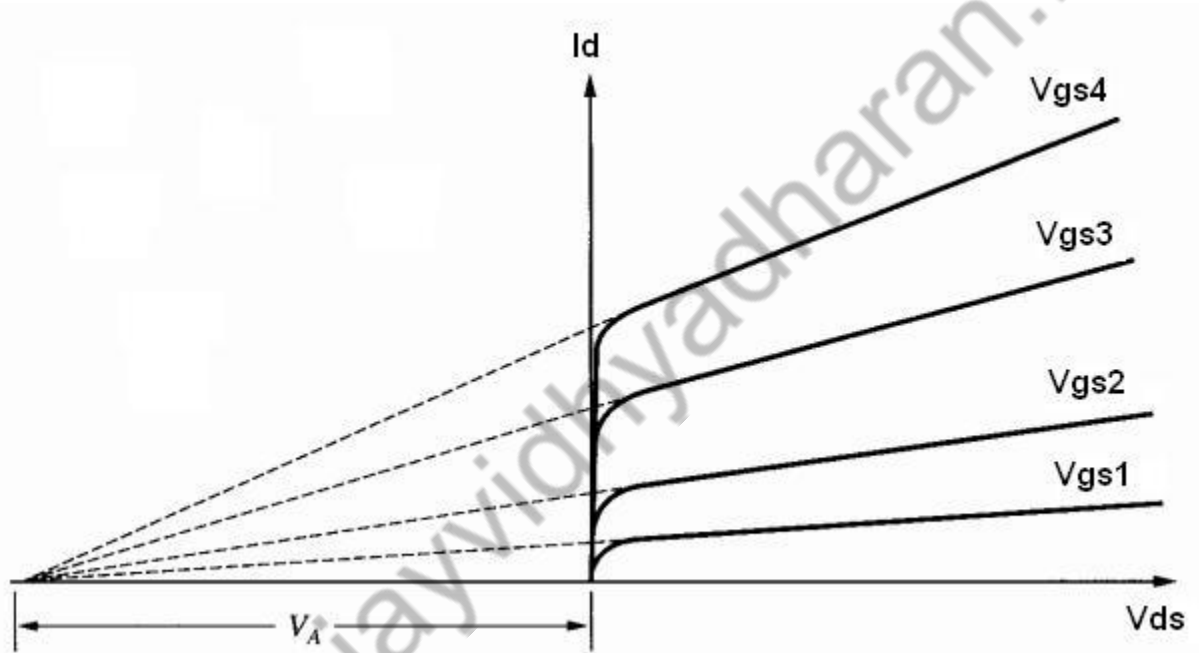


MOSFET Large Signal Equivalent



MOSFET Large Signal Equivalent

Channel Length Modulation



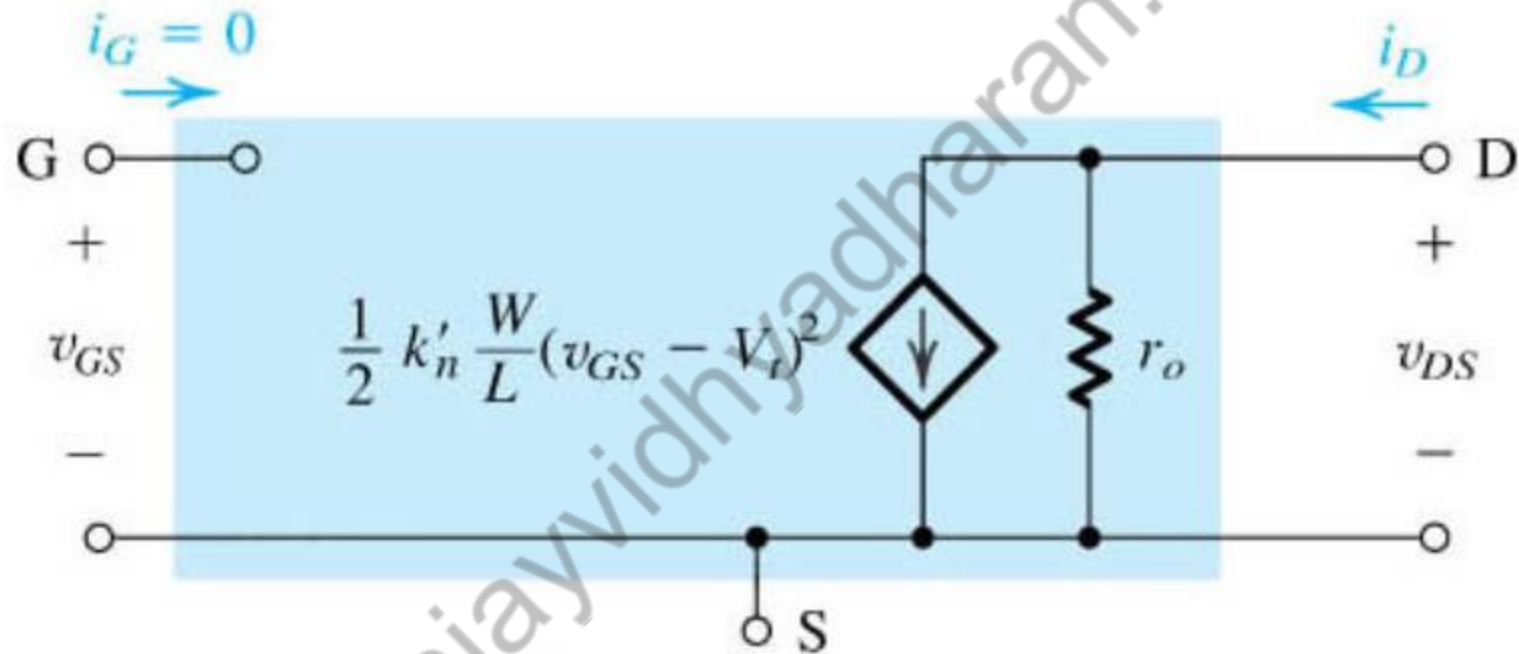
V_A Early Voltage

$$\lambda = \frac{1}{V_A}$$

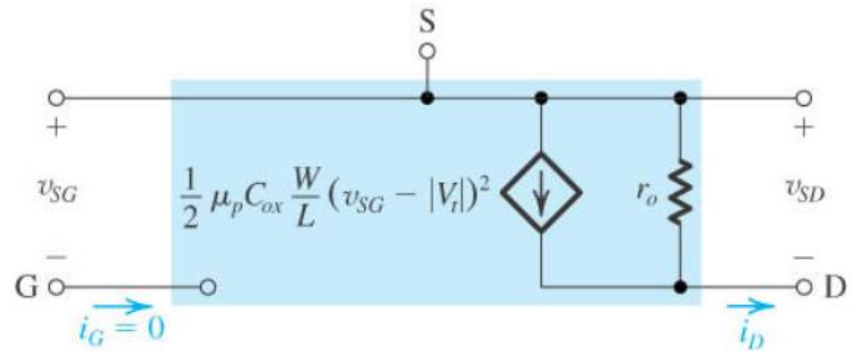
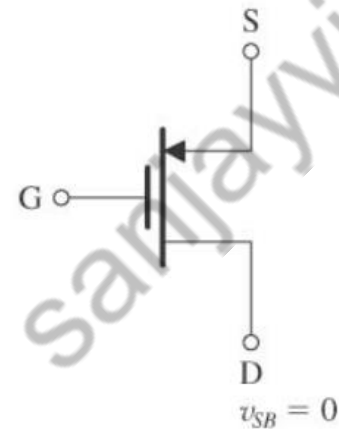
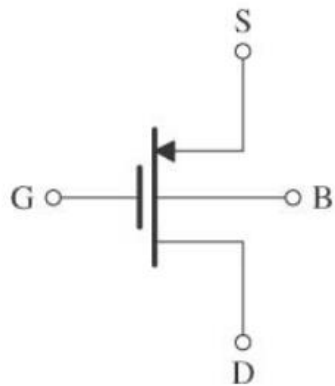
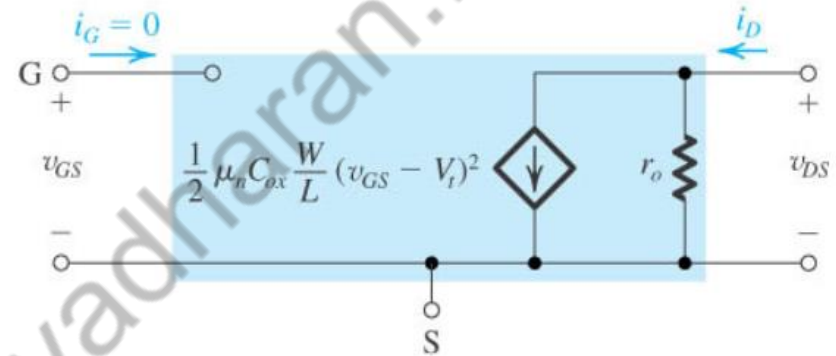
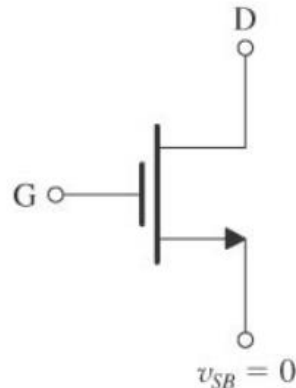
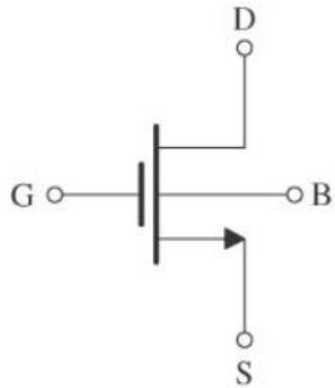
$$r_o \approx \frac{1}{\lambda I_D}$$

$$\lambda \propto 1/L$$

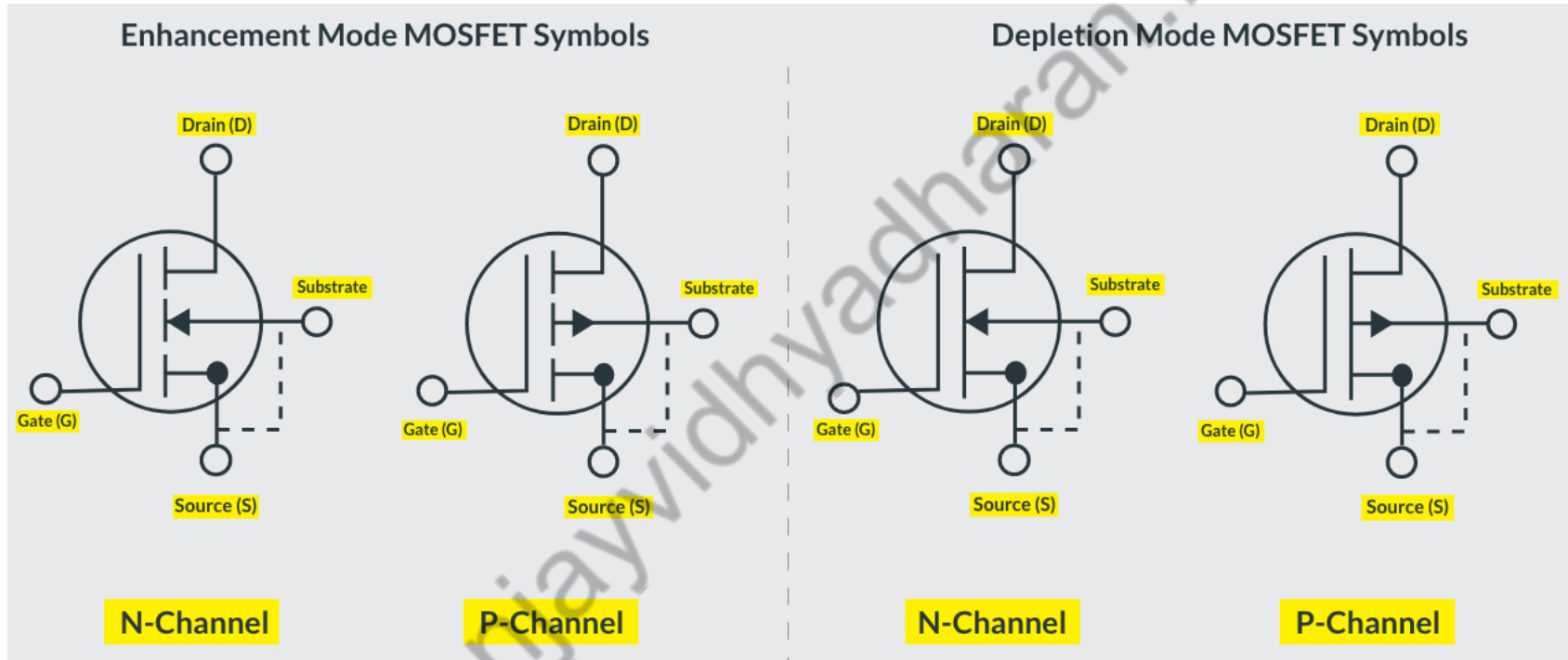
MOSFET Large Signal Equivalent



MOSFET Large Signal Equivalent

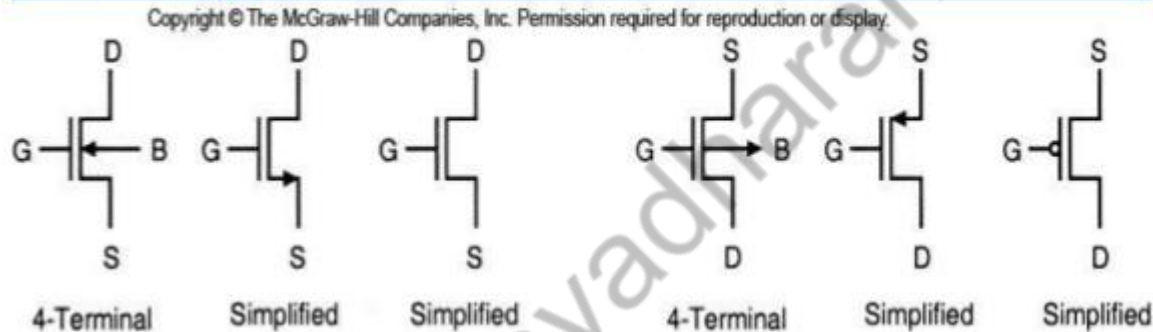


Circuit Symbols



Circuit Symbols

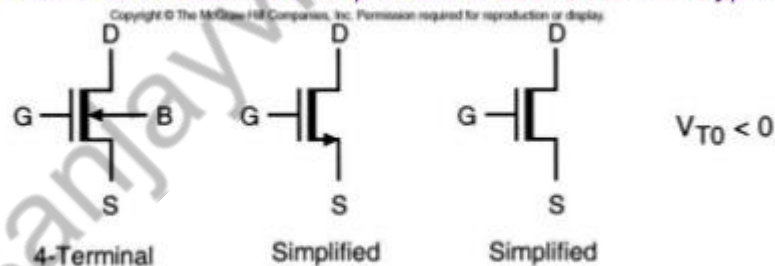
Circuit symbols



n-channel MOSFET

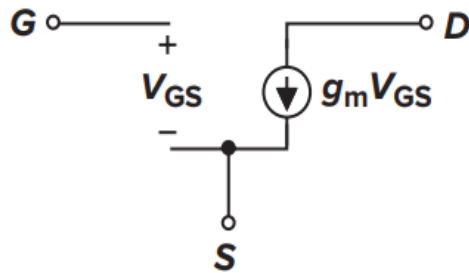
p-channel MOSFET

Circuit symbols for n-channel and p-channel enhancement-type MOSFETs

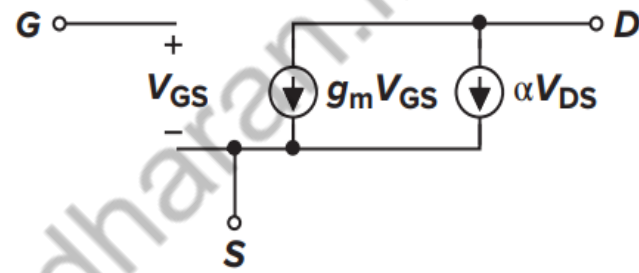


Circuit symbols for n-channel depletion-type MOSFETs

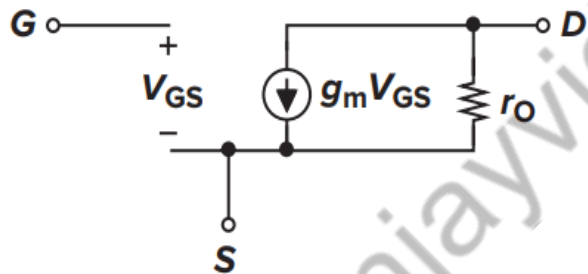
MOSFET Small Signal Equivalent



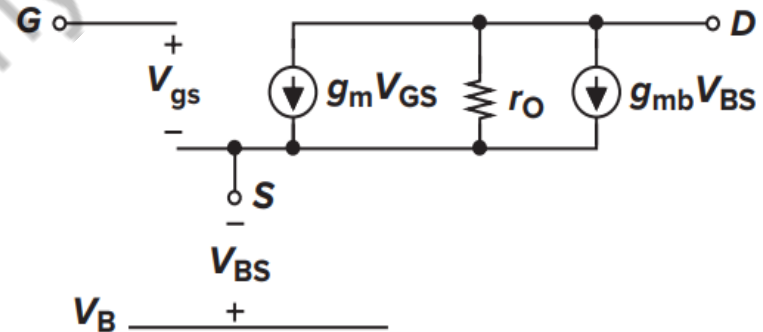
(a)



(b)



(c)



(d)

MOSFET Small Signal Equivalent

Small Signal Modelling

Find an equivalent circuit which relates the incremental changes in i_D , v_{GS} , v_{DS} , etc.

Since the changes are small, the small-signal equivalent circuit has **linear** elements only (e.g., capacitors, resistors, controlled sources)

$$v_{GS} = V_{GS} + v_{gs}, i_D = I_D + i_d$$

$$i_D = (1/2) \mu_n C_{ox} (W/L) (v_{GS} - V_{Tn})^2 (1 + \lambda_n v_{DS}) = i_D(v_{GS}, v_{DS}, v_{BS})$$

$$(V_{GS} - V_{Tn})^2 + 2(V_{GS} - V_{Tn}) v_{gs} + v_{gs}^2$$

$$g_m = \mu_n C_{ox} \left(\frac{W}{L} \right) (V_{GS} - V_{Tn}) (1 + \lambda_n V_{DS})$$

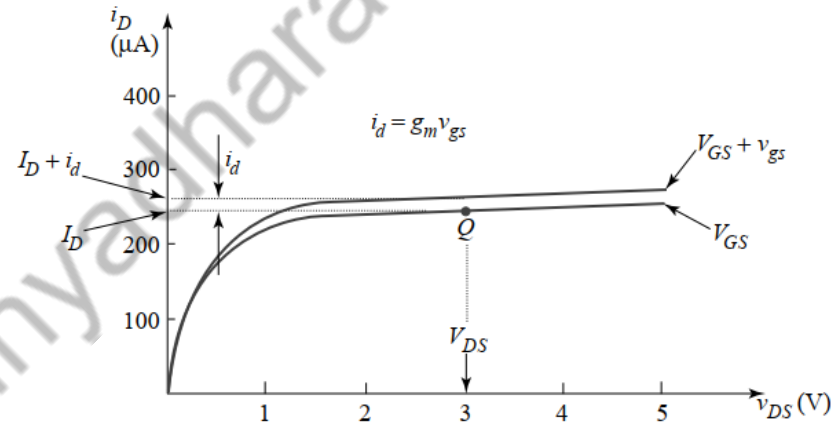
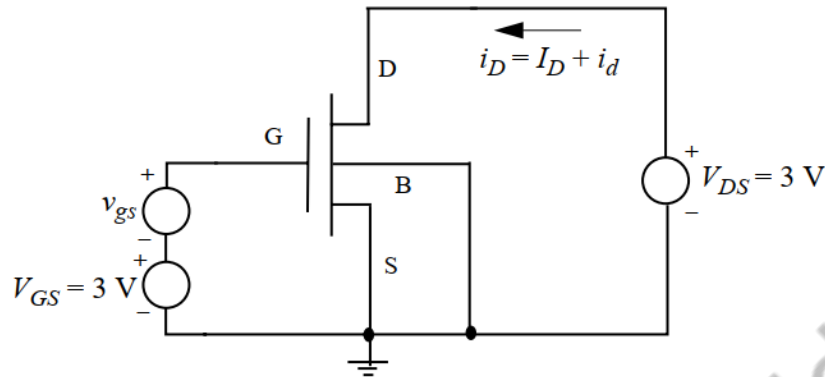
$$g_m = \mu_n C_{ox} \left(\frac{W}{L} \right) (V_{GS} - V_{Tn}) \quad \text{Neglecting CLM}$$

$$g_m = \sqrt{2 \mu_n C_{ox} \left(\frac{W}{L} \right) I_D}$$

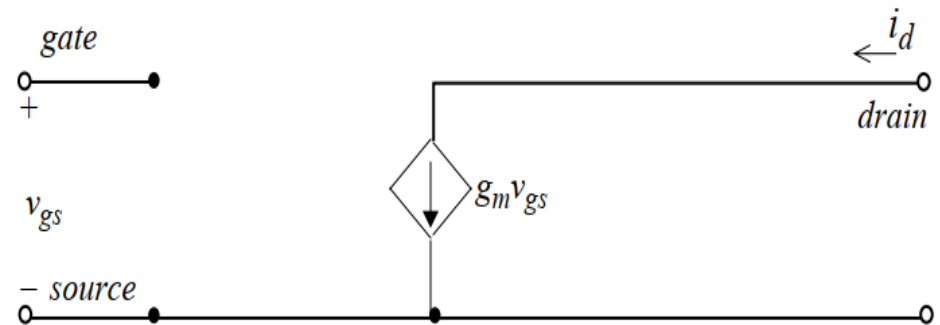
MOSFET Small Signal Equivalent

Transconductance

The small-signal drain current due to v_{gs} is given by $i_d = g_m v_{gs}$.

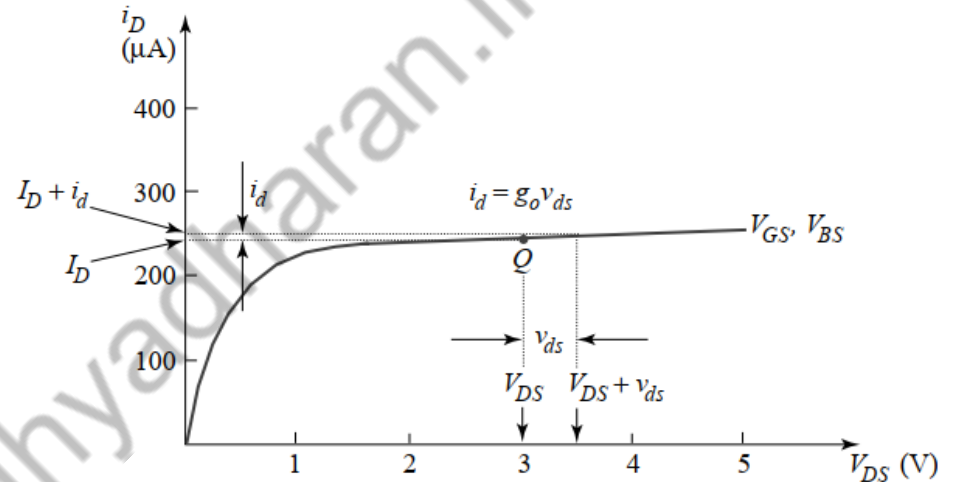
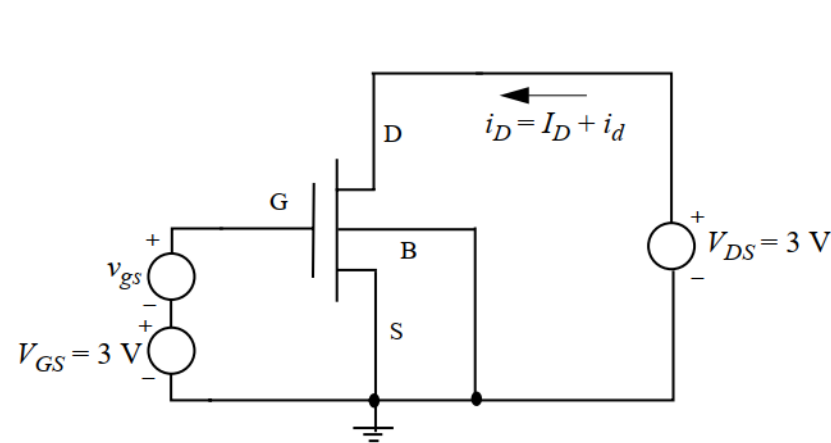


$$g_m = \sqrt{2\mu_n C_{ox} \left(\frac{W}{L}\right) I_D}$$



MOSFET Small Signal Equivalent

Output Conductance

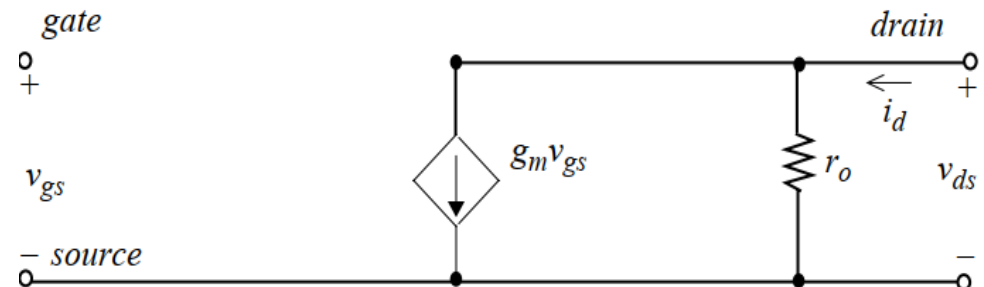


$$i_D = (1/2) \mu_n C_{ox} (W/L) (v_{GS} - V_{Tn})^2 (1 + \lambda_n v_{DS})$$

$$g_o = \left. \frac{\partial i_D}{\partial v_{DS}} \right|_Q = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L} \right) (V_{GS} - V_T)^2 \lambda_n \equiv \lambda_n I_D$$

$$r_o = \frac{1}{g_o} = \frac{1}{\lambda_n I_D}$$

$$i_d = g_m v_{gs} + (1/r_o) v_{ds}$$



MOSFET Small Signal Equivalent

Backgate Transconductance

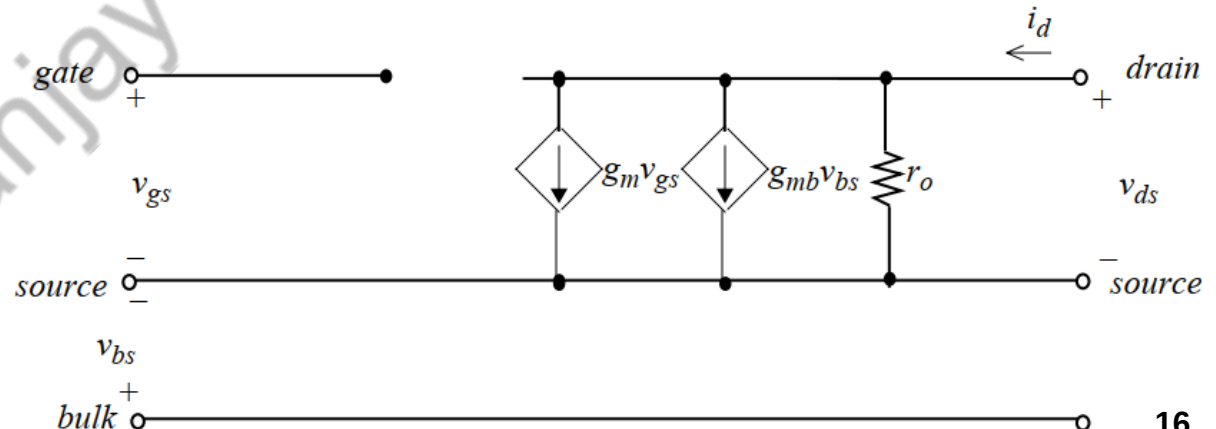
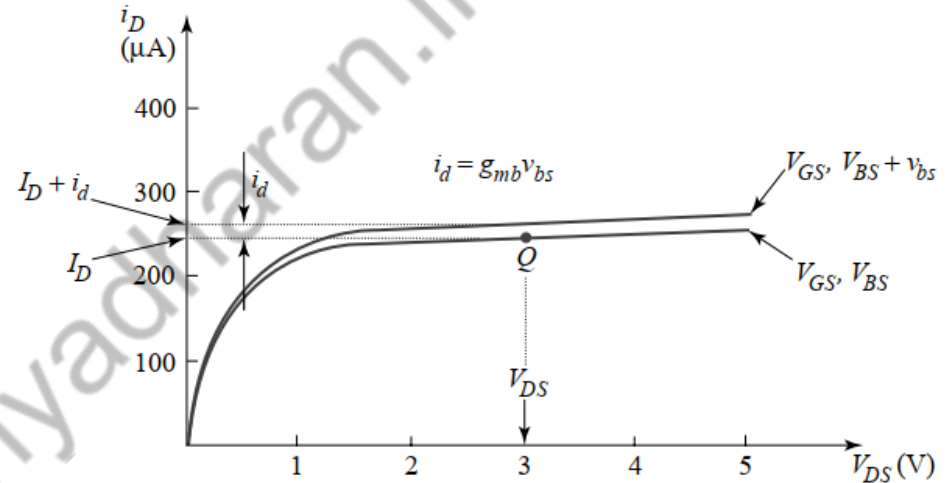
$$i_D = (1/2) \mu_n C_{ox} (W/L) (v_{GS} - V_{Tn})^2 (1 + \lambda_n v_{DS})$$

$$g_{mb} = \left. \frac{\partial i_D}{\partial v_{BS}} \right|_Q = \left. \frac{\partial i_D}{\partial V_{Tn}} \right|_Q \left. \frac{\partial V_{Tn}}{\partial v_{BS}} \right|_Q$$

$$\left. \frac{\partial i_D}{\partial V_{Tn}} \right|_Q = -\mu_n C_{ox} \left(\frac{W}{L} \right) (V_{GS} - V_{Tn}) (1 + \lambda_n V_{DS}) \approx -g_m$$

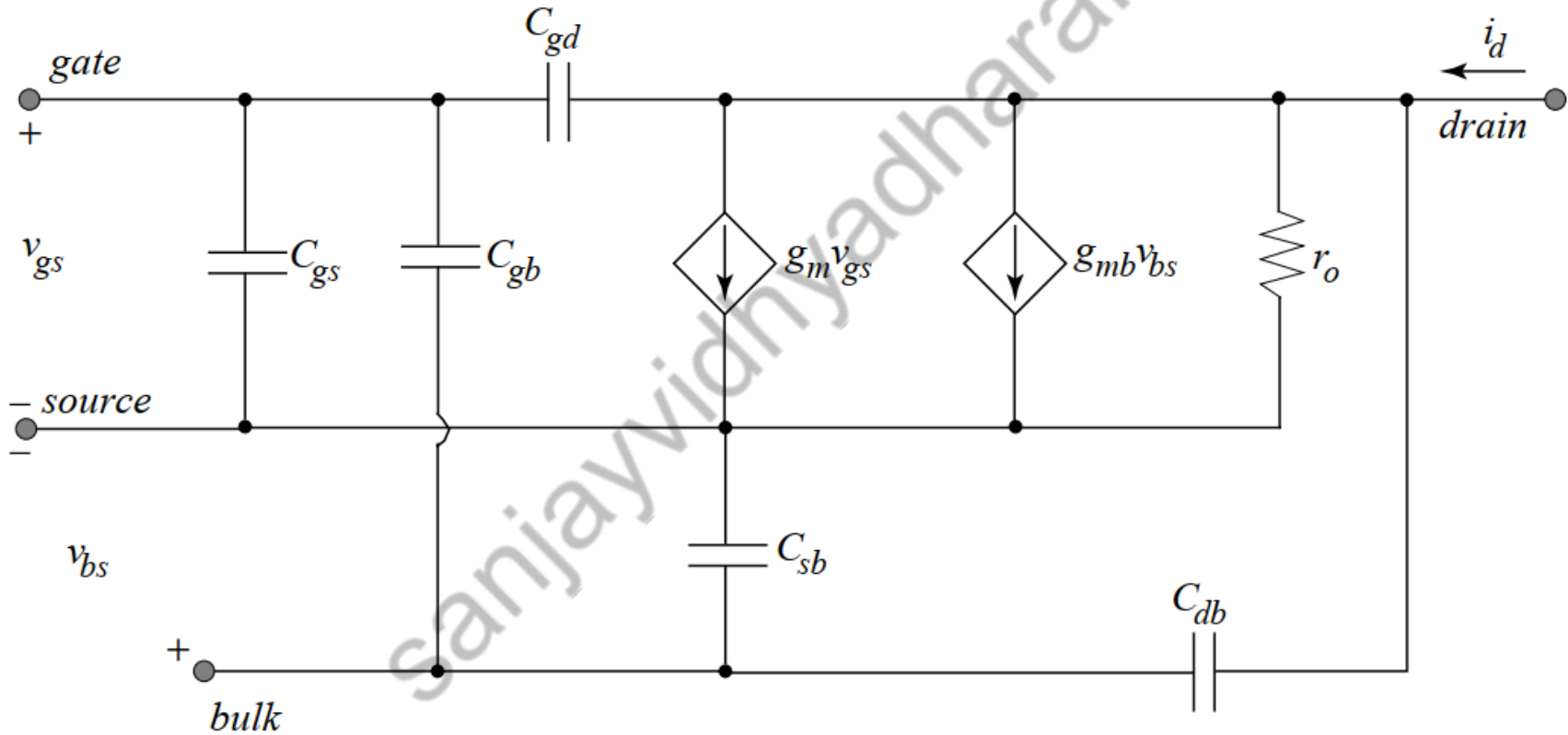
$$V_{TH} = V_{TH0} + \gamma \left(\sqrt{|2\phi_F| + V_{SB}} - \sqrt{|2\phi_F|} \right)$$

$$g_{mb} = (-g_m) \left. \frac{\partial V_{Tn}}{\partial v_{BS}} \right|_Q = (-g_m) \left(\frac{-\gamma_n}{2\sqrt{-2\phi_p - V_{BS}}} \right) = \frac{\gamma_n g_m}{2\sqrt{-2\phi_p - V_{BS}}}$$

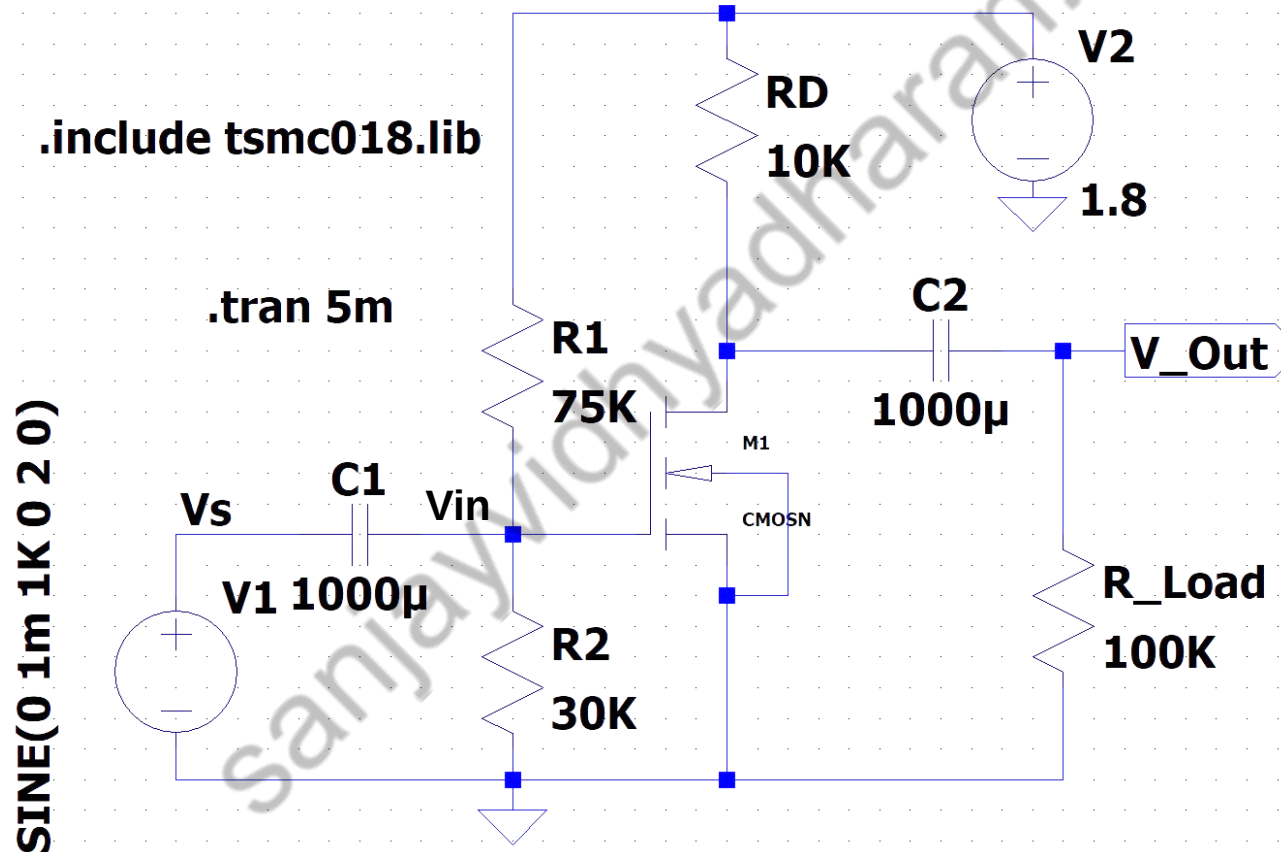


MOSFET Small Signal Equivalent

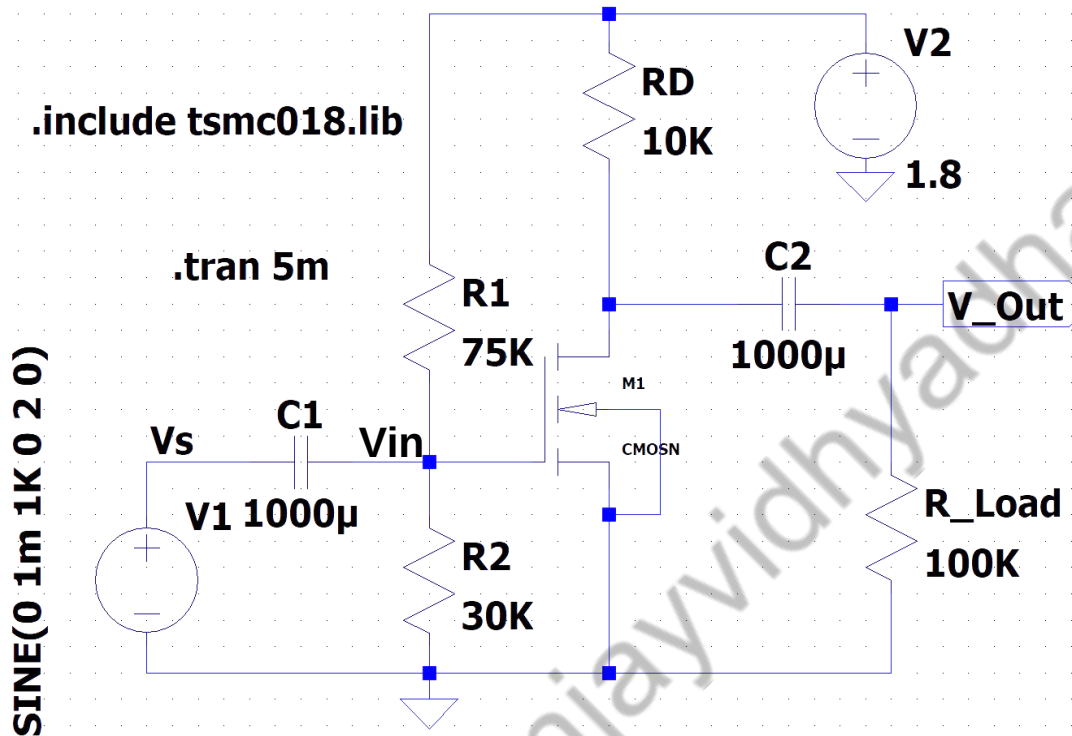
High Frequency Model



CS Amplifier



CS Amplifier



$$V_{Drain} = V_{DD} - I_D * R_D$$

$$V_{Drain} = V_{DD} - (I_{DC} + i_d) * R_D$$

$$V_{Drain} = V_{DQ} - i_d * R_D$$

$$V_{out} = -i_d * R_D$$

$$V_{out} = -g_m V_{in} * R_D$$

$$Gain = -g_m * R_D$$

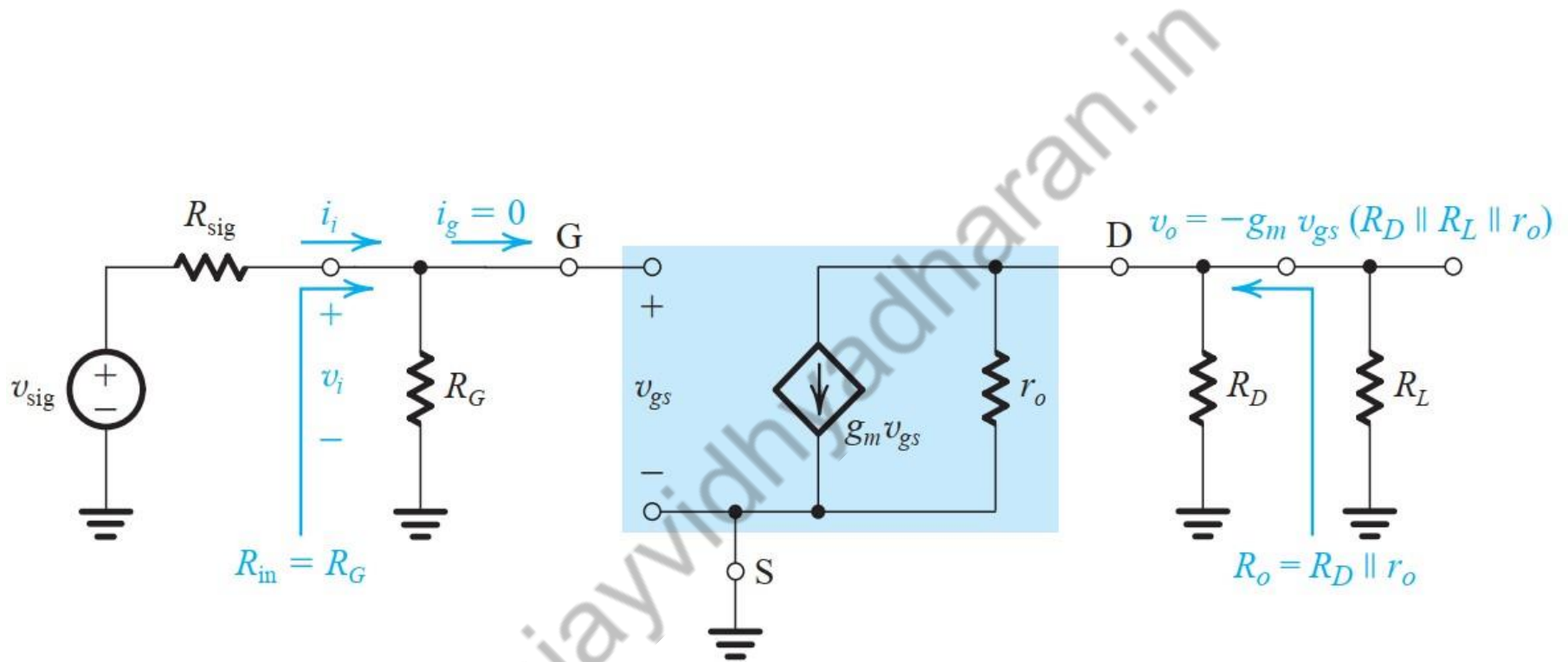
$$g_m = \sqrt{2\mu_n C_{ox} \left(\frac{W}{L}\right) I_D}$$

Example

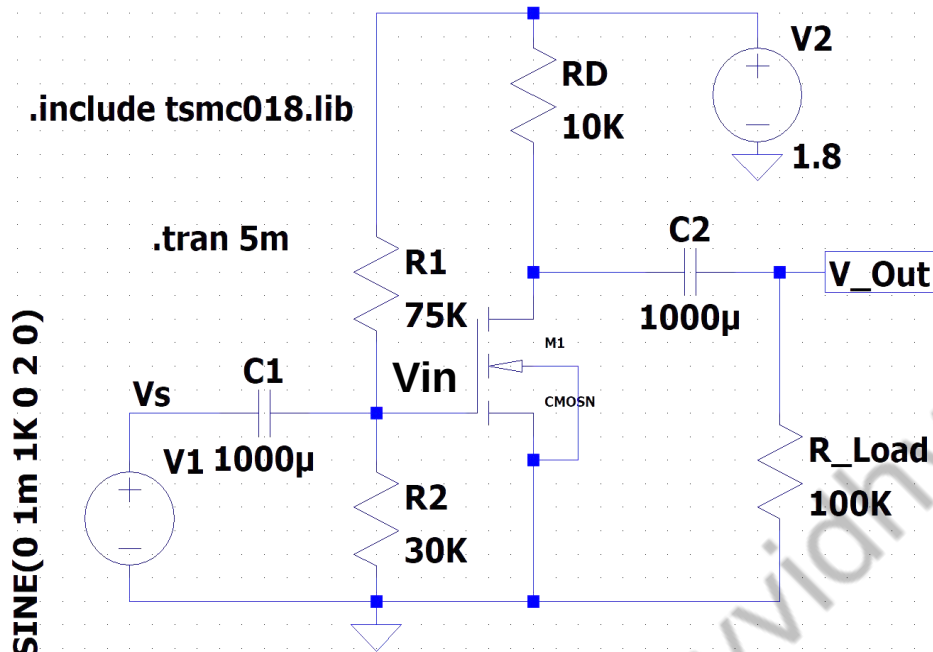
$$K_n = 200 \mu A/V^2 \quad W/L = 50 \quad I_D = 100 \mu A \quad g_m = 1.4 m \quad Gain = 14$$

$$I_D = 100 \mu A, \quad \lambda = 0.12 V^{-1} \quad r_o \text{ in few Mega Ohms}$$

CS Amplifier



CS Amplifier



Design Steps

1. Fix I_{DQ} Meeting following conditions
 - (a) $I_{DQ} * V_{DD} < \text{Max Power Constraint}$

- (b) $SR = dV_o / dt$ maximum V/µs
 $SR = I_D / C_{Load}$

2. Fix R_D for Max Symmetrical Output swing
 $R_D = (V_{DD} - V_{ov}) / 2I_{DQ}$

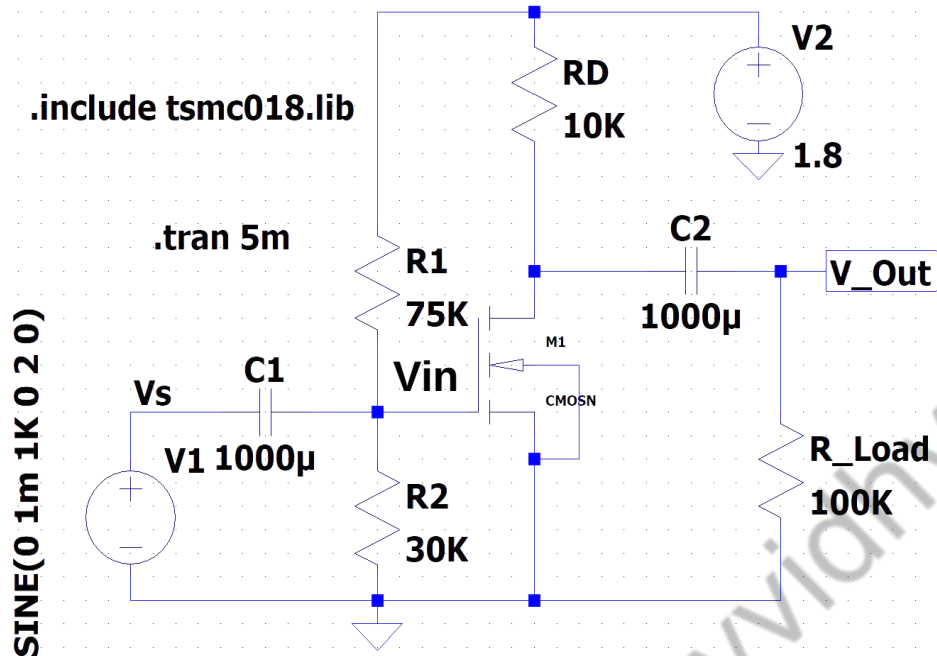
$$g_m = 2I_D / V_{ov}$$

3. Fix (W/L) for required gain

$$Gain = -g_m * R_D$$

$$g_m = \sqrt{2\mu_n C_{ox} \left(\frac{W}{L} \right) I_D}$$

CS Amplifier



Design Steps

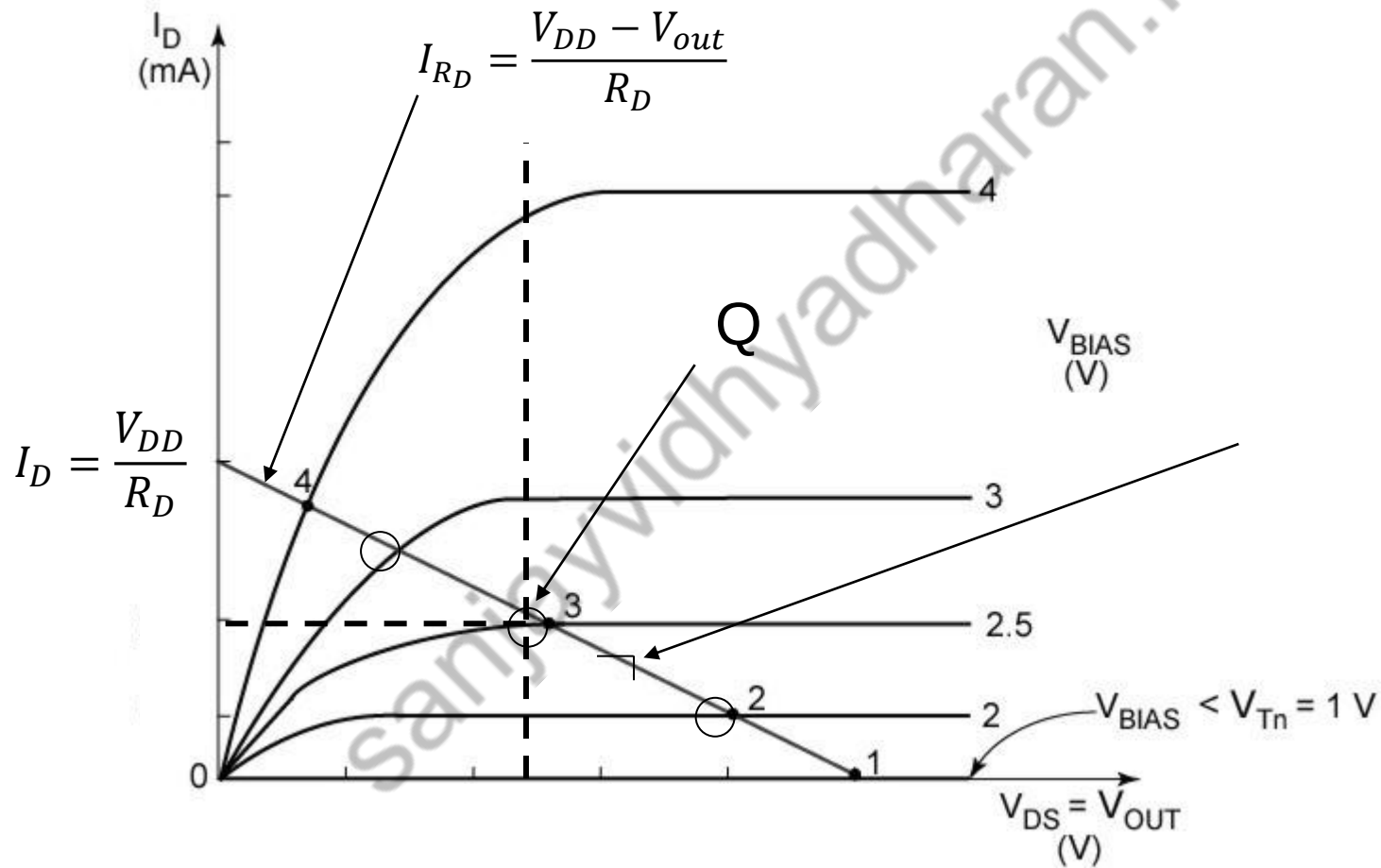
4. Design issues with R1 and R2
Set for V-overdrive (V_{GS})

5. Values of C1 and C2

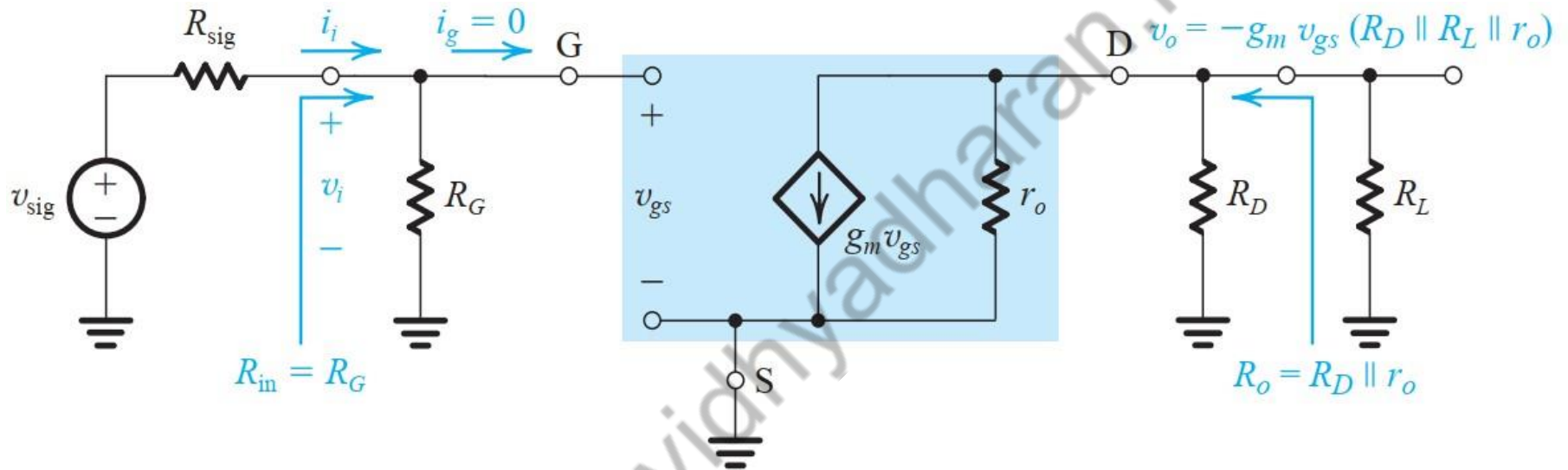
$$Gain = -g_m * R_D$$

$$g_m = \sqrt{2\mu_n C_{ox} \left(\frac{W}{L}\right) I_D}$$

Load-Line Analysis to find Q



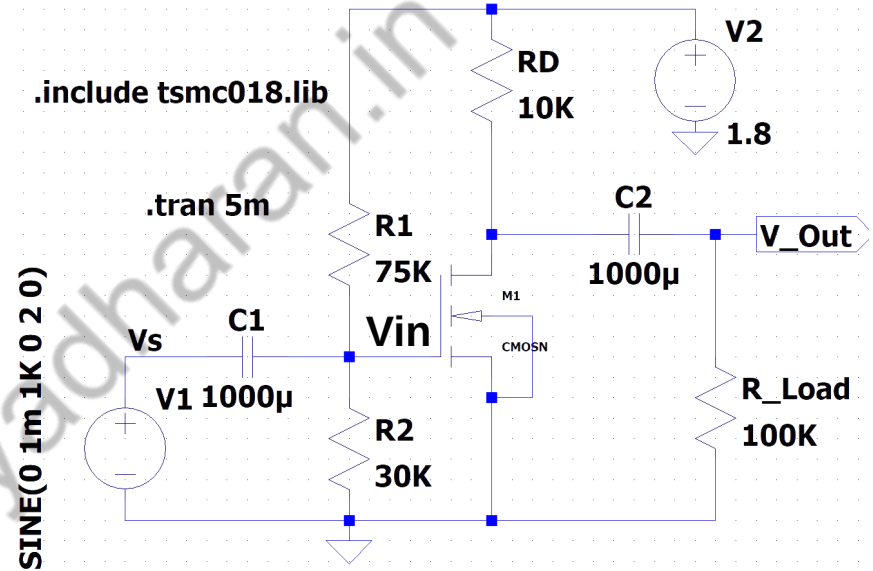
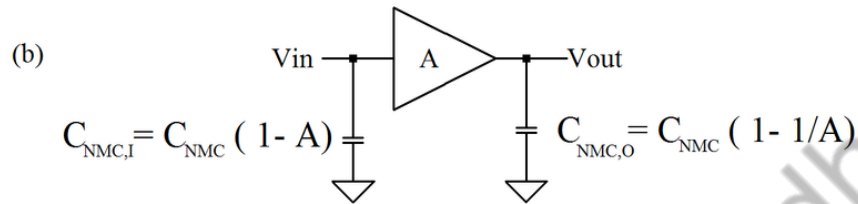
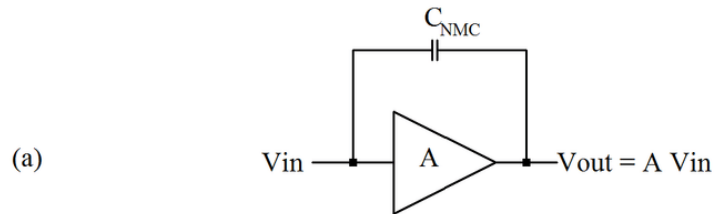
CS Amplifier



Gain is a function of Load Resistance
High Input Impedence
High Miller Capacitance

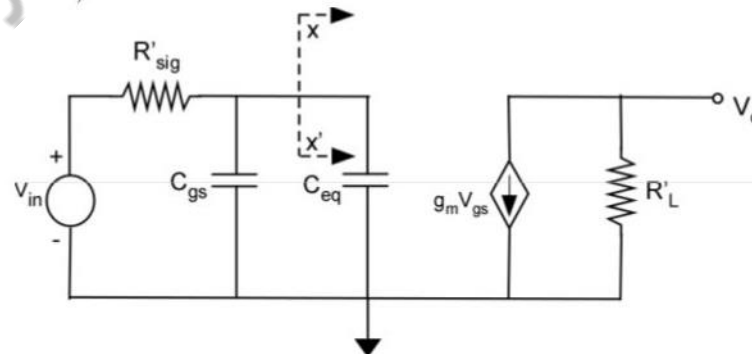
CS Amplifier

High Miller Capacitance



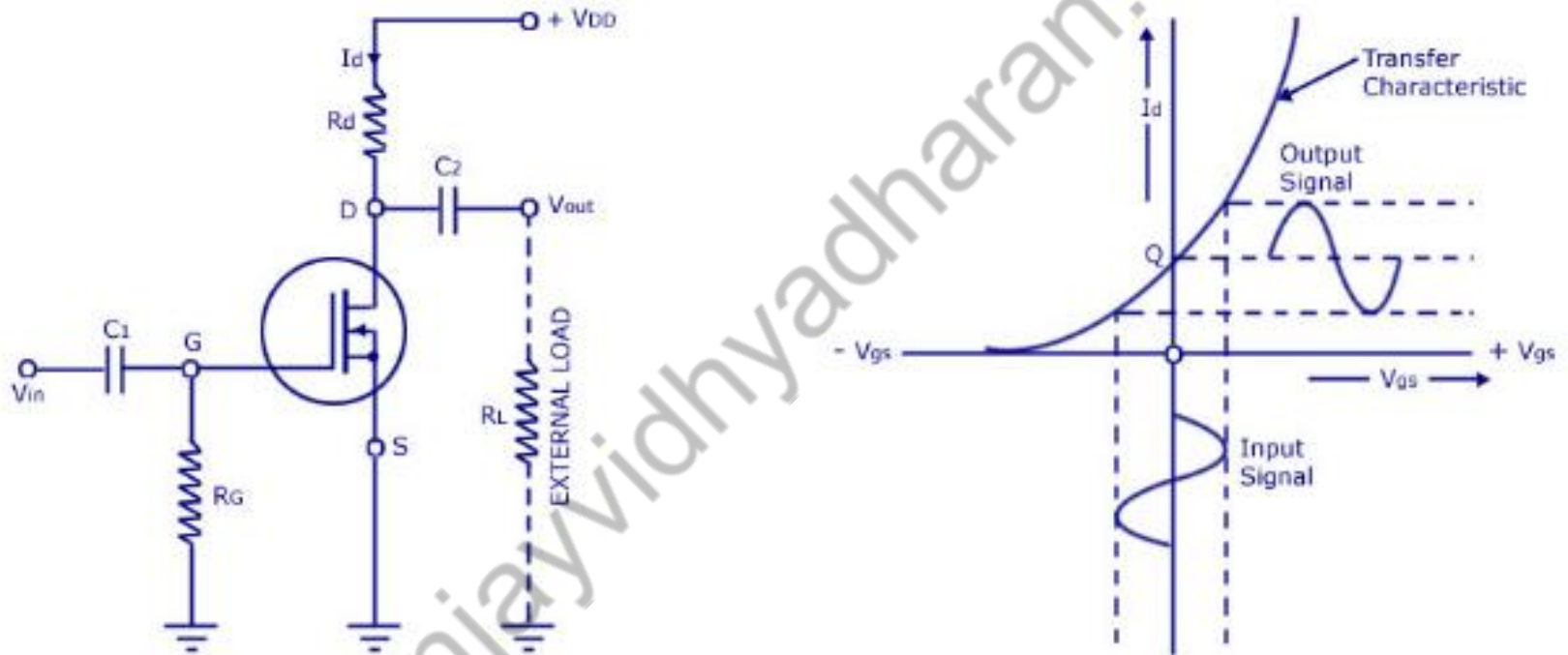
$$C_{eq} = C_{gd} (1 + g_m R'_L) = \text{Miller Capacitance}$$

$$v_{in} = \frac{R_g V_{sig}}{R_g + R_{sig}}$$



CS Amplifier

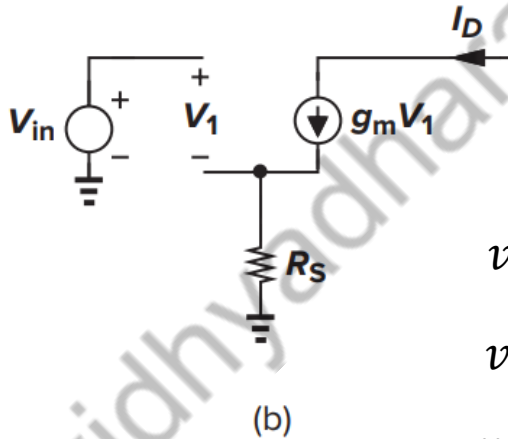
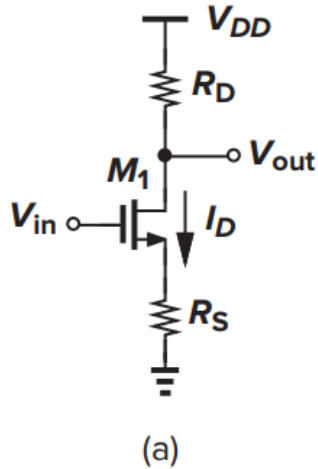
No Q-point Stability



$$i_D = (1/2) \mu_n C_{ox} (W/L) (v_{GS} - V_{Tn})^2 (1 + \lambda_n v_{DS})$$

CS Amplifier

CS stage with source degeneration.



$$V_{IN} = V_{GS} + I_D R_S$$

$$\Delta I_D = \Delta(V_{IN} - V_{GS})/R_S$$

$$v_{in} = v_{gs} + i_d R_S$$

$$v_{in} = v_{gs} + g_m v_{gs} R_S$$

$$v_{in} = v_{gs} (1 + g_m R_S)$$

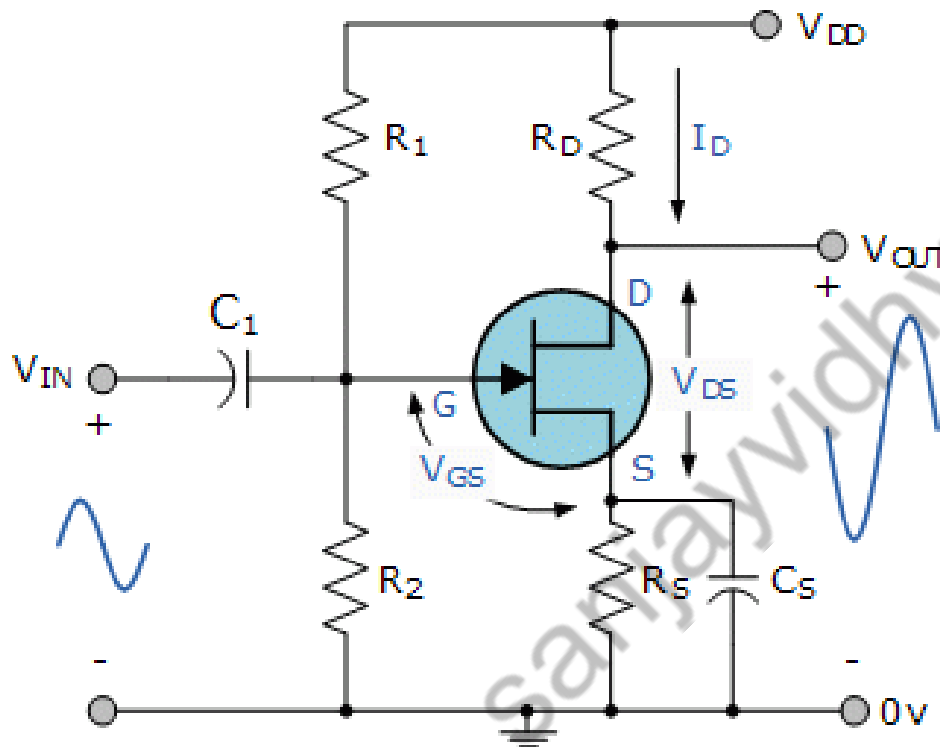
$$v_{out} = i_d R_D$$

$$v_{out} = -v_{gs} g_m R_D$$

$$Gain \sim - \frac{R_D}{R_S}$$

CS Amplifier

CS stage with source degeneration and bypass capacitor.

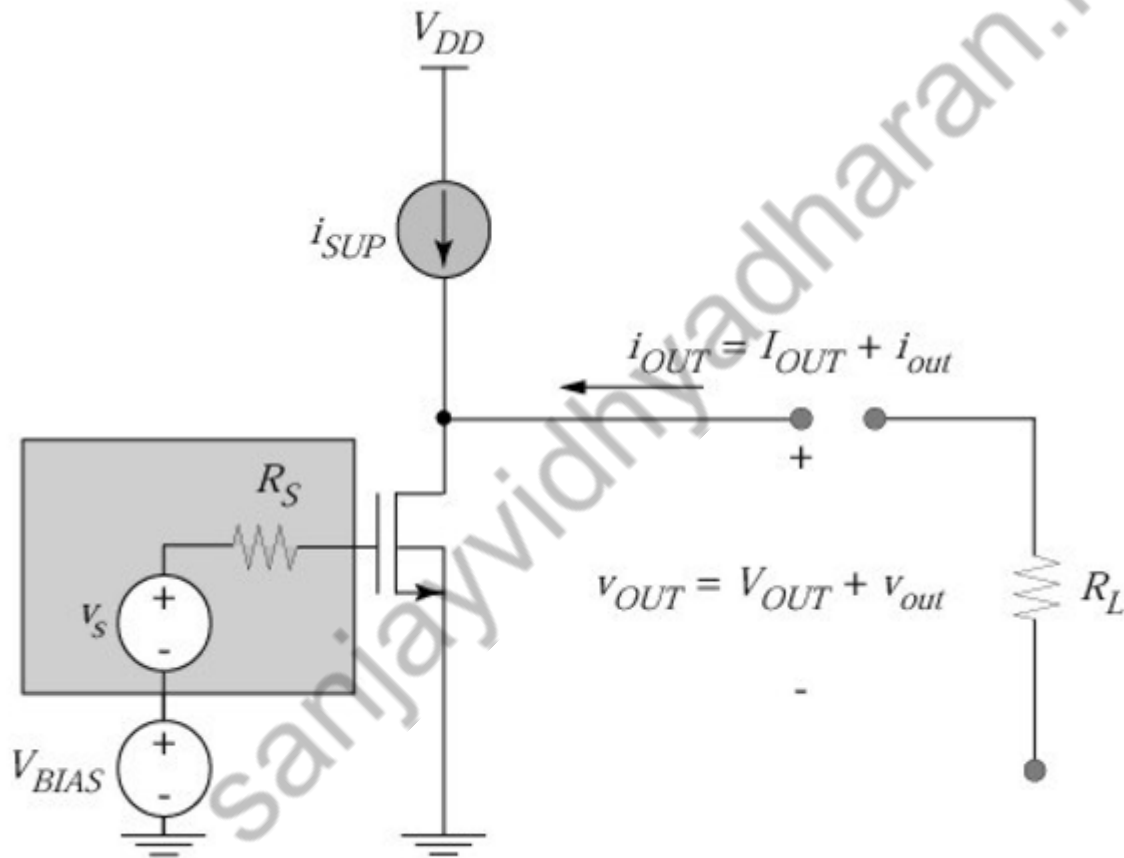


$$\text{Gain} \sim -g_m R_D$$

Design Steps

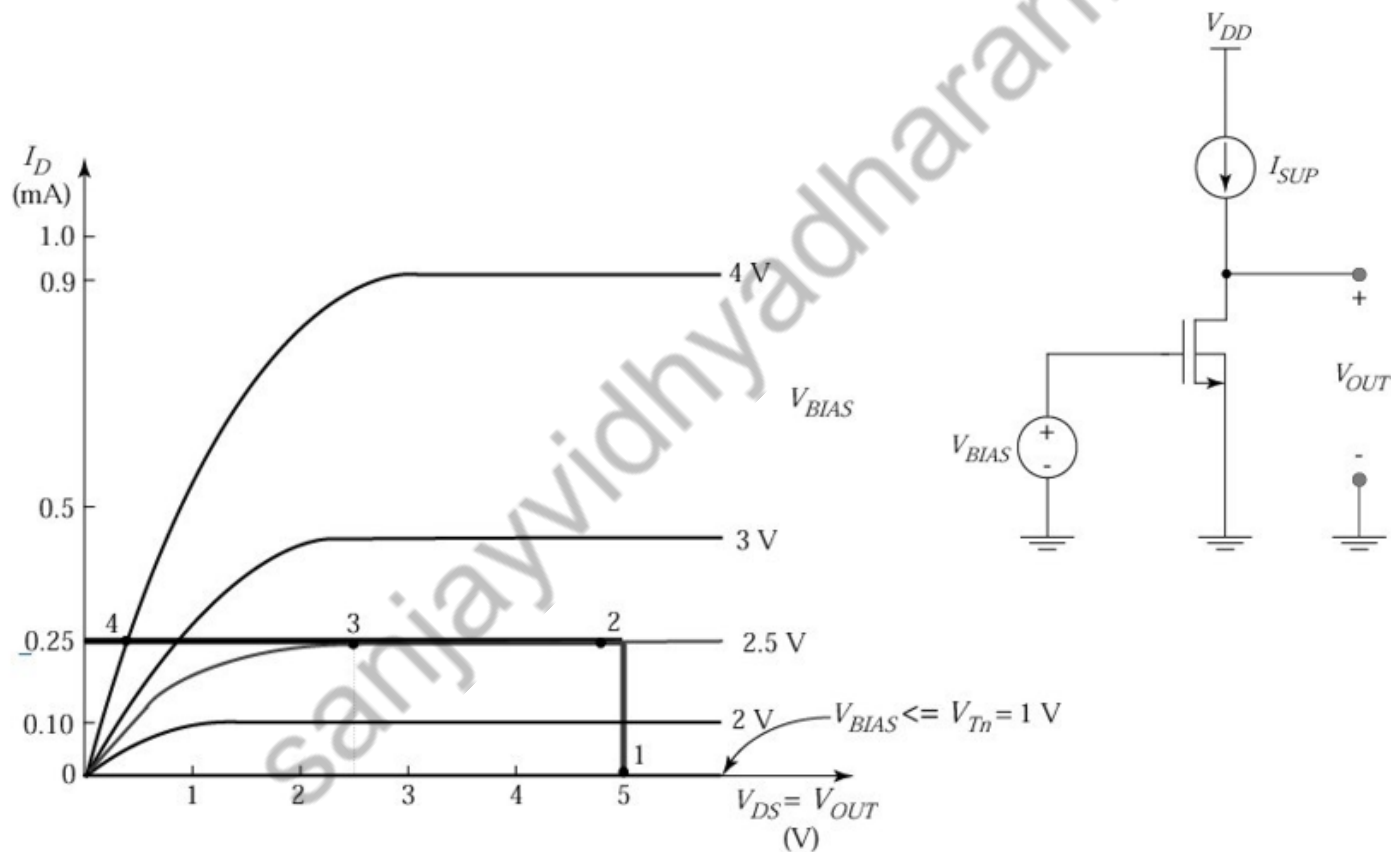
1. Fix I_{DQ} Meeting following conditions
 - (a) $I_{DQ} * V_{DD} < \text{Max Power Constraint}$
 - (b) $SR = dV_o / dt$ maximum $V/\mu s$
 $SR = I_{DQ} / C_{Load}$
2. Fix R_D for Max Symmetrical Output swing
 $R_D = (0.9 V_{DD} - V_{ov}) / 2I_{DQ}$
3. $R_S = 0.1 V_{DD} / I_{DQ}$

CS Amp with Current Source Supply

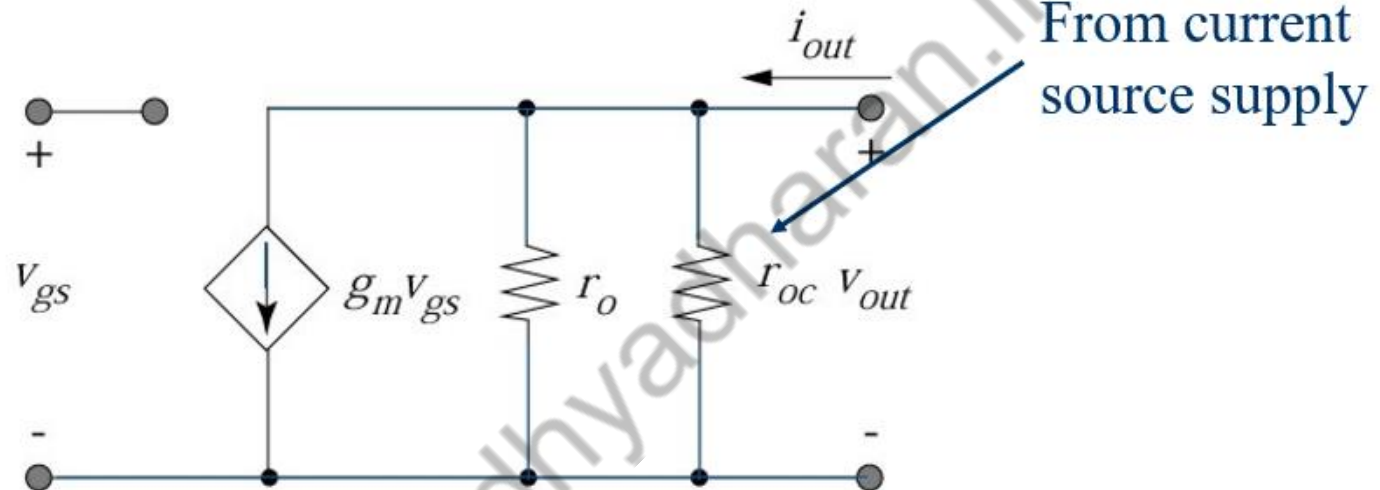


Gain = ?

CS Amp with Current Source Supply



CS Amp with Current Source Supply

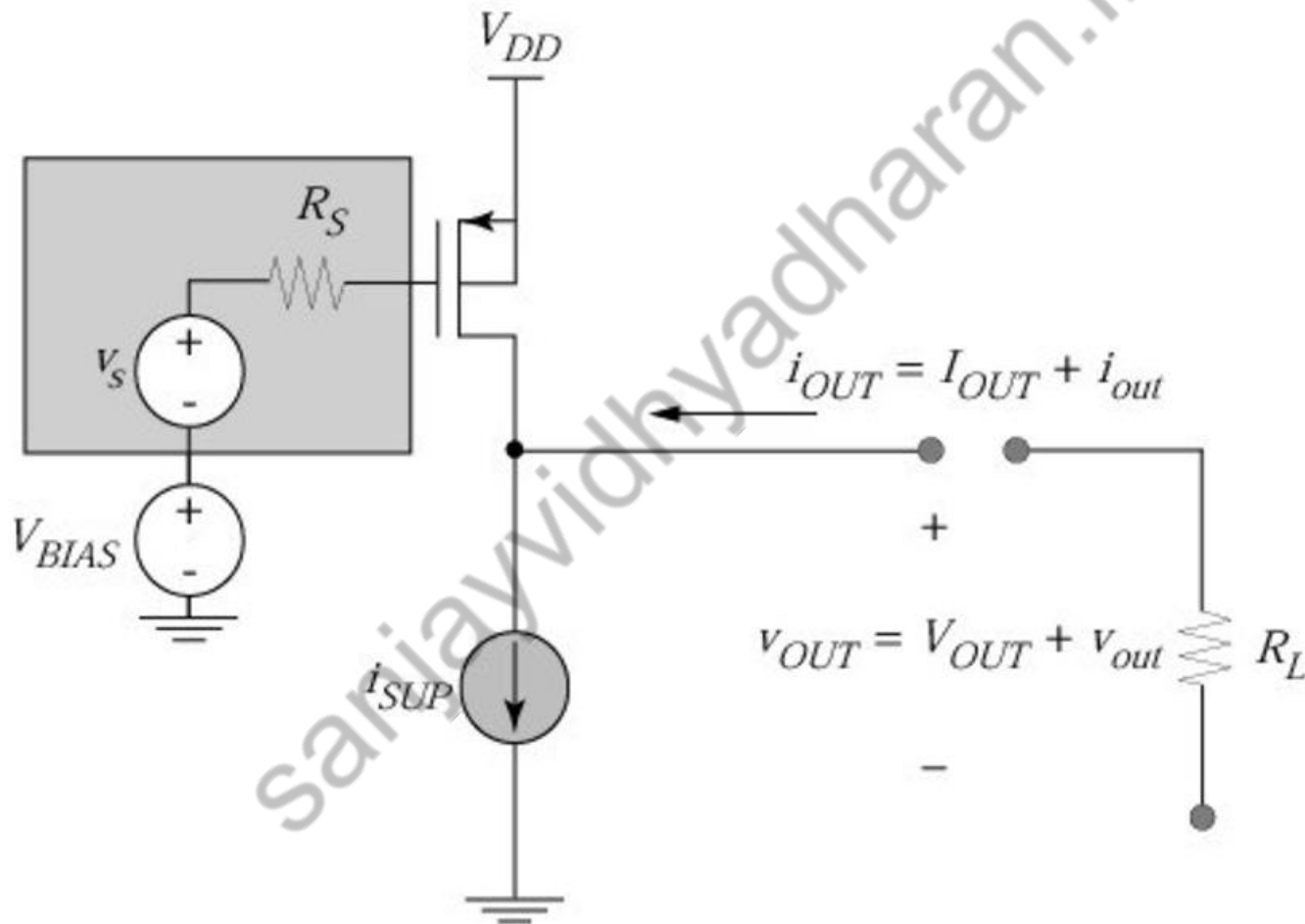


$$R_{in} = \infty$$

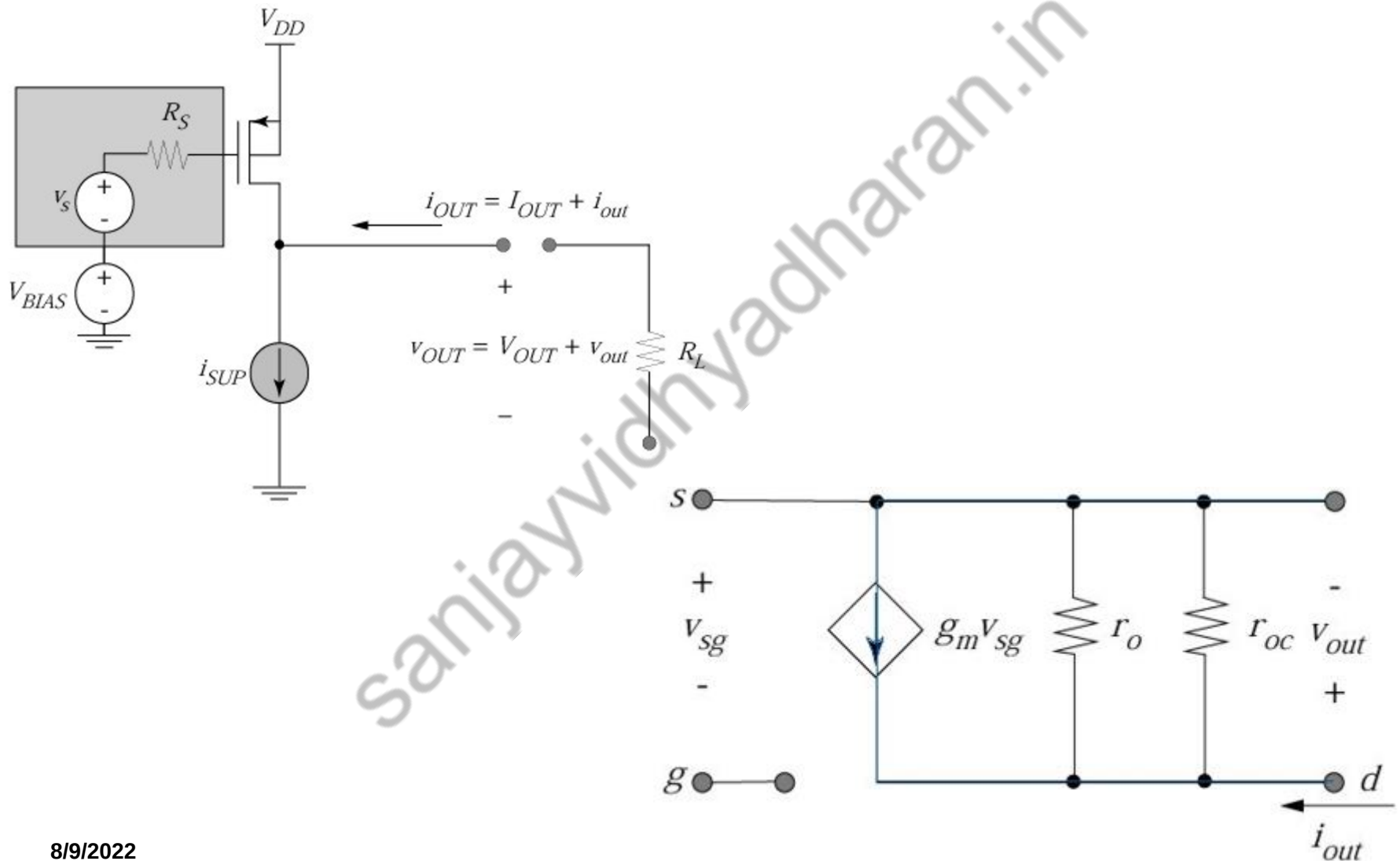
$$G_m = g_m$$

$$R_{out} = r_o \parallel r_{oc}$$

P-Channel CS Amplifier

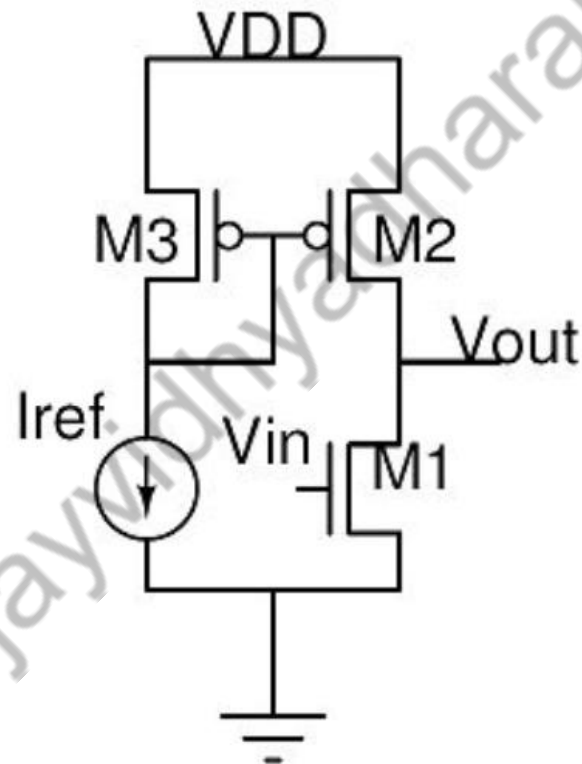


P-Channel CS Amplifier

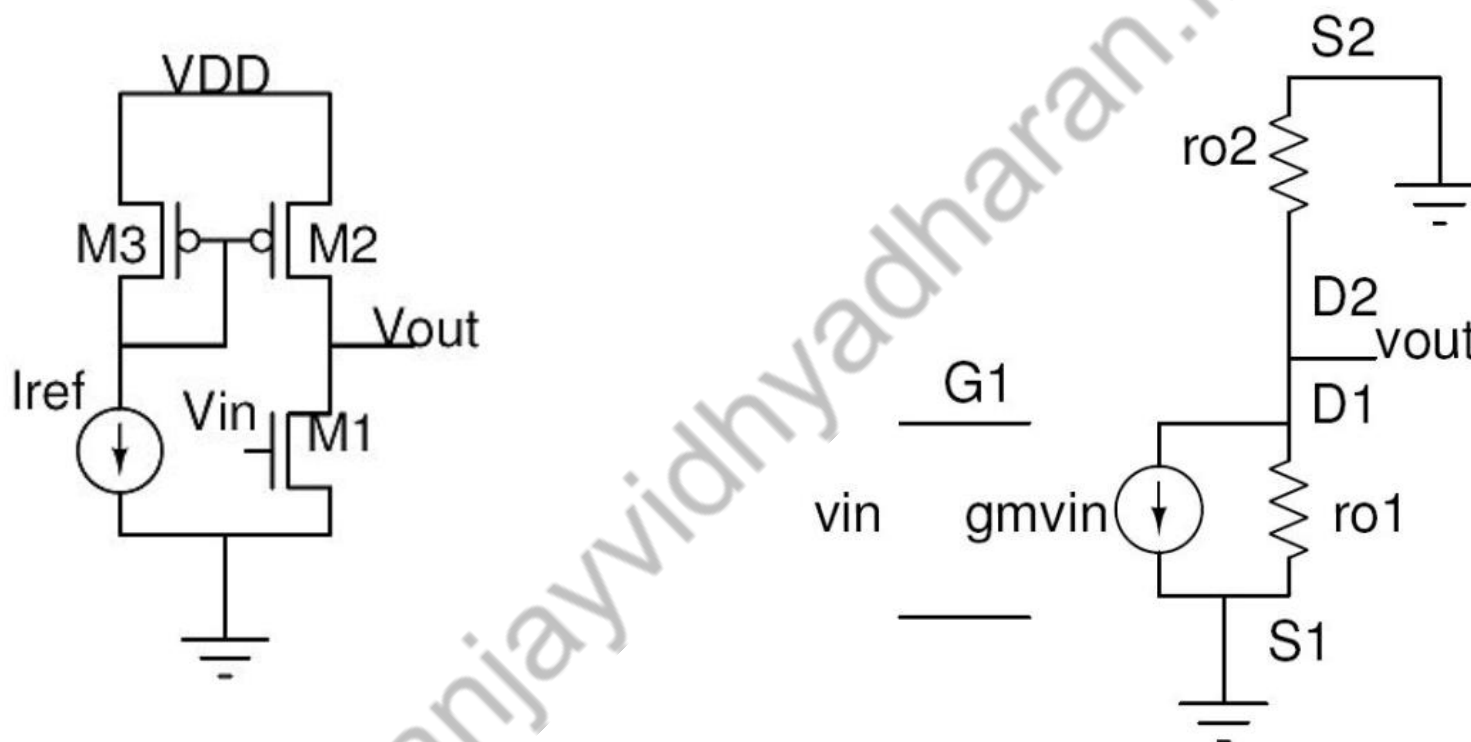


8/9/2022

CS Amplifier with Active Load



CS Amplifier with Active Load



$$v_{out} = g_{m1} v_{in} * (r_{o1} || r_{o2})$$

Thank you