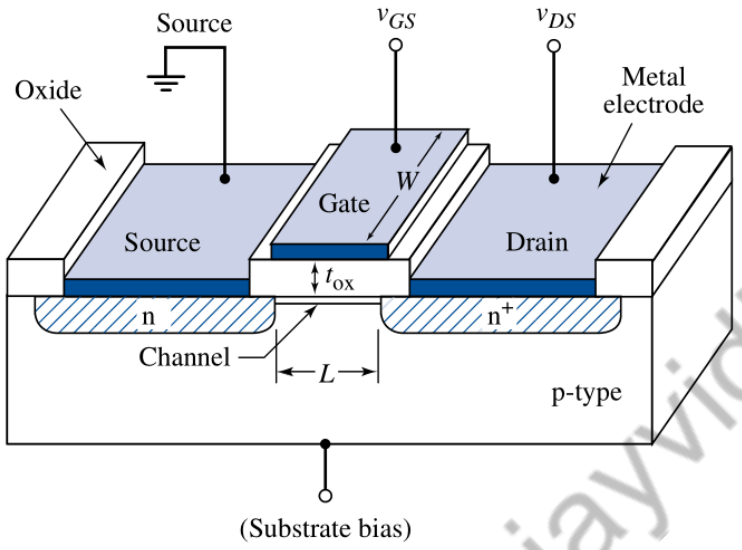
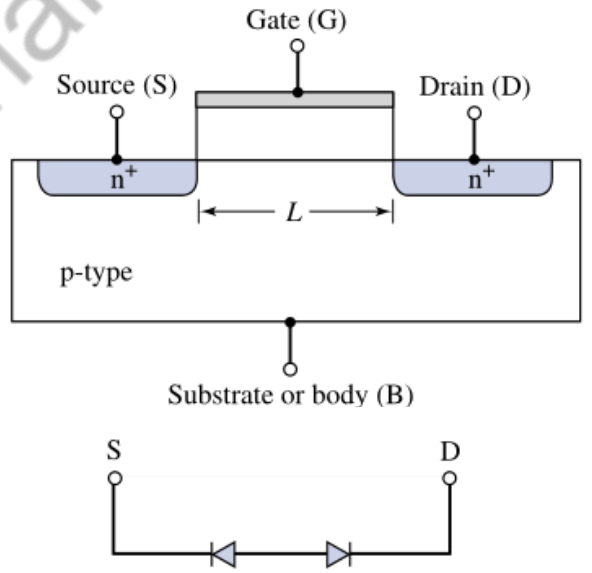
Advanced VLSI Design : 2021-22
Lecture 14-A
Deep-Submicron MOSFET operation

By Dr. Sanjay Vidhyadharan

MOSFET Operation

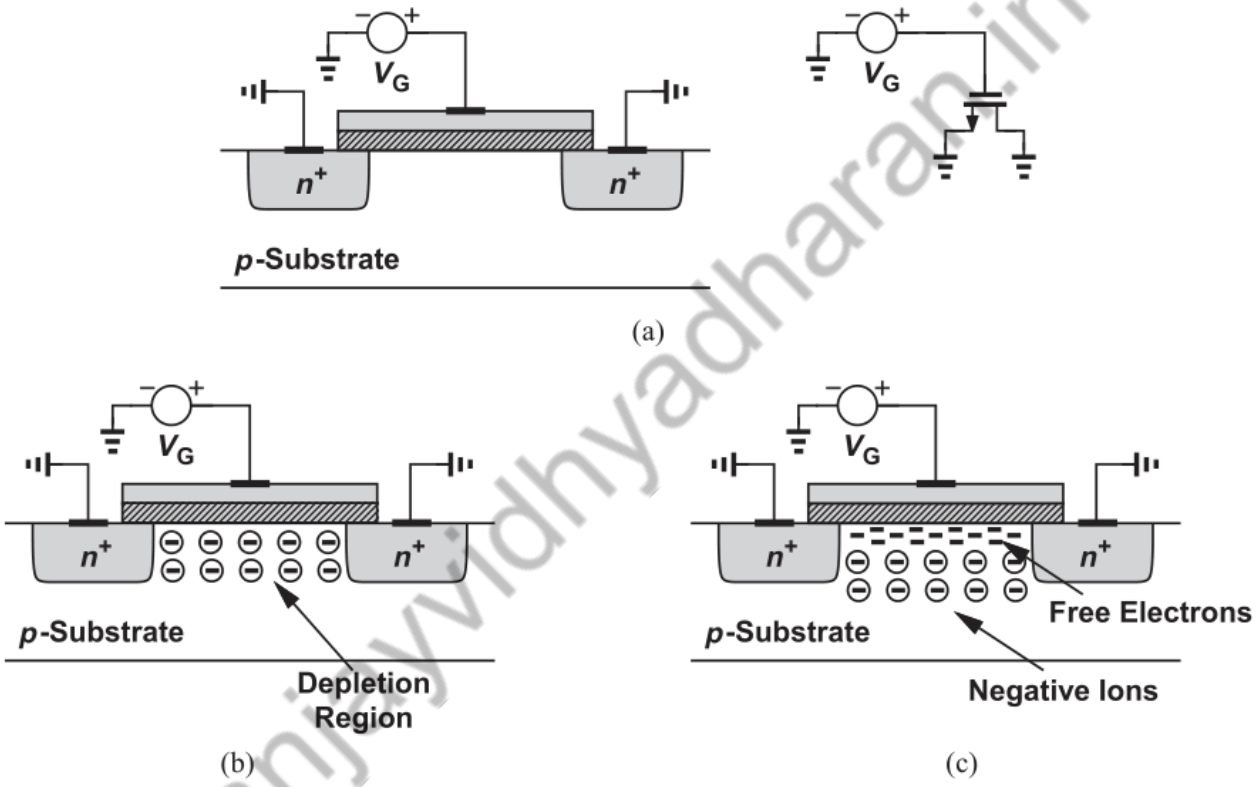
Cut-off Region





$For\ V_{GS} < V_T \qquad I_D = 0$

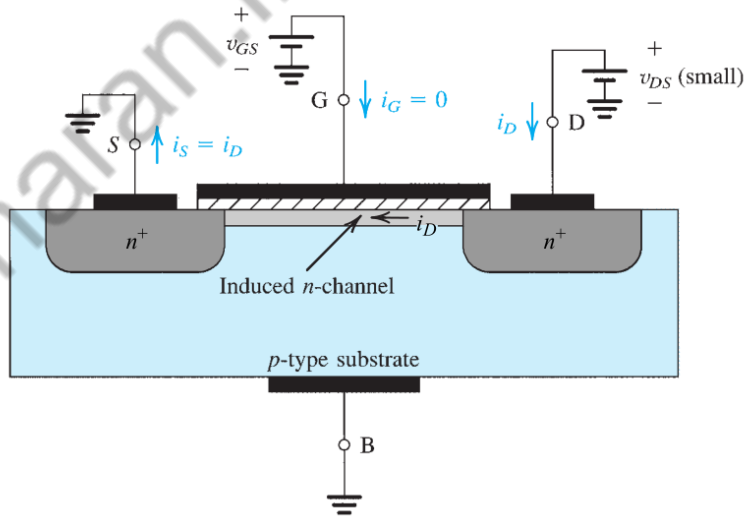
The Threshold Voltage



As a practical definition, The threshold Voltage V_T is that gate voltage when the surface is said to be inverted, i.e. the density of mobile electrons on the surface becomes equal to the density of holes in the bulk (p-type) substrate.

The Threshold Voltage

$$V_{T0} = \Phi_{GC} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}$$



1. The work function difference TGC between the gate and the channel reflects the built-in potential of the MOS system, which consists of the p-type substrate, the thin silicon dioxide layer, and the gate electrode. Depending on the gate material, the work function difference is

$$\emptyset_{GC} = \emptyset_{F\_Substrate} - \emptyset_{F_{metal}} \quad For\ Metal\ Gate$$

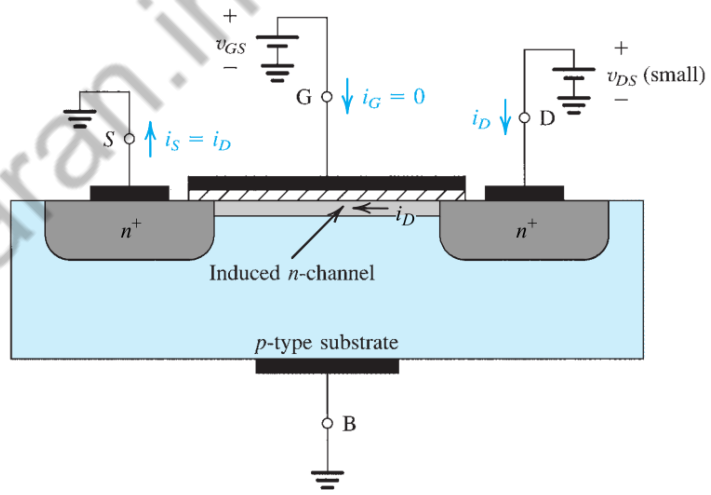
$$\emptyset_{GC} = \emptyset_{F\_Substrate} - \emptyset_{F_{Polysilicon}} \quad ForPolysilicon\ Gate$$

2. The externally applied gate voltage must be changed to achieve surface inversion, i.e., to change the surface potential by - 2 $\emptyset_F$. This will be the second component of the threshold voltage.

$$\phi_{Fp} = \frac{kT}{q} \ln \frac{n_i}{N_A}$$

The Threshold Voltage

$$V_{T0} = \Phi_{GC} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}$$

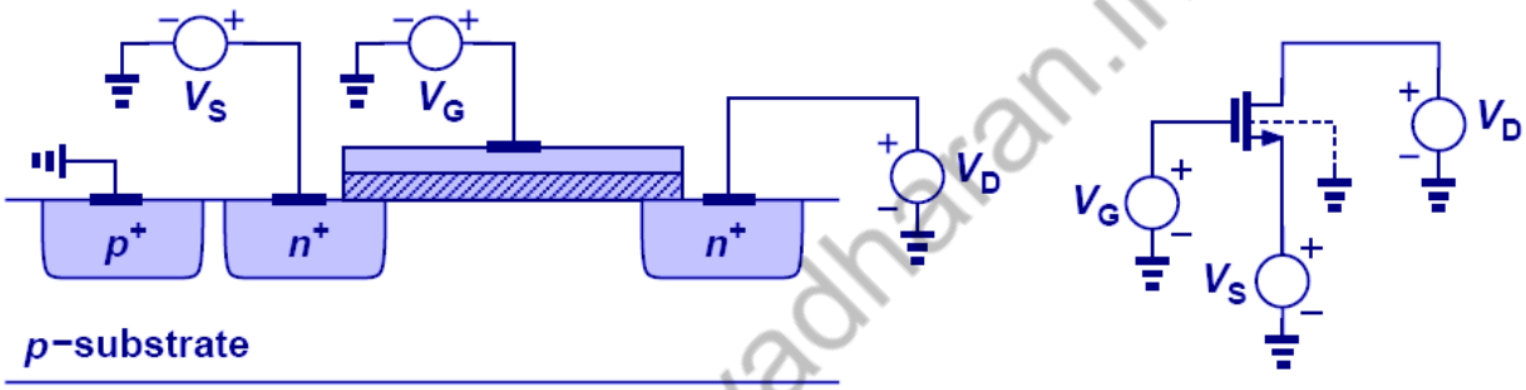


3. Another component of the applied gate voltage is necessary to offset the depletion region charge, which is due to the fixed acceptor ions located in the depletion region near the surface.

$$Q_{B0} = -\sqrt{2q \cdot N_A \cdot \varepsilon_{Si} \cdot |-2\phi_F|}$$

4. There always exists a fixed positive charge density Q_{ox} at the interface between the gate oxide and the silicon substrate, due to impurities and/or lattice imperfections at the interface. The gate voltage component that is necessary to offset this positive charge at the interface is - Q_{OX}/C_{ox}.

The Threshold Voltage

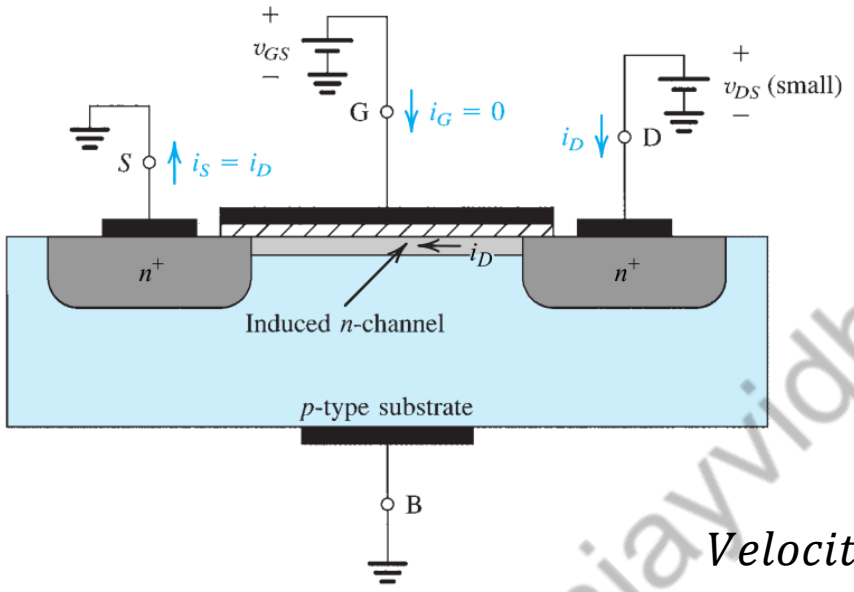


$$V_{TH} = V_{TH\,0} + \gamma\left(\sqrt{|2\phi_F| + V_{SB}} - \sqrt{|2\phi_F|}\right)$$

The **body effect** occurs in a MOSFET when the source is not tied to the substrate (which is always connected to the most negative power supply in the integrated circuit for n-channel devices and to the most positive for p-channel devices). The substrate then acts as a "second gate" or a back-gate for the MOSFET

MOSFET Current

Linear Region- Small V_{DS}



$$V_{ov} = V_{GS} - V_T$$

$$C_{ox}WL = \frac{Q}{V_{ov}}$$

$$Charge\ per\ unit\ Length = \frac{Q}{L} = C_{ox}WV_{ov}$$

$$Electric\ Field\ in\ Channel = \frac{V_{DS}}{L}$$

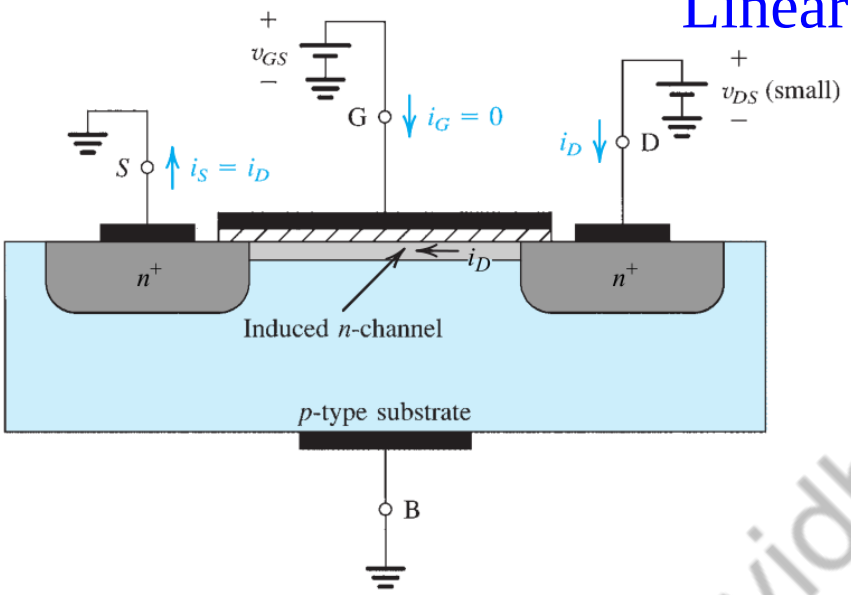
$$Velocity\ of\ Charge\ in\ Channel(v) = \mu_n E = \frac{V_{DS}\mu_n}{L}$$

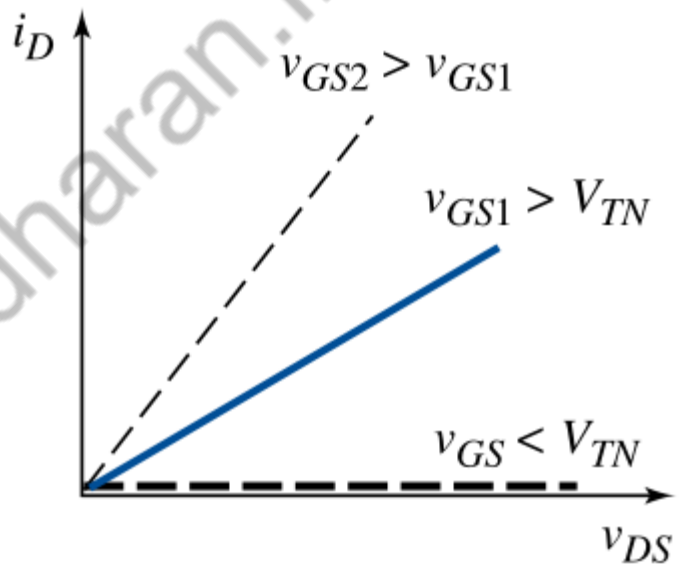
$$Current\ in\ Channel\ \ (I_D) = v * \frac{Q}{L} = \frac{V_{DS}\mu_n}{L} * C_{ox}WV_{ov}$$

$$I_D = \frac{\mu_n C_{ox} W (V_{GS} - V_T) V_{DS}}{L}$$

MOSFET Current

Linear Region- Small V_{DS}





V_{ov}

$$I_D = \frac{\mu_n C_{ox} W (V_{GS} - V_T) V_{DS}}{L}$$

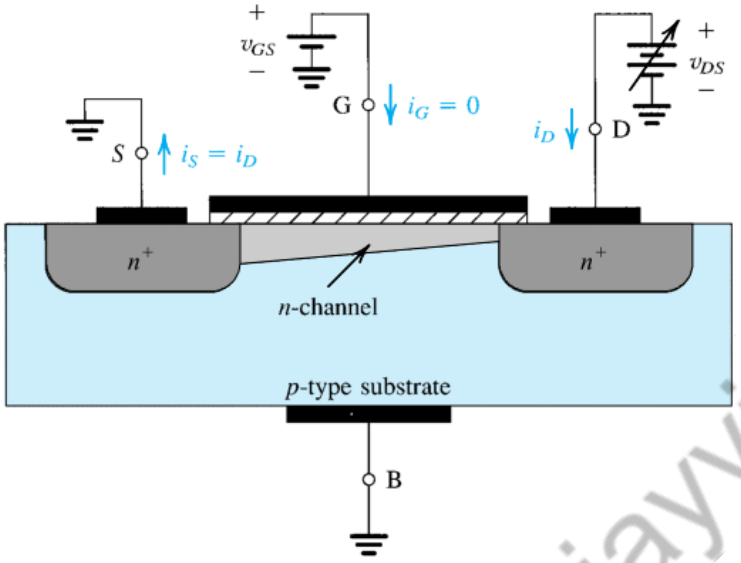
$$Transconductance\ of\ Channel\ g_{DS} = \frac{\mu_n C_{ox} W V_{ov}}{L}$$

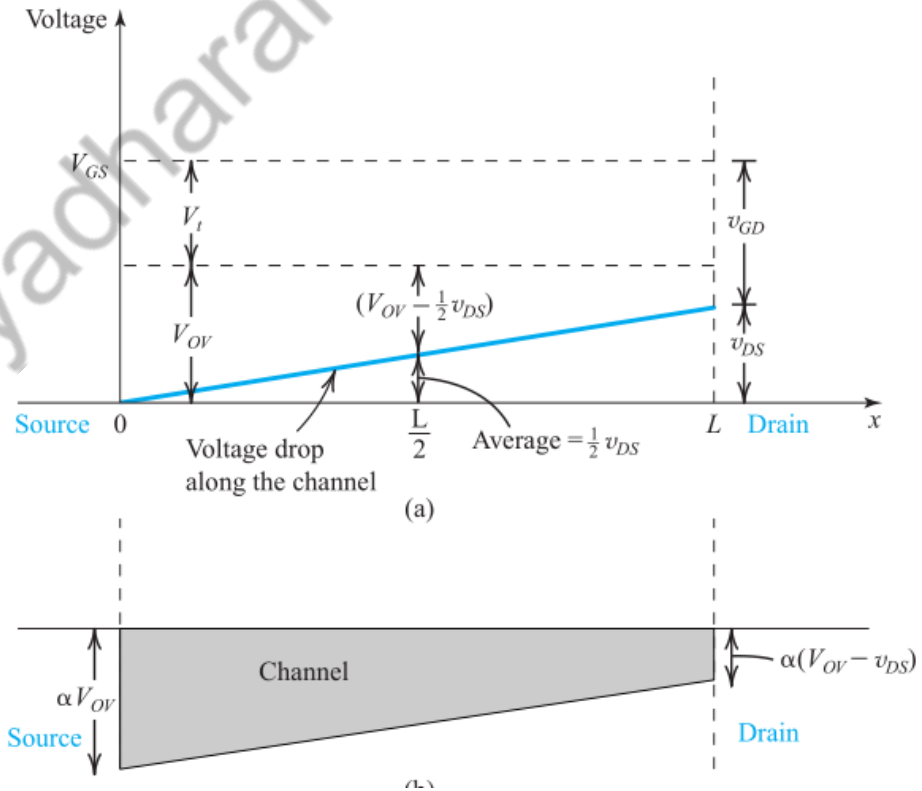
$$Process\ transconductance\ parameter\ k_n' = \mu_n C_{ox}$$

$$I_D = \frac{k_n' W V_{ov} V_{DS}}{L}$$

MOSFET Current

Linear Region as V_{DS} is Increased



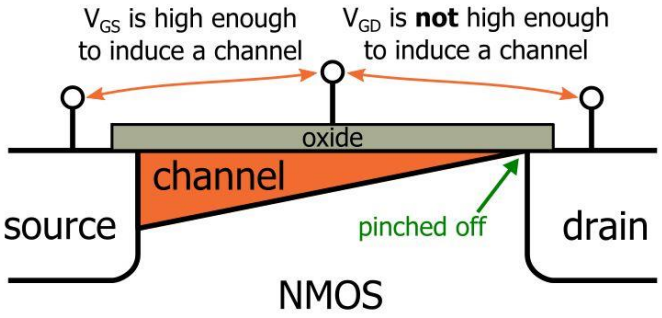


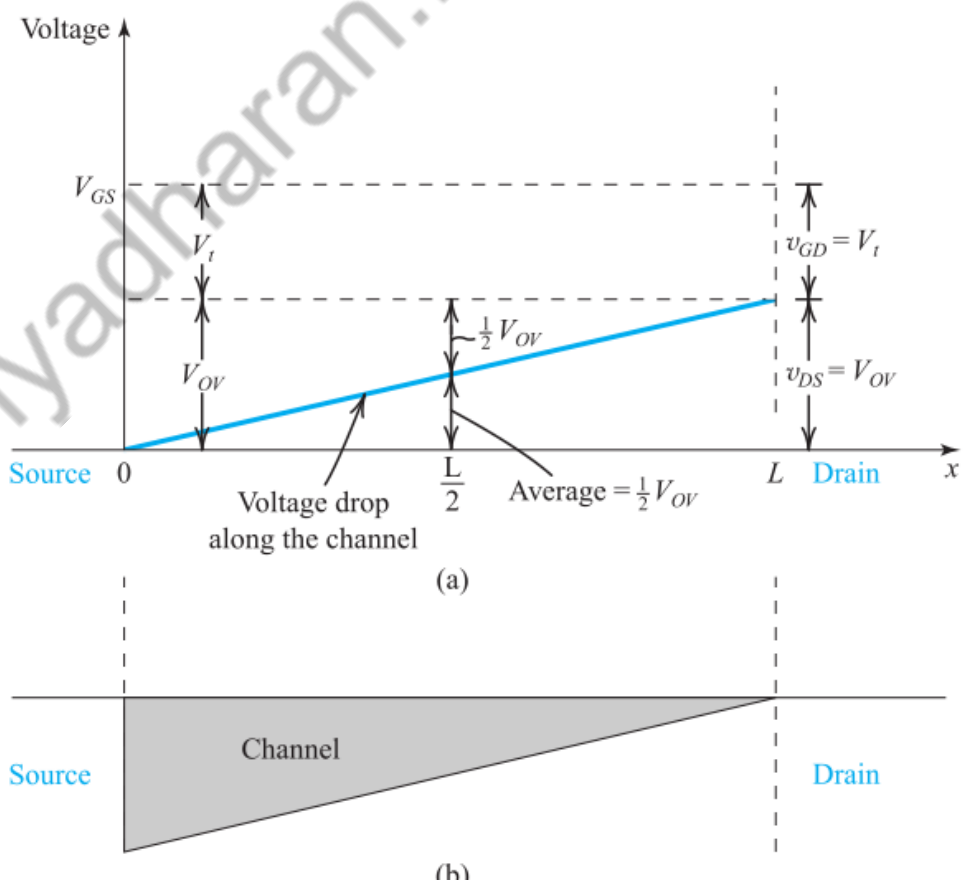
Charge in the tapered channel is proportional to the channel cross-sectional area

$$I_D = \frac{k_n' W (V_{ov} - \frac{V_{DS}}{2}) V_{DS}}{L}$$

MOSFET Current

Saturation Region



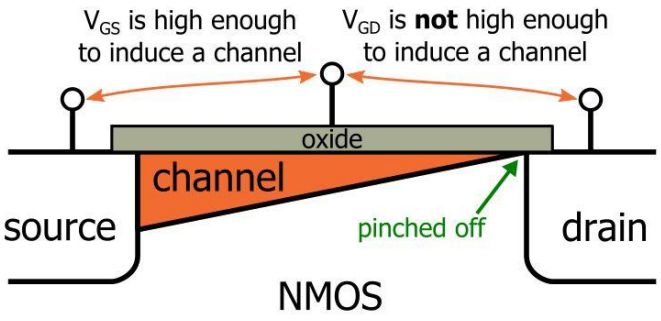


$$V_{DS} = V_{ov} = V_{GS} - V_T$$

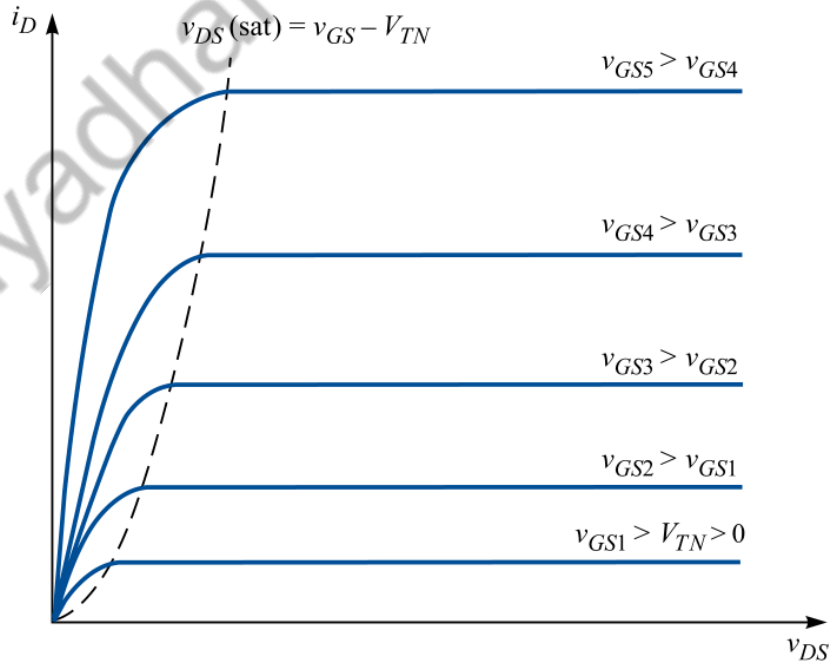
$$I_D = \frac{k_n' W (V_{ov} - \frac{V_{DS}}{2}) V_{DS}}{L}$$

$$I_D = \frac{k_n' W (V_{GS} - V_T)^2}{2L}$$

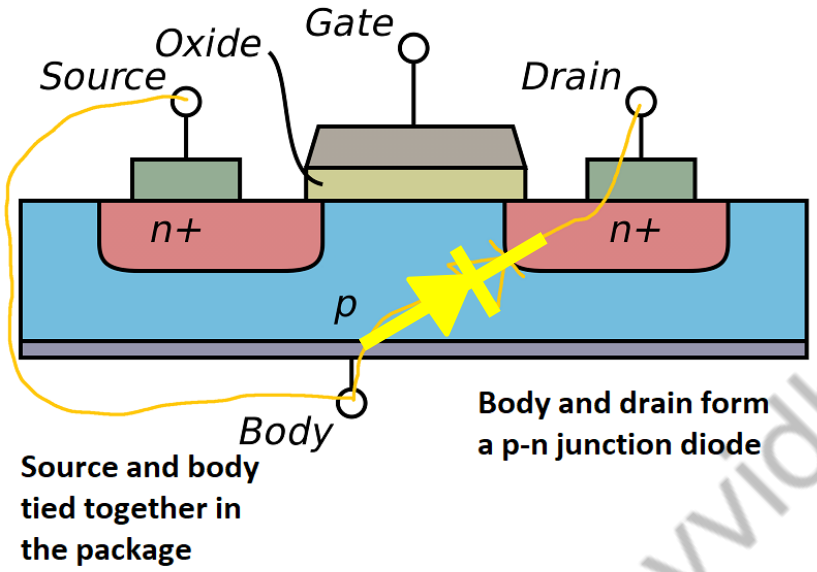
MOSFET Current

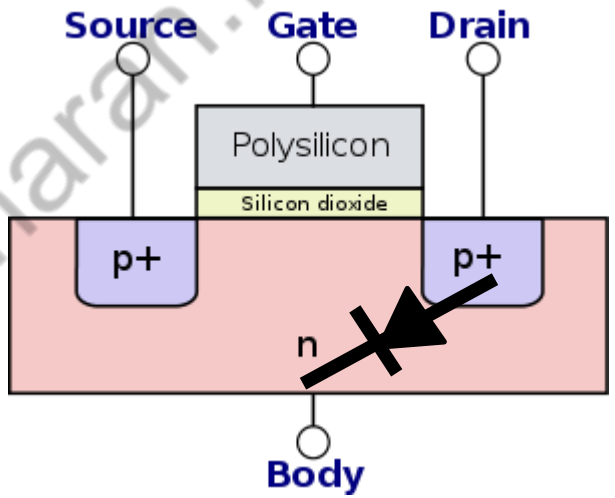


$$I_D = \frac{k_n' W (V_{GS} - V_T)^2}{2L}$$



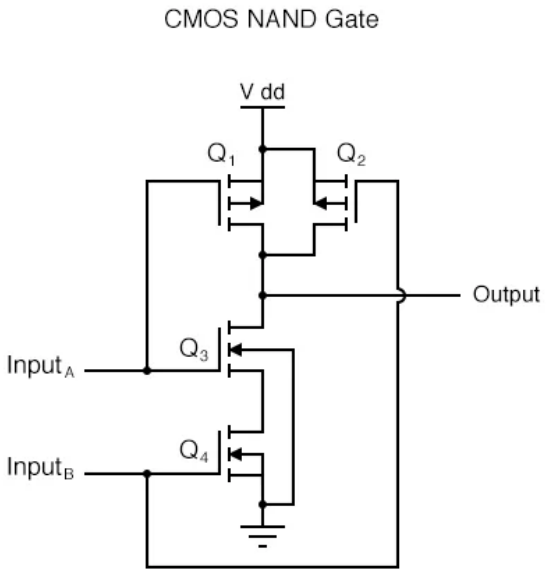
MOSFET BODY CONNECTION

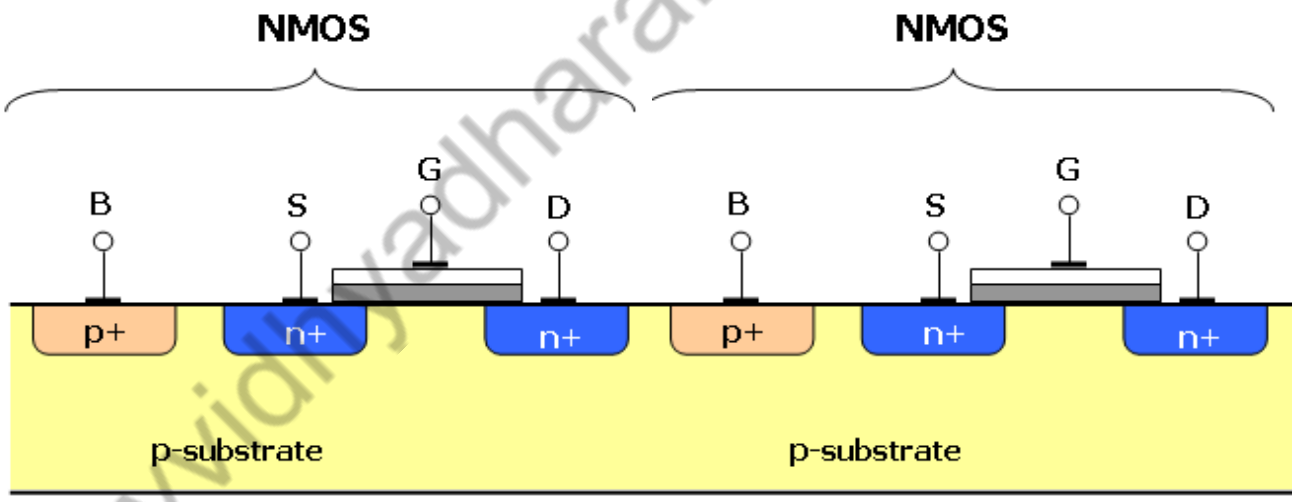




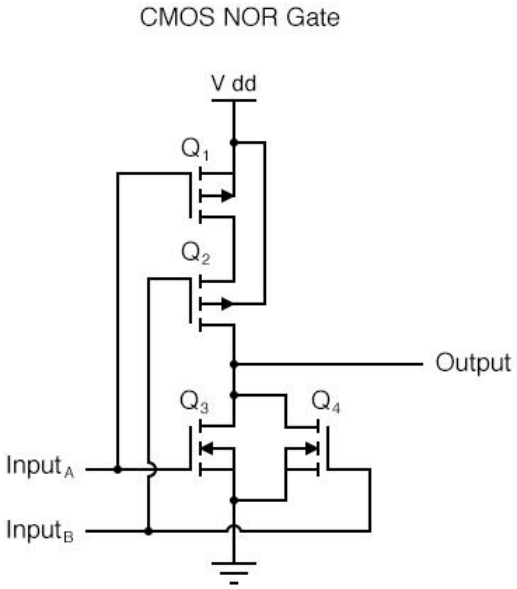
- NMOS Body to Lowest Possible Potential (Gnd)
- PMOS Body to Highest Possible Potential (V_{DD})

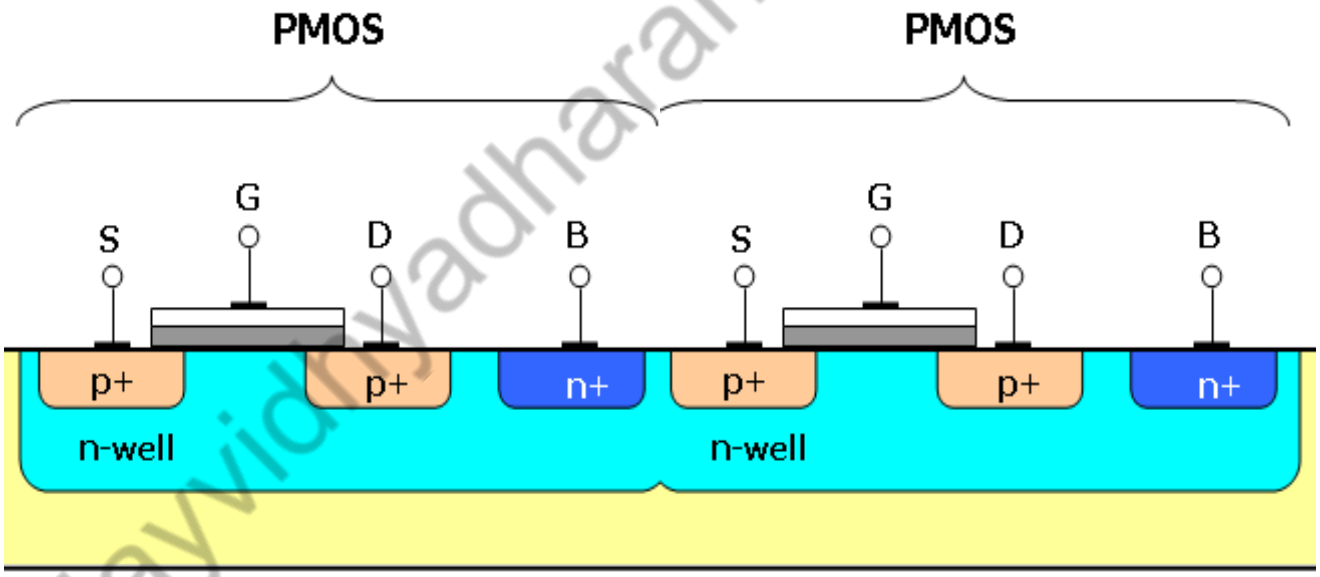
MOSFET BODY CONNECTION



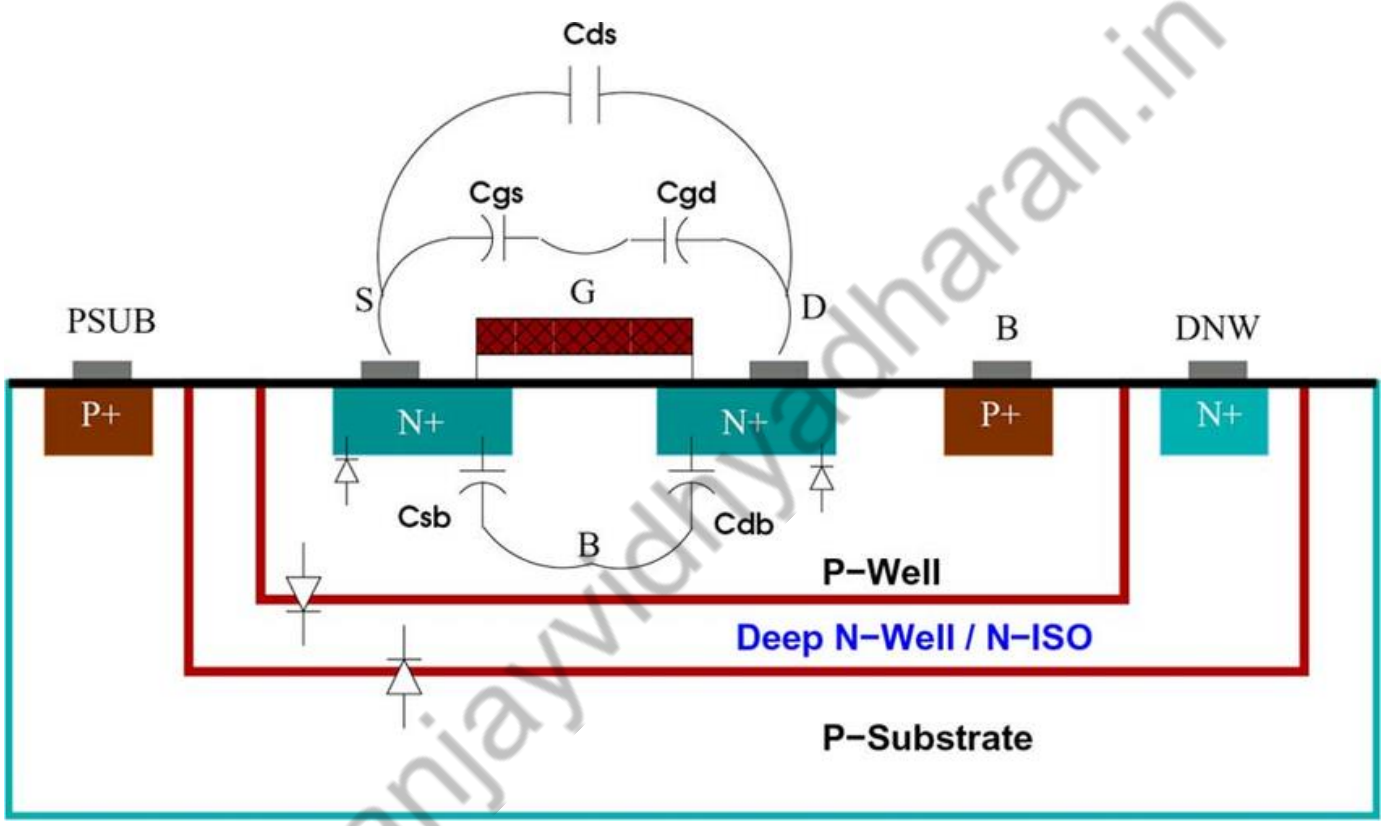


MOSFET BODY CONNECTION



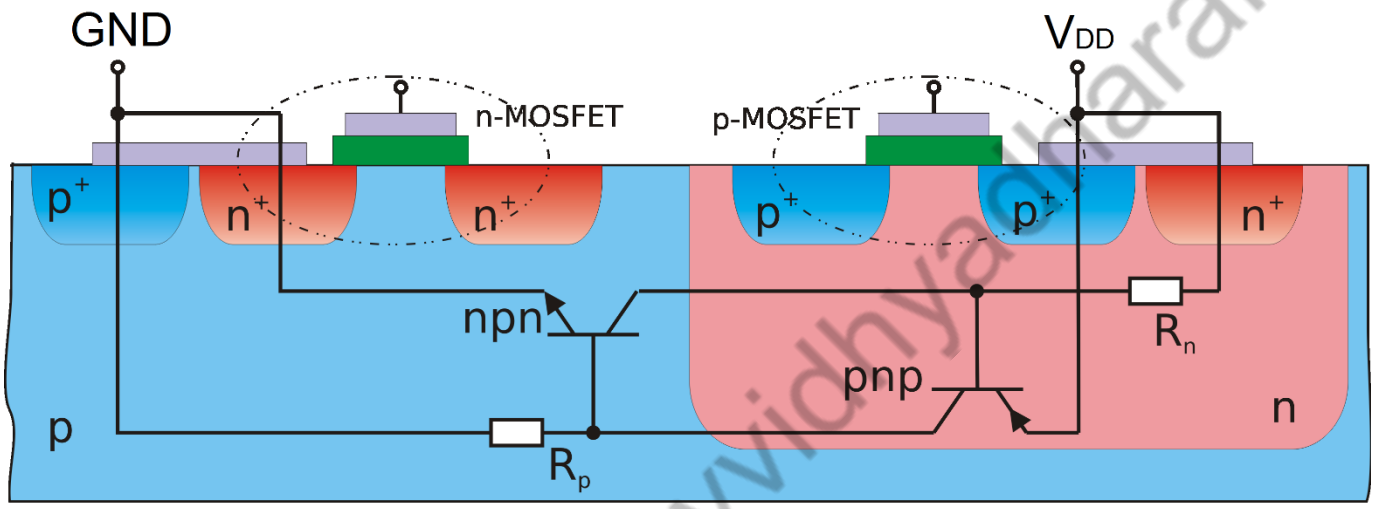


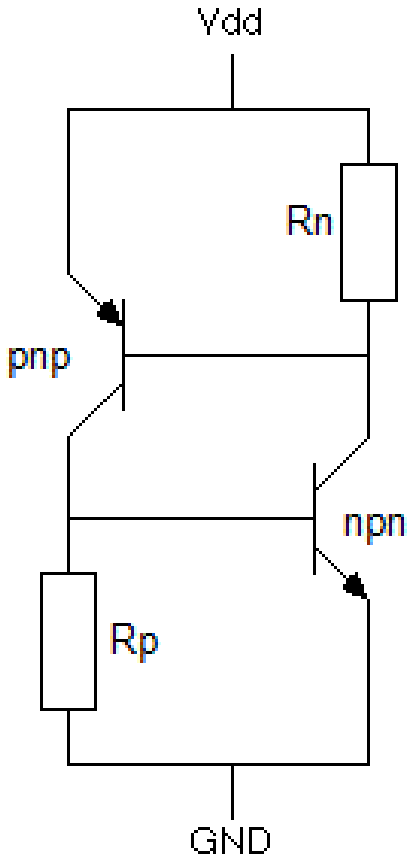
MOSFET BODY CONNECTION



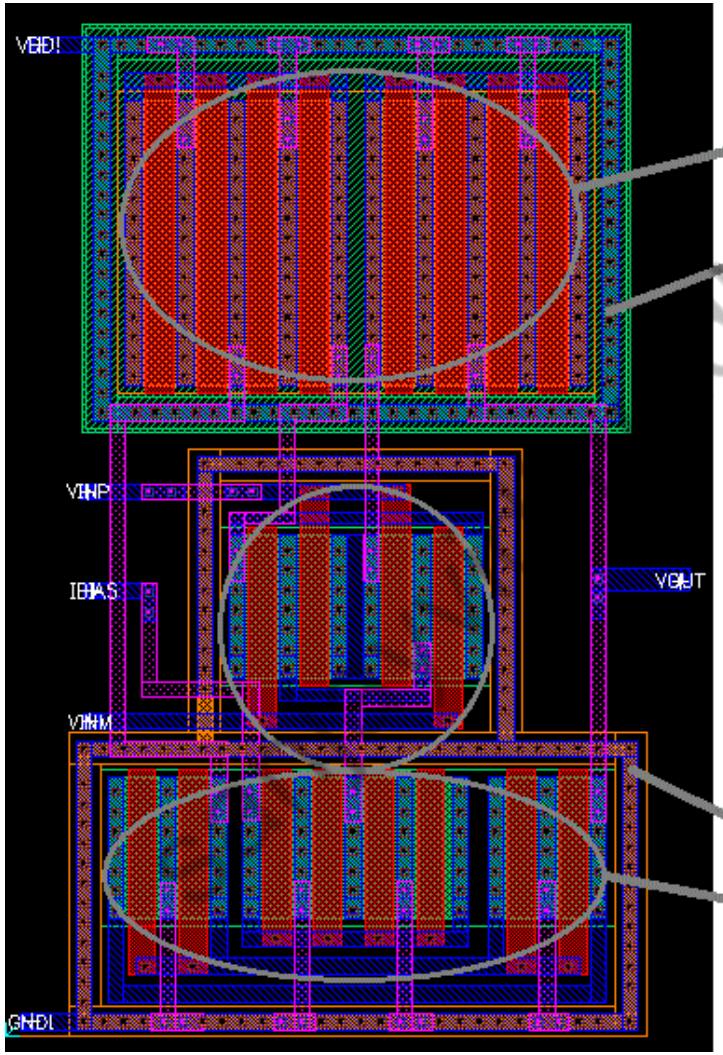
- NMOS Double well : Body not same as Substrate

MOSFET LATCH

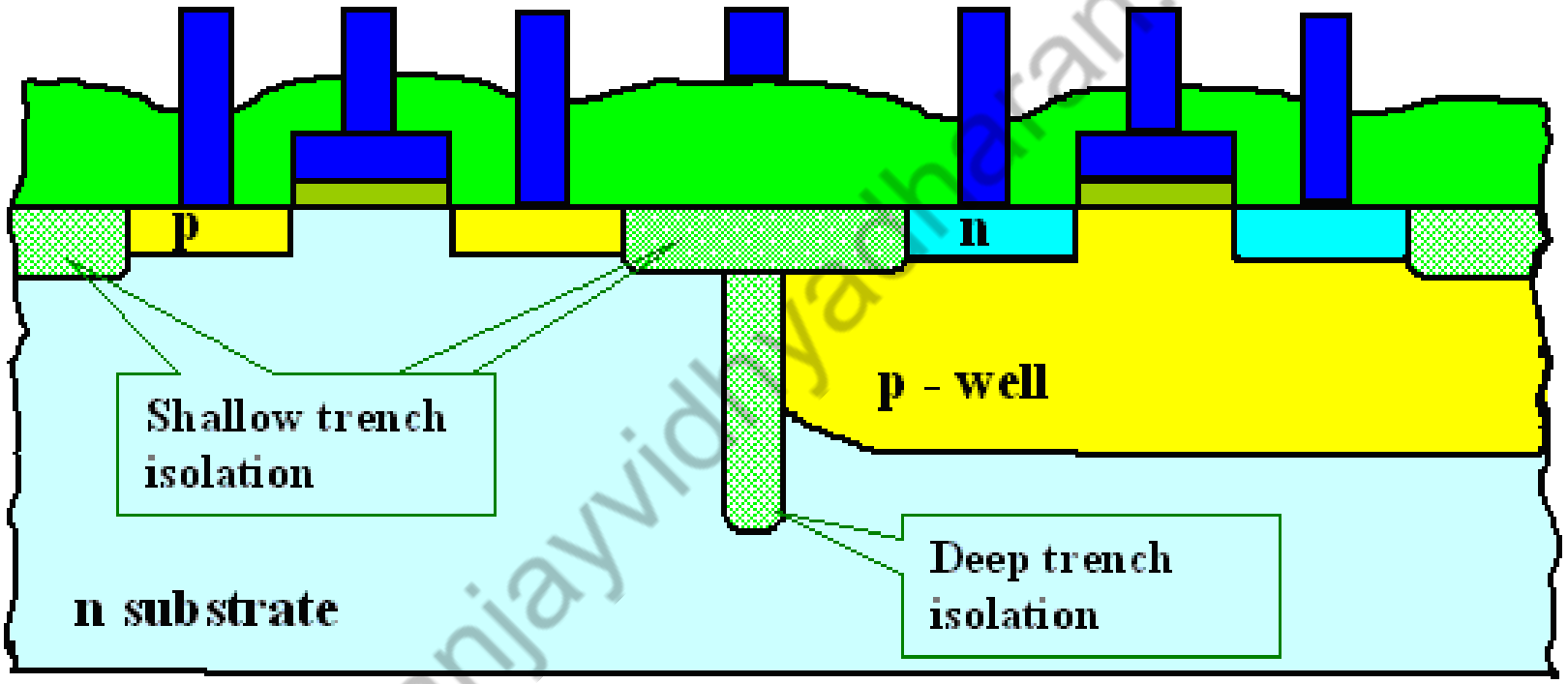




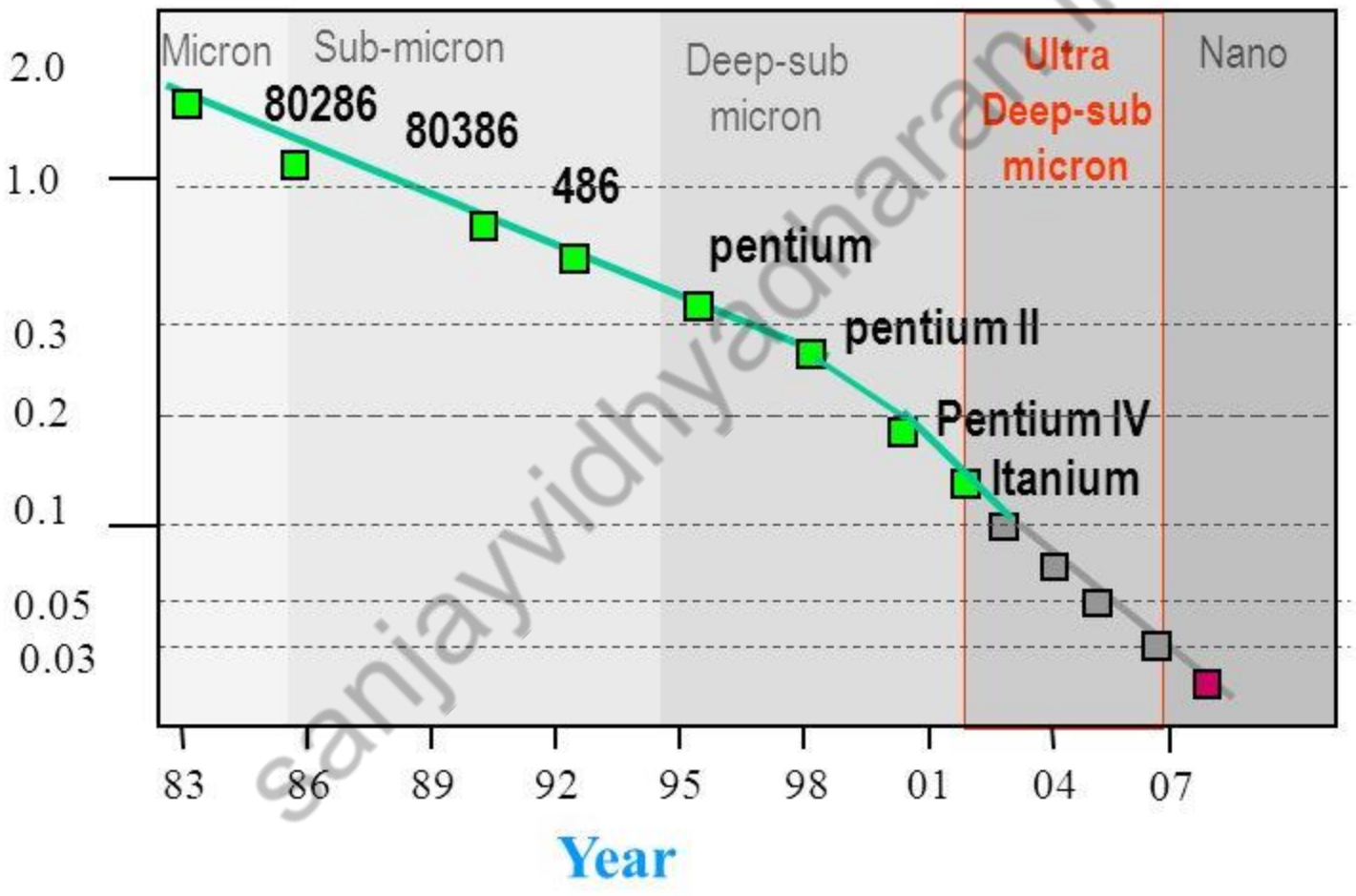
MOSFET LATCH



MOSFET LATCH



Deep-submicron MOSFET operation

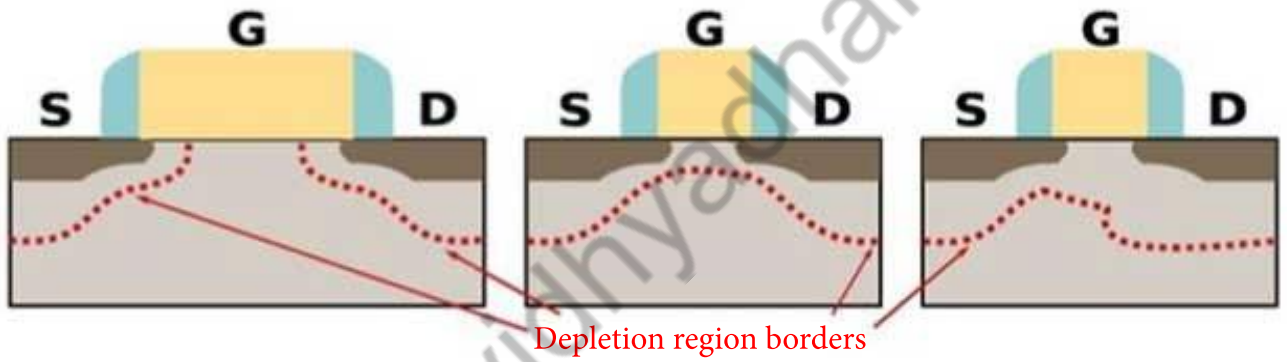


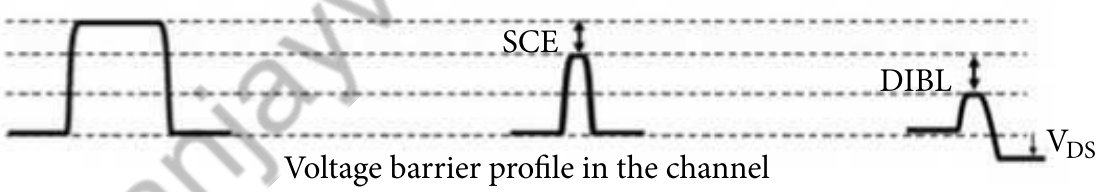
Deep-submicron MOSFET operation

- Threshold voltage reduction
  - VT Roll Off
  - Drain-induced barrier lowering (DIBL)
- Mobility degradation due to a vertical field
- Velocity saturation effects
- Channel length modulation
- Subthreshold (weak inversion) conduction
- Hot-electron effects on output resistance

VT Variation

- VT Roll Off
- Drain-induced barrier lowering (DIBL)





(a) Long channel $V_{DS}=0$

(b) Short channel $V_{DS}=0$

(c) Short channel $V_{DS}\neq 0$

Mobility Degradation

There also exists a normal (vertical) field originating from the gate voltage that further inhibits channel carrier mobility. This effect, which is called mobility degradation, reduces the surface mobility with respect to the bulk mobility.

$$\mu_{n,\,eff} = \frac{\mu_{n0}}{1 + \eta(V_{GS} - V_T)}$$

with μ_{n0} the bulk mobility and η an empirical parameter.

Velocity Saturation Effect

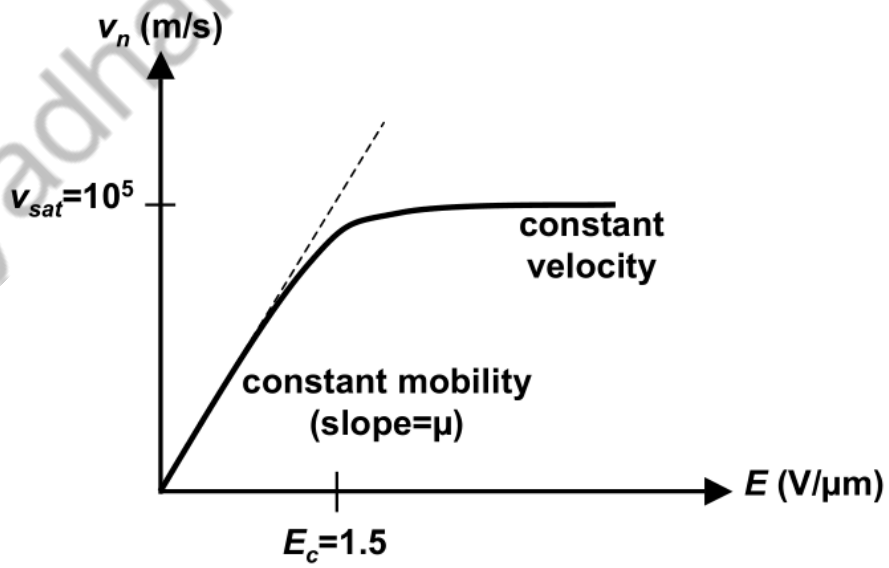
When the electric field reaches a critical value EC the velocity of the carriers tends to saturate.

$$v = \frac{\mu_n E}{1 + E/E_C} \qquad \text{for } E \le E_C$$

$$v = v_{sat} \qquad \text{for } E \ge E_C$$

$$v_{sat} = \begin{cases} 8\times10^6 \text{ cm/s} & \text{for electrons in Si} \\ 6\times10^6 \text{ cm/s} & \text{for holes in Si} \end{cases}$$

$$\mathcal{E}_{sat} = \frac{2v_{sat}}{\mu}$$



Velocity Saturation Effect

- **Linear region:**

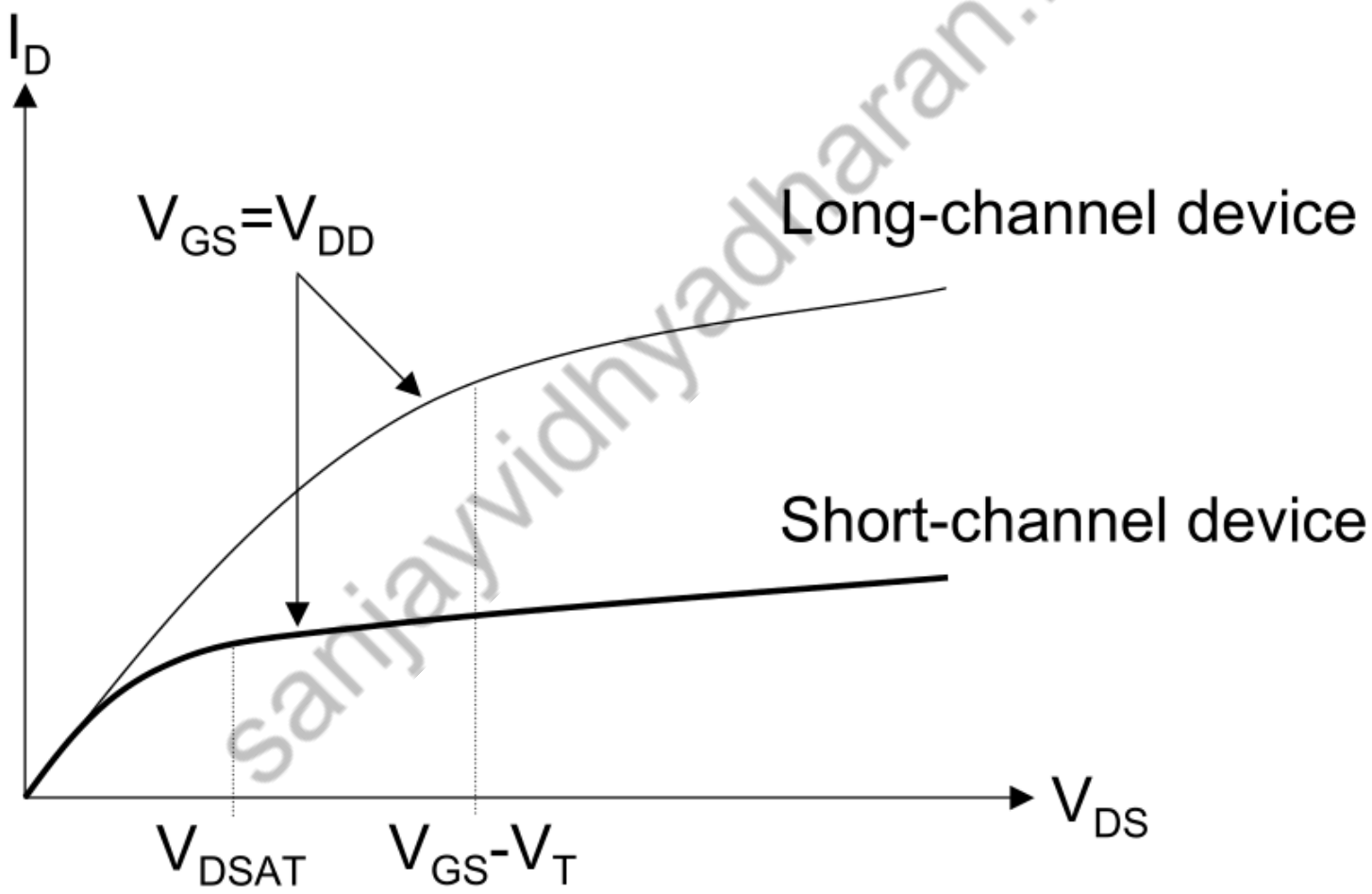
$$I_{DS} = \frac{\frac{W}{L} C_{oxe} \mu_{eff,n} \left(V_{GS} - V_{Tn} - \frac{m}{2} V_{DS} \right) V_{DS}}{1 + \frac{V_{DS}}{\mathcal{E}_{sat} L}}$$

- **Saturation region:**

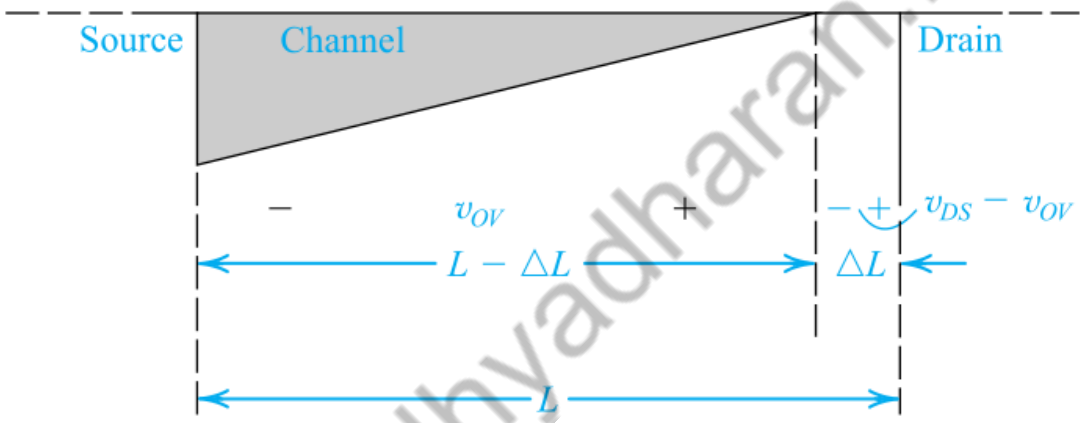
$$I_{DS} = I_{DSsat} = \frac{\frac{W}{2mL} C_{oxe} \mu_{eff,n} \left(V_{GS} - V_T \right)^2}{1 + \frac{V_{GS} - V_T}{\mathcal{E}_{sat} L}} \qquad \mathcal{E}_{sat} = \frac{2 v_{sat}}{\mu}$$

$v_{sat} = 8 \times 10^6$ cm/s
for electrons in Si

Velocity Saturation Effect

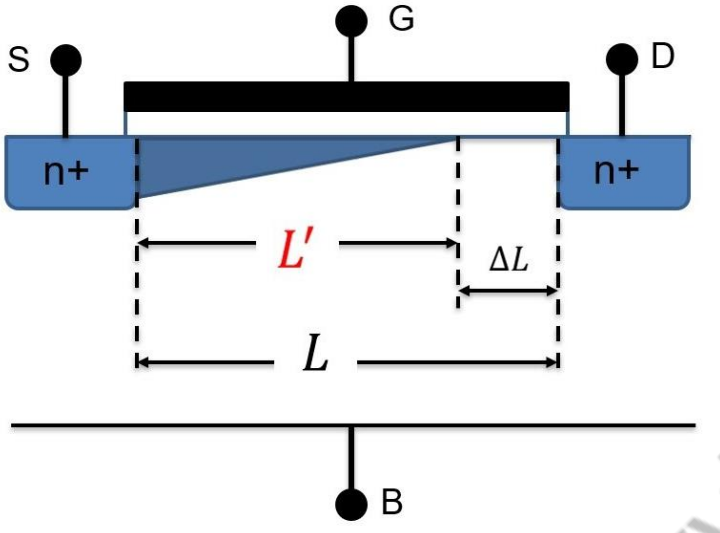


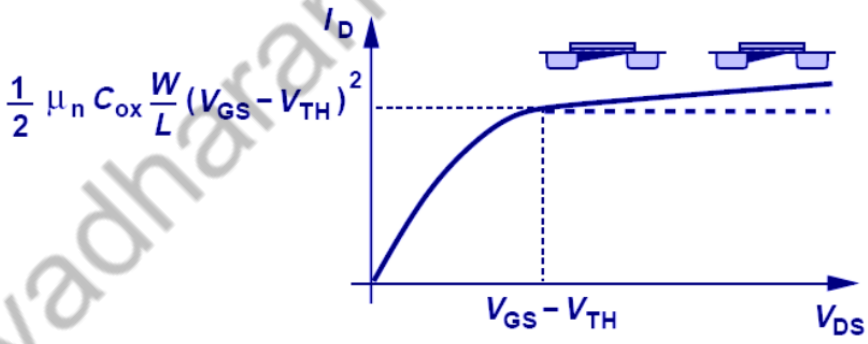
Channel Length Modulation



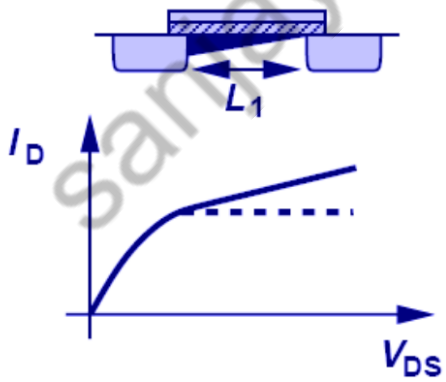
When the V_{DS} is increased beyond V_{OV} , the pinch-off point is moved slightly away from the drain, toward the source. The additional voltage applied to the drain appears as a voltage drop across the narrow depletion region between the end of the channel and the drain region. This voltage accelerates the electrons that reach the drain end of the channel and sweeps them across the depletion region into the drain.

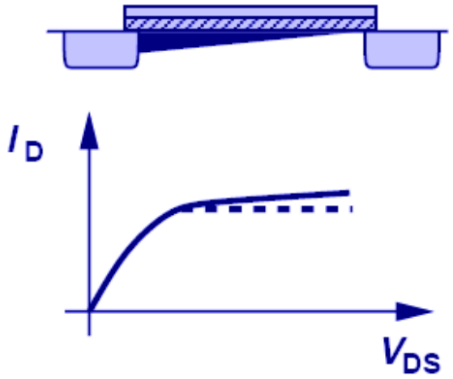
Channel Length Modulation



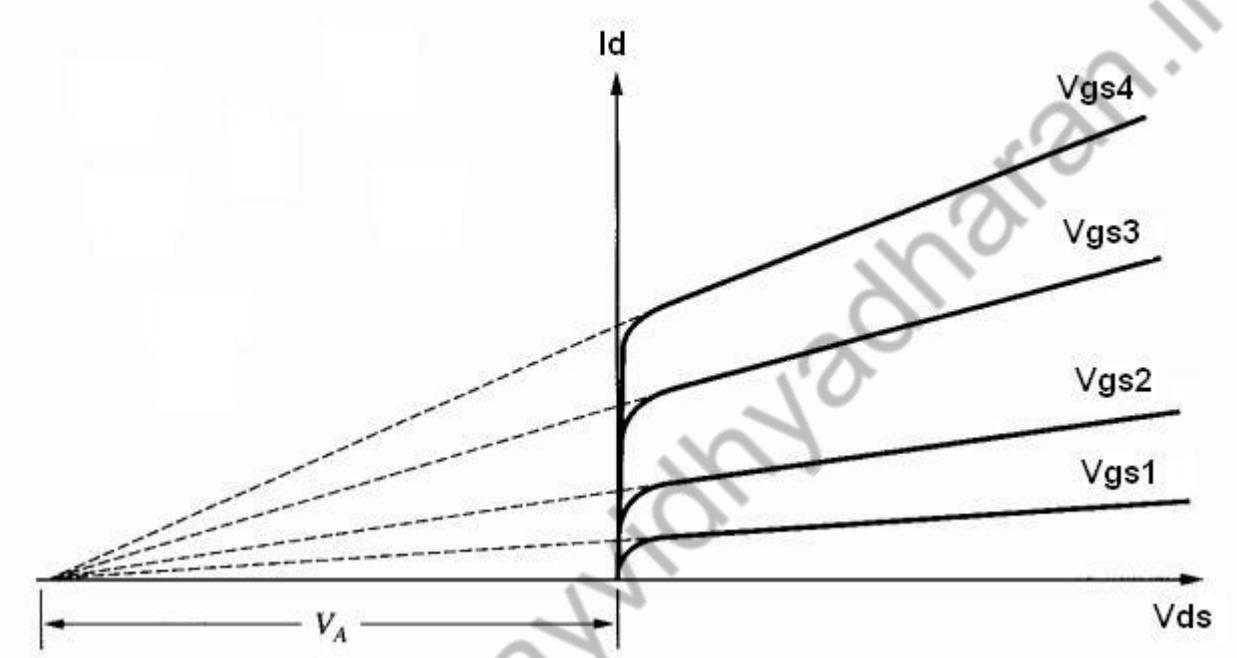


$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2(1+\lambda V_{DS})$$





Channel Length Modulation



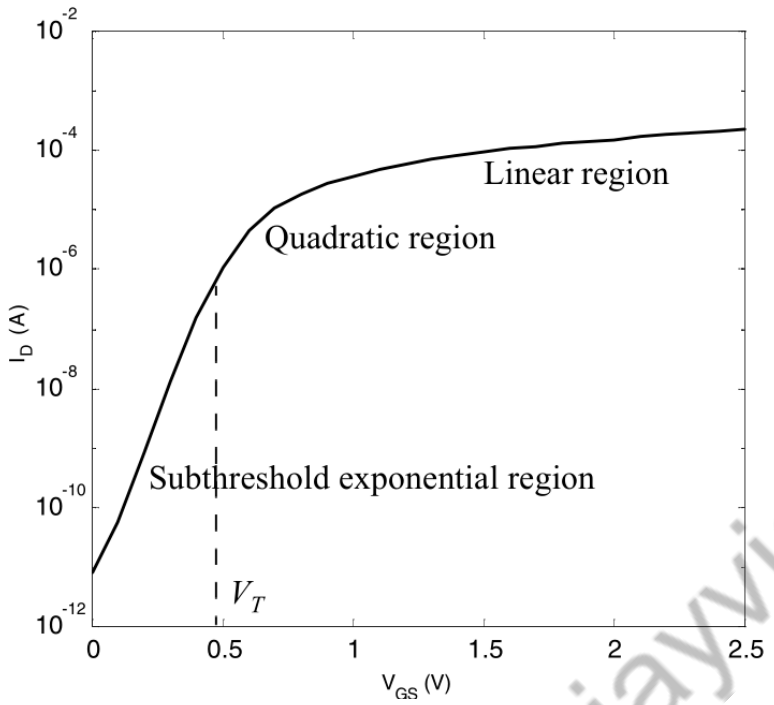
V_A *Early Voltage*

$$\lambda = \frac{1}{V_A}$$

$$r_o \approx \frac{1}{\lambda I_D}$$

$\lambda \propto 1/L$

Subthreshold Conduction



$$I_D = I_S e^{\frac{V_{GS}}{nkT/q}} \left(1 - e^{-\frac{V_{DS}}{kT/q}}\right)$$

where I_S and n are empirical parameters, with $n \geq 1$ and typically ranging around 1.5.

Subthreshold current has some important repercussions. In general, we want the current through the transistor to be as close as possible to zero at $V_{GS} = 0$. This is especially important in the so-called dynamic circuits, which rely on the storage of charge on a capacitor and whose operation can be severely degraded by subthreshold leakage.

Hot Carrier Effects

Increase in the electric field strength causes an increasing energy of the electrons.

- Some electrons are able to leave the silicon and tunnel into the gate oxide.
- Such electrons are called “Hot carriers”.
- Electrons trapped in the oxide change the V_T of the transistors.
- This leads to a long term reliability problem.
- For an electron to become hot an electric field of 10^4 V/cm is necessary.
- This condition is easily met with channel lengths below 1µm.

Thank you