



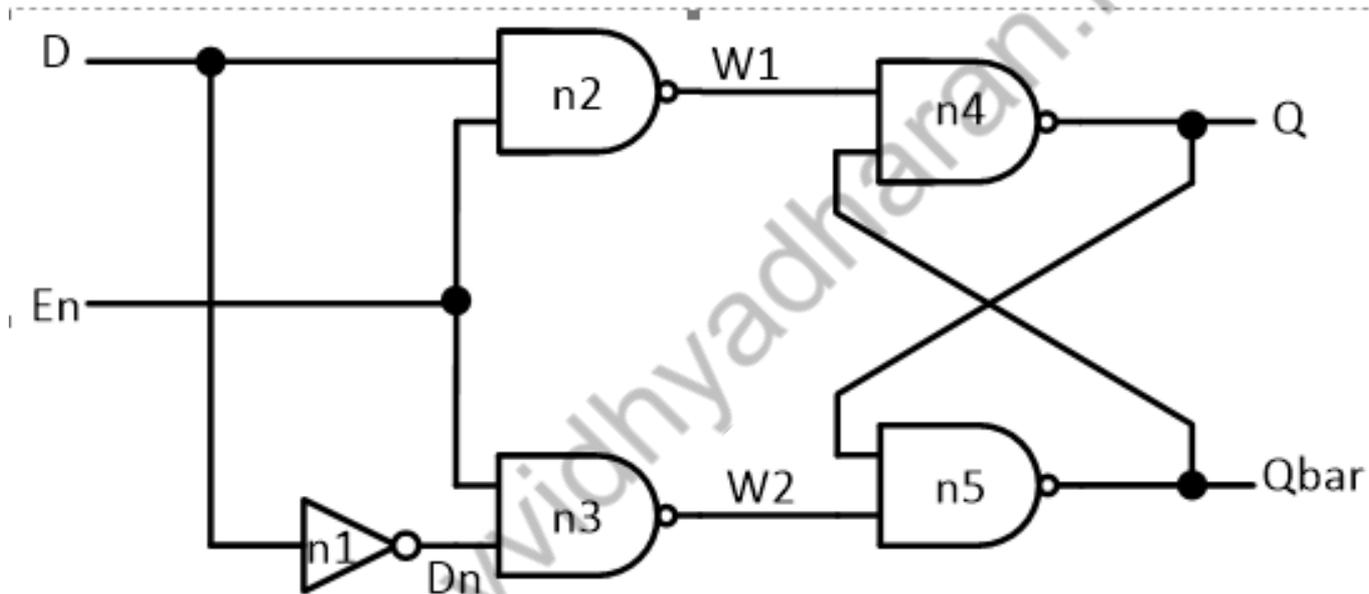
VLSI SYSTEMS AND ARCHITECTURE

2021-22

Lab-8 : Sequential Circuit Design using Flip-flops in Xilinx

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D Latch



D Latch

```
module D_latch(  
    input D,  
    input En,  
    output Q,  
    output Qbar  
);  
wire Dn, W1, W2;  
  
not n1(Dn,D); // NOT gate instance  
  
nand n2(W1, D, En); // NAND gate instance for n2  
  
//similarly write the NAND instances n3.  
  
//Q and Qbar can also be used as inputs for example  
//n4 NAND instance can be written as shown below  
nand n4(Q, W1, Qbar);  
  
//similarly write the NAND instances n5.  
  
endmodule
```

D Flip-Flop

```
module DFF (  
input D,  
input Clk,  
output reg Q);  
always @ (posedge Clk)  
begin  
Q <= D;  
end  
endmodule
```

D Flip-Flop

```
module DDF_test;
    // Inputs reg D; reg Clk;
    // Outputs wire Q;
    // Instantiate the Unit Under Test (UUT)
    DFF_CLK uut ( .D(D), .Clk(Clk), .Q(Q) );
    initial begin
        // Initialize Inputs
        Clk = 0;
        repeat (9)
            #100 Clk = ~ Clk;
    end
    initial begin
        // Initialize Inputs
        D = 0;
        repeat (6)
            #225 D = ~ D;
    end
endmodule
```

D Flip-flop with Reset

```
module DFF_R(input D, input Clk, input Reset,
output reg Q);
always @ (posedge Clk, posedge Reset)
begin
if (Reset==1)
Q <= 1'b0;
else
Q <= D;
end
endmodule
```

D Flip-flop with Reset

Testbench for D Flip-flop with Reset

```
initial begin
```

```
    Clk = 0;  
    repeat (9)  
        #100 Clk = ~ Clk;
```

```
end
```

```
initial begin
```

```
    D = 0;  
    repeat (6)  
        #225 D = ~ D;
```

```
end
```

```
initial begin
```

```
    Reset <= 0'b0;  
    # 350;  
    Reset <= 1'b1;  
    # 20;  
    Reset <= 0'b0;
```

```
end
```

Thank you