VLSI Design : 2021-22
Lecture 13
Domino Logic

By Dr. Sanjay Vidhyadharan

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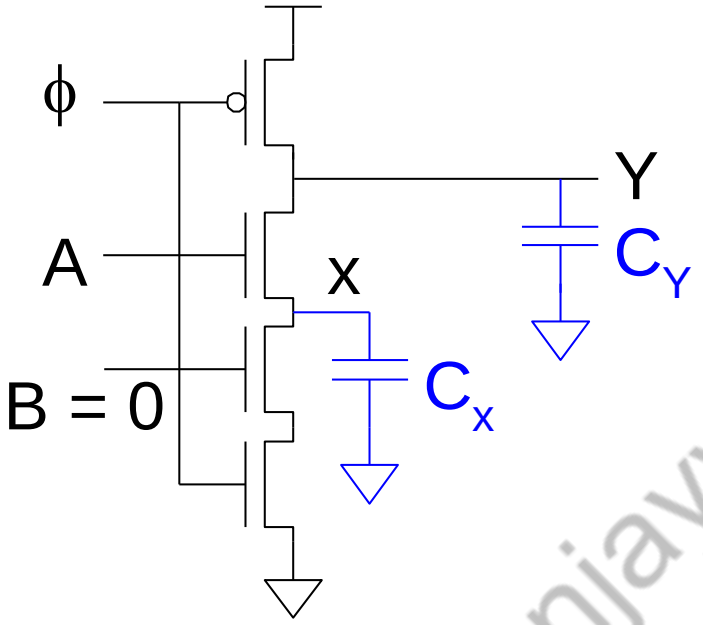
Dynamic Logic

- **Dynamic Logic Suffers from Charge Sharing Phenomenon**



Case1. $\Delta V_{out} < V_{Tn} - V_{out}$

$$V_{DD} \cdot C_Y = V_Y C_Y + (V_{DD} - V_{Tn}) C_X$$

$$\Delta V_{out} = - \frac{(V_{DD} - VT_n) C_X}{C_Y}$$

$$C_X << C_Y$$

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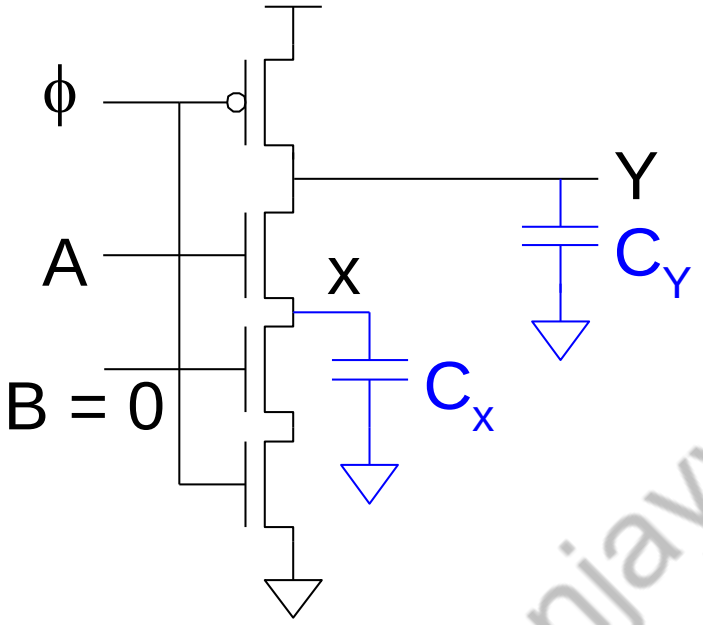
Dynamic Logic

- **Dynamic Logic Suffers from Charge Sharing Phenomenon**



Case2. $\Delta V_{out} > V_{Tn} - V_{out}$

$$V_{DD}.C_Y = V_Y C_Y + V_X C_X$$

$$V_{DD}.C_Y = V_Y C_Y + V_Y C_X$$

$$V_{DD}.C_Y = (V_{DD} + \Delta V_{out})(C_Y + C_X)$$

$$\Delta V_{out} = -\frac{V_{DD} C_X}{C_{Y+} C_X}$$

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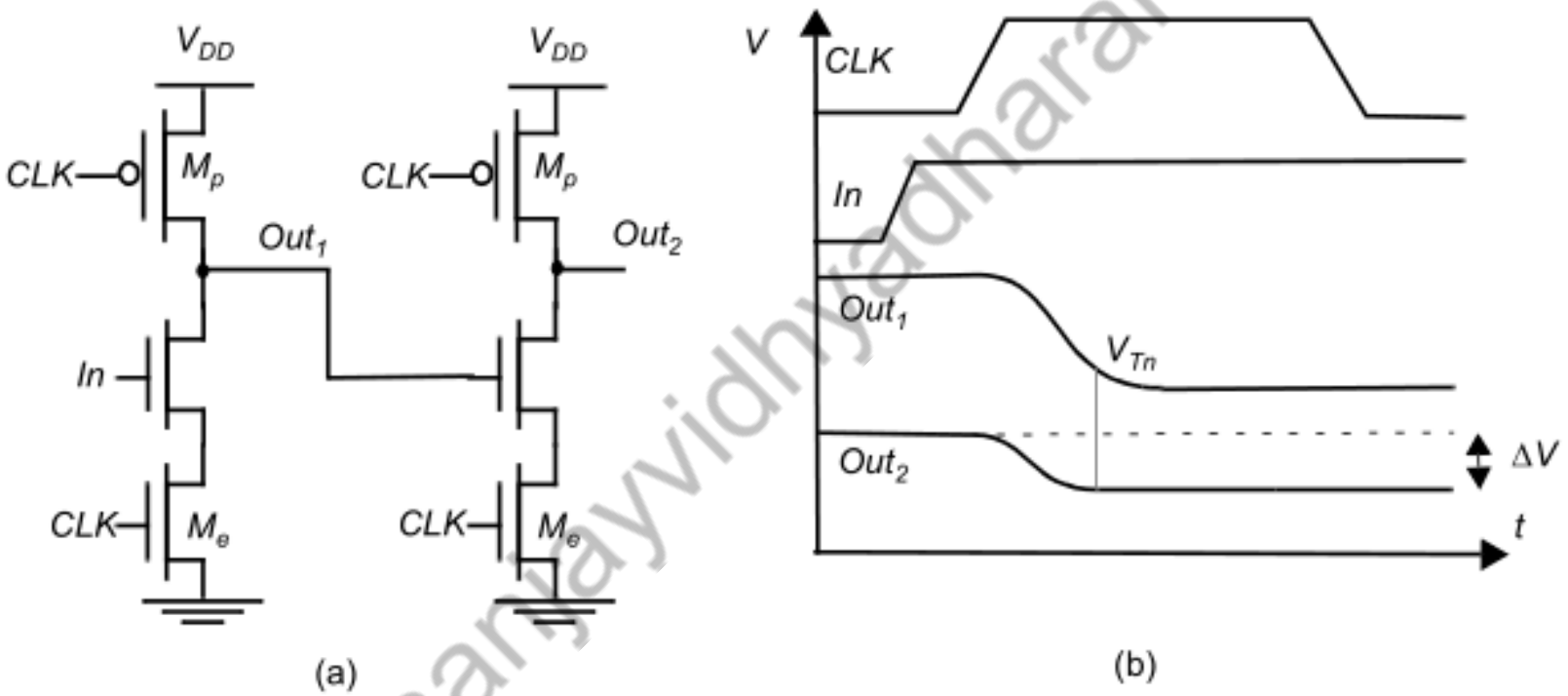
Dynamic Logic

- **Cascading Dynamic Gates**



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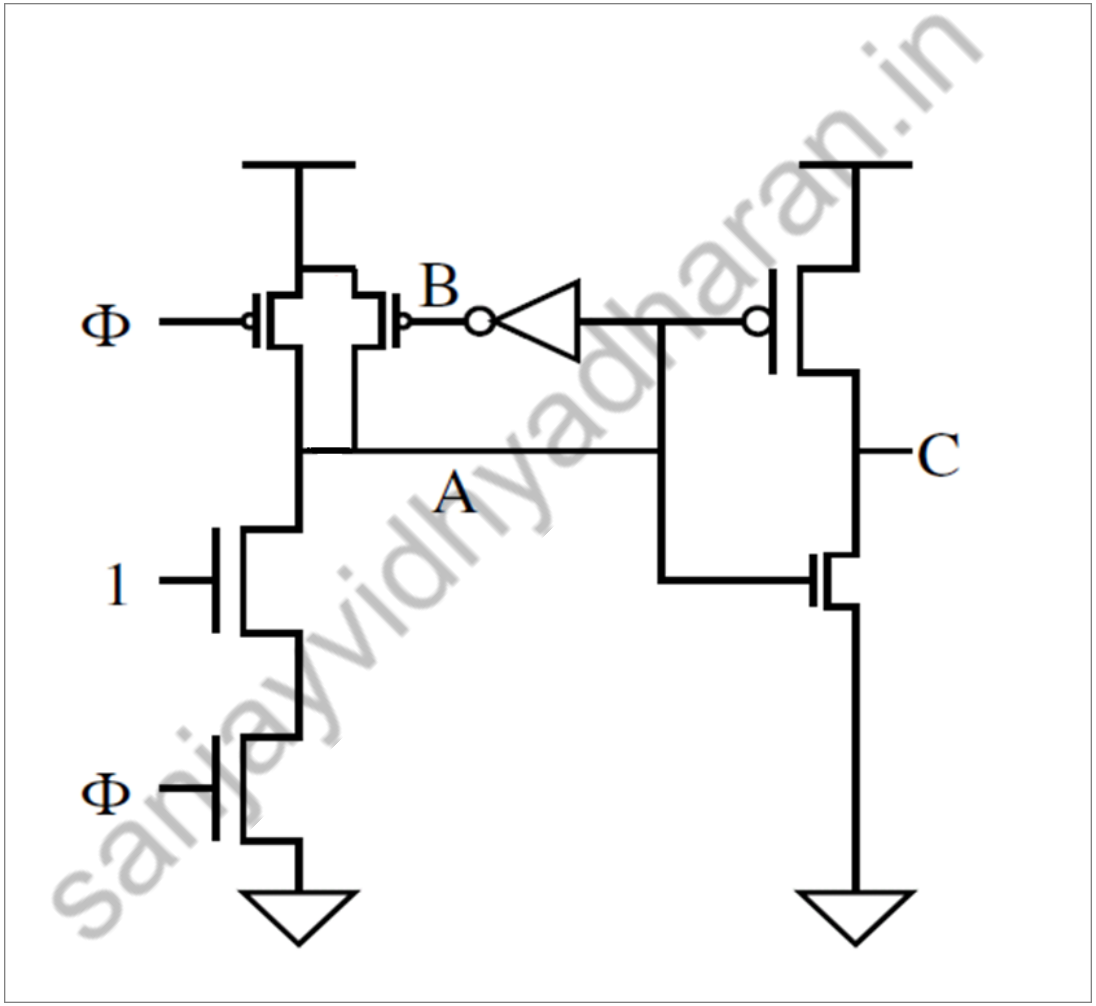
Domino Logic



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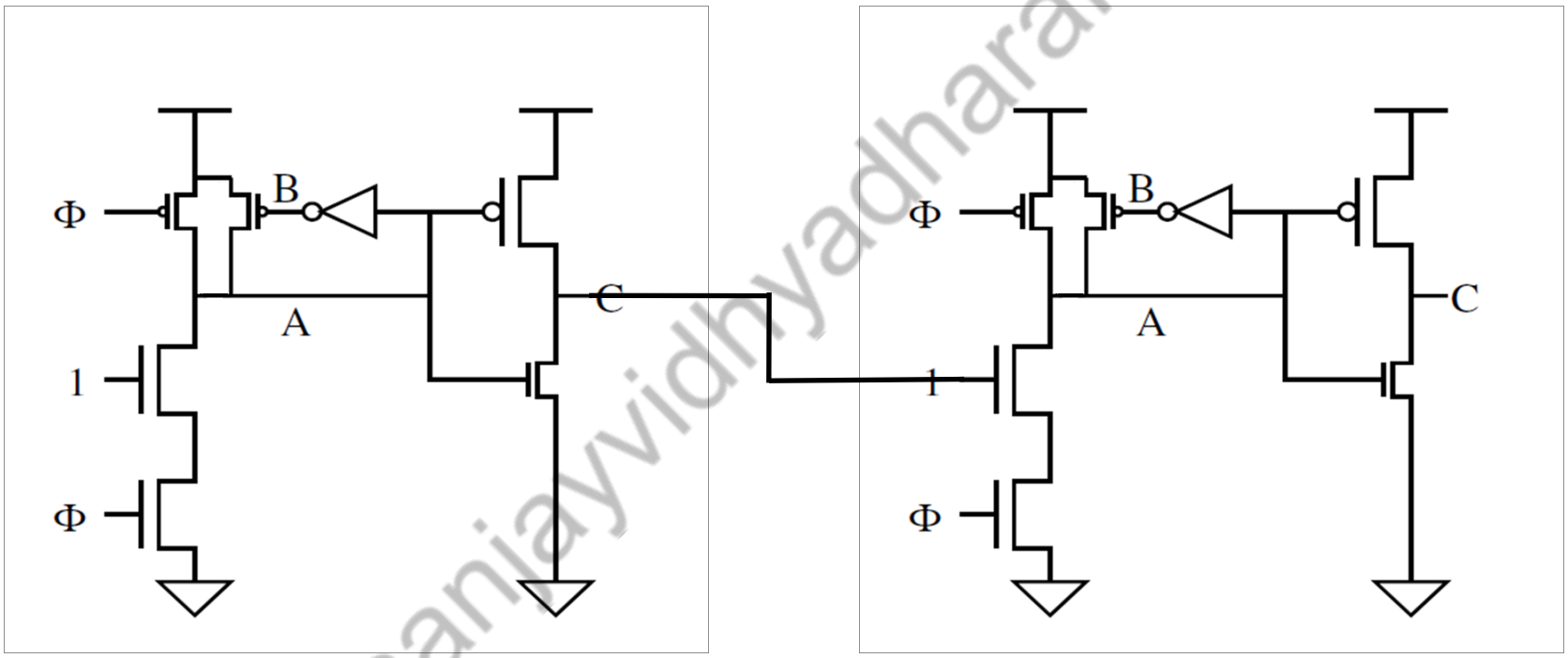
Domino Logic

- **Cascading Domino Logic**



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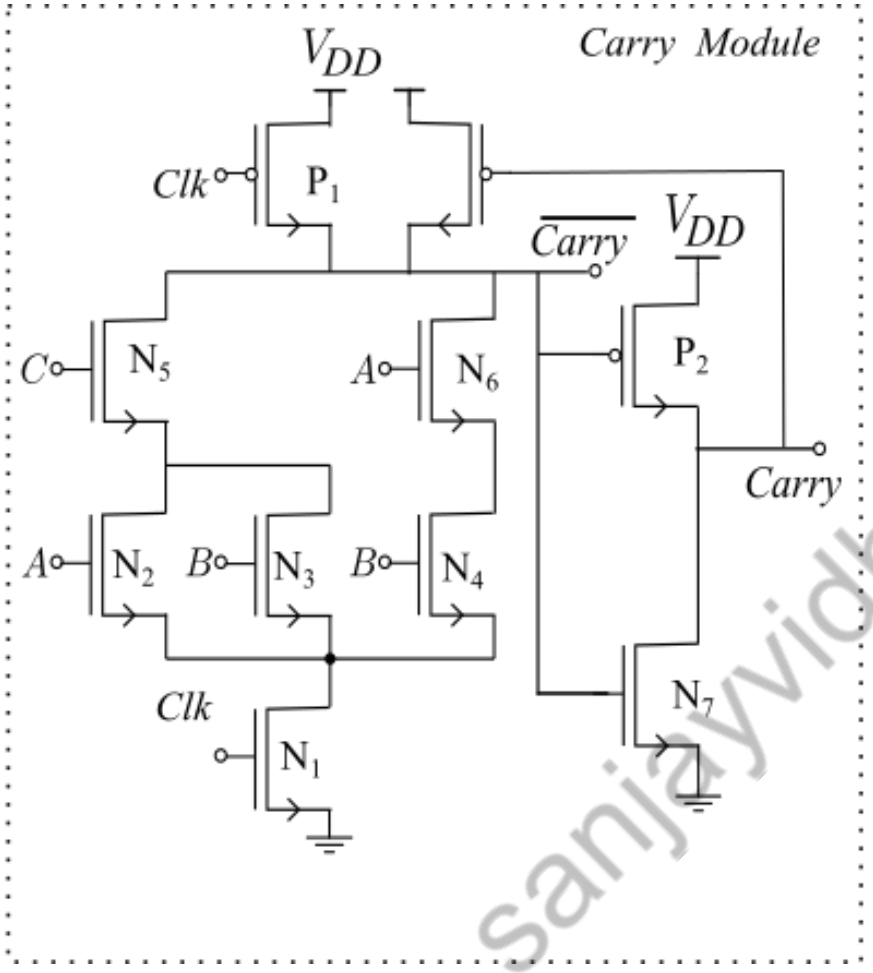
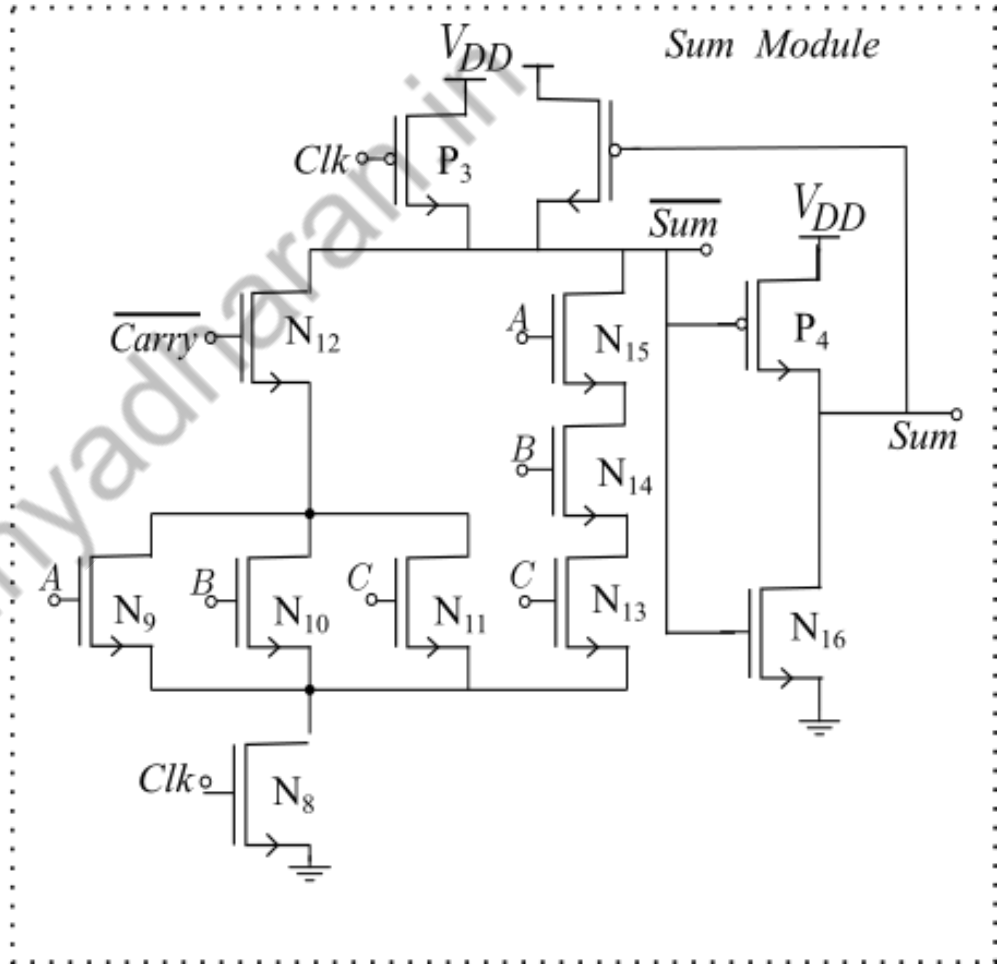
Domino Logic





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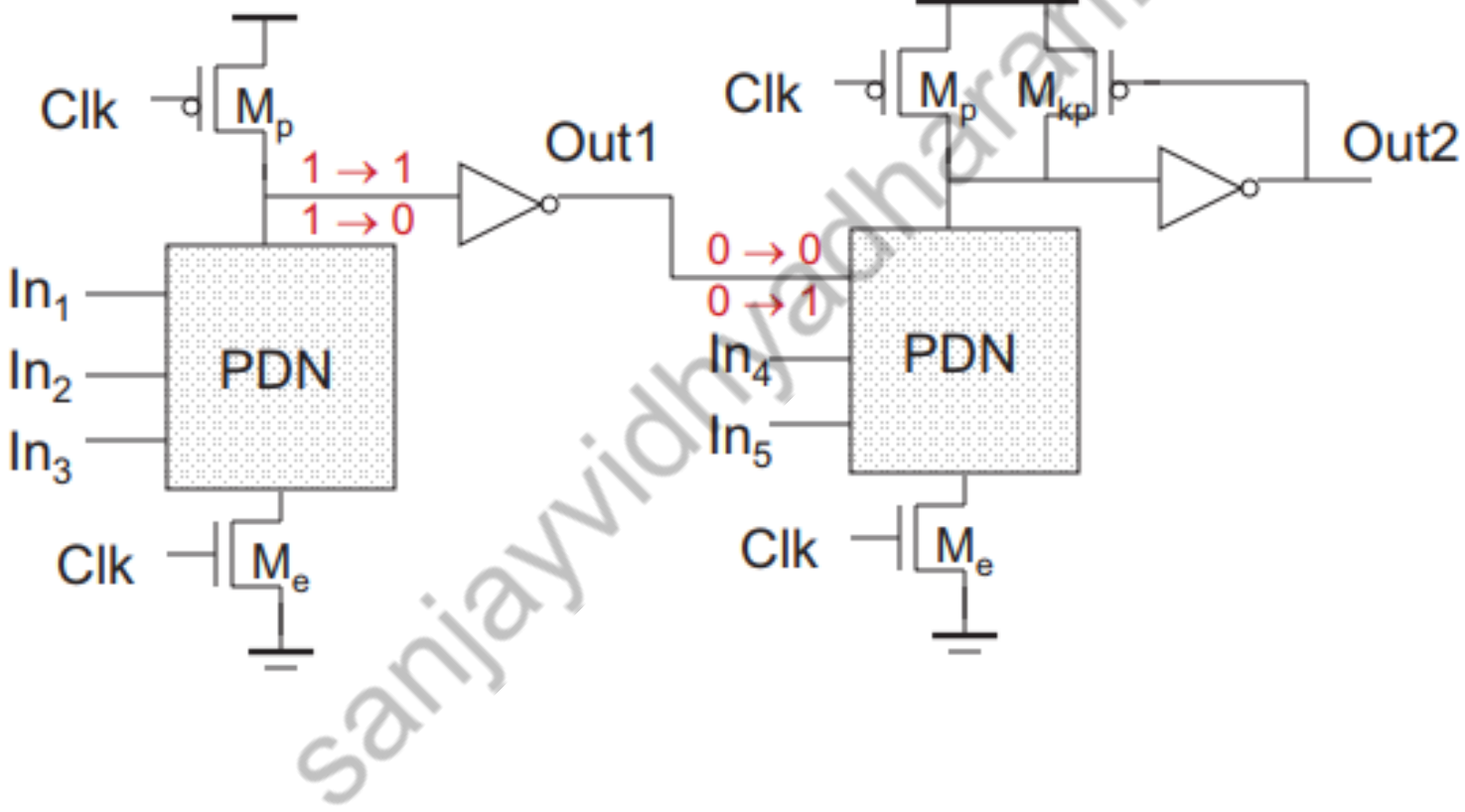
22T Domino Full Adder

Domino Logic



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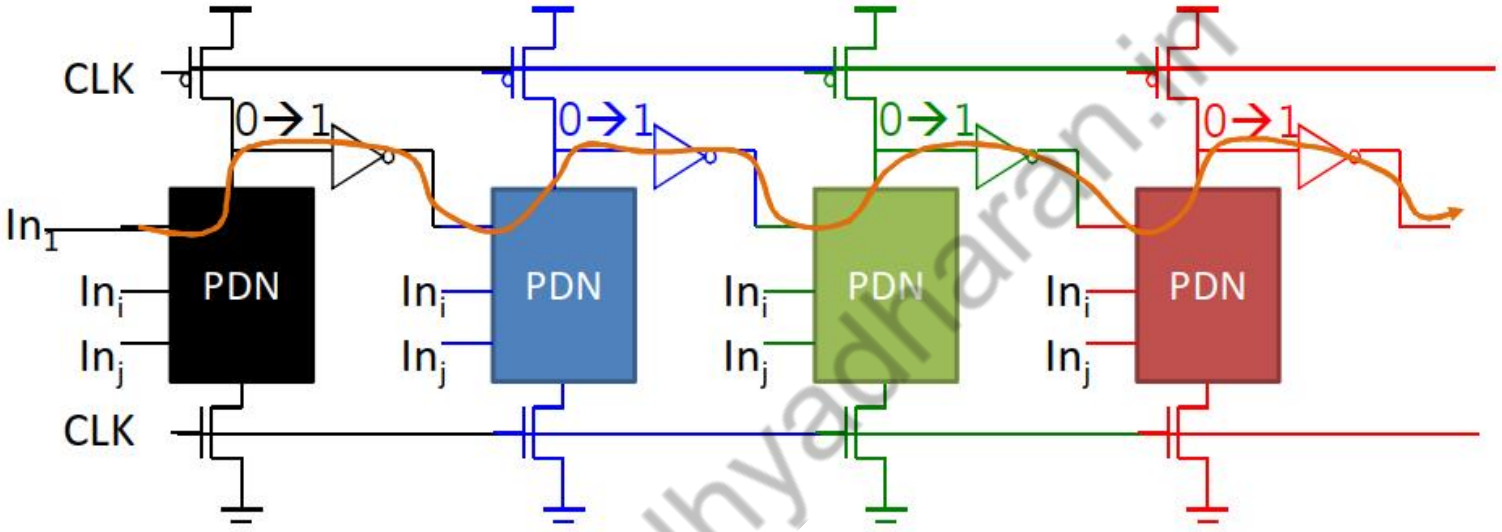
Domino Logic



- Behave like falling dominos…

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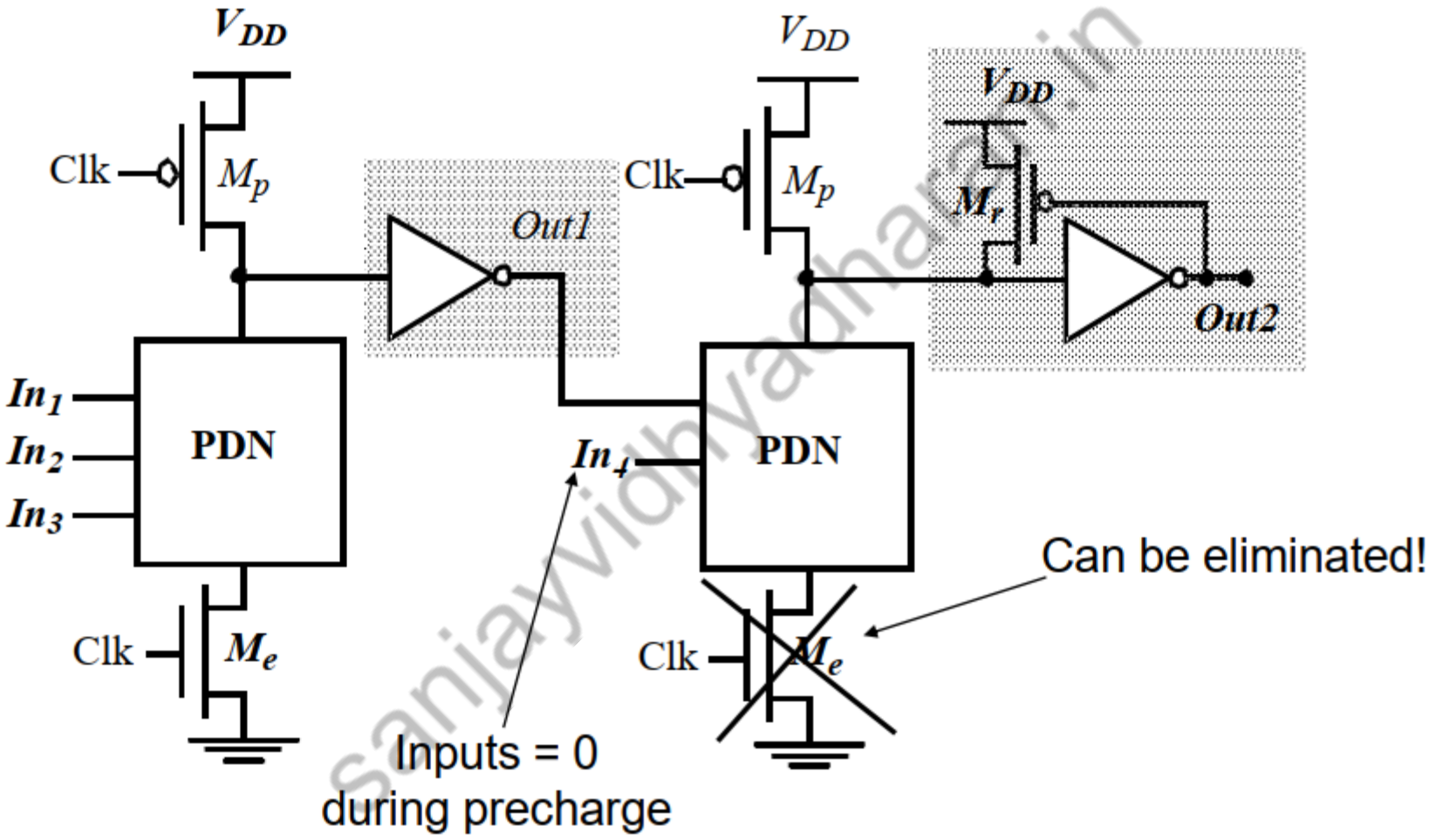
Designing Domino Logic



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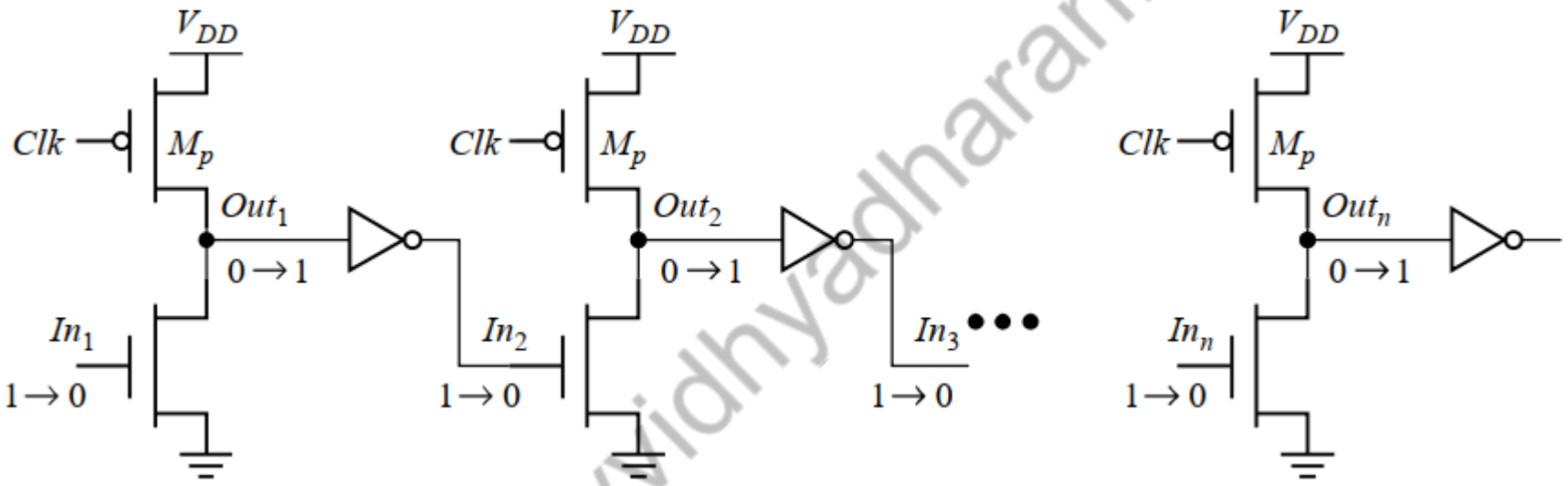
Designing Domino Logic

Footless Domino



Pre-charge is rippling – short-circuit current

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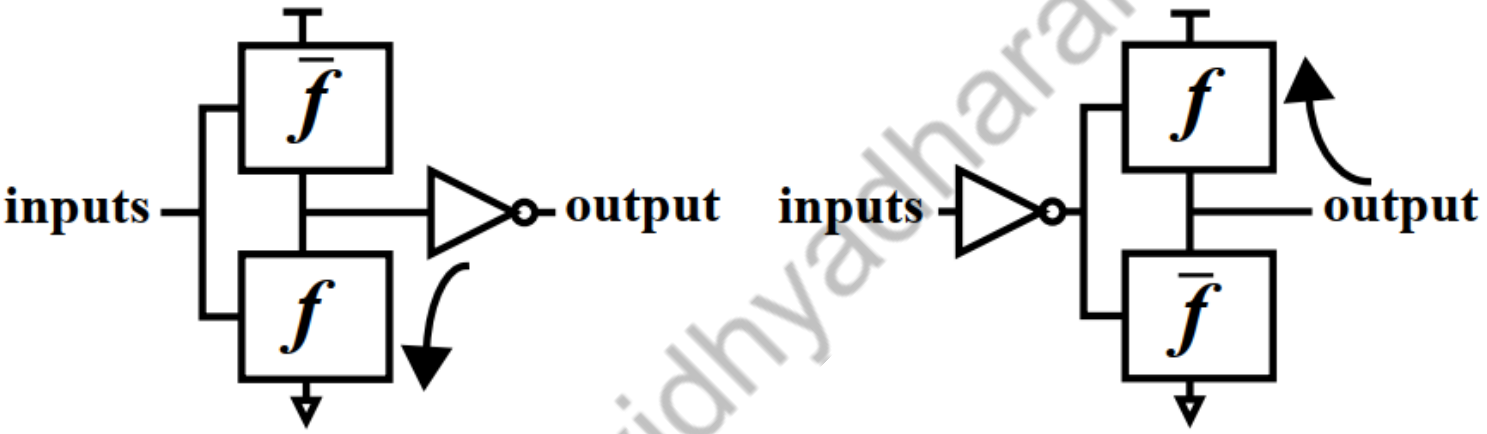
Designing Domino Logic

Domino cannot implement inverting switching functions, such as a NOT gate and an XOR gate



Forms for implementing a non-inverting function f

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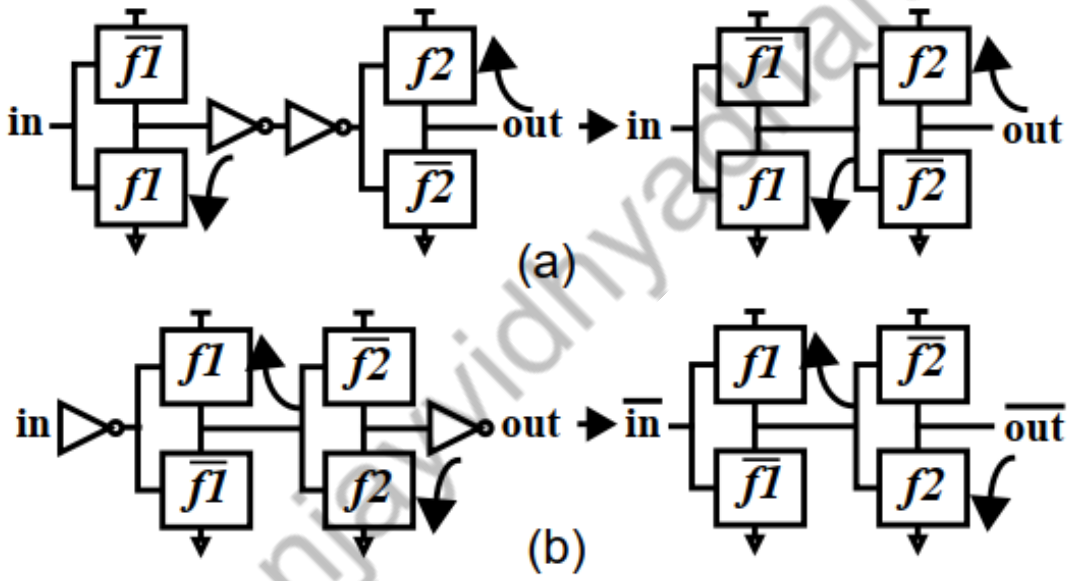
Designing Domino Logic

Domino cannot implement inverting switching functions, such as a NOT gate and an XOR gate



Merging of two non-inverting functions *f1* and *f2*

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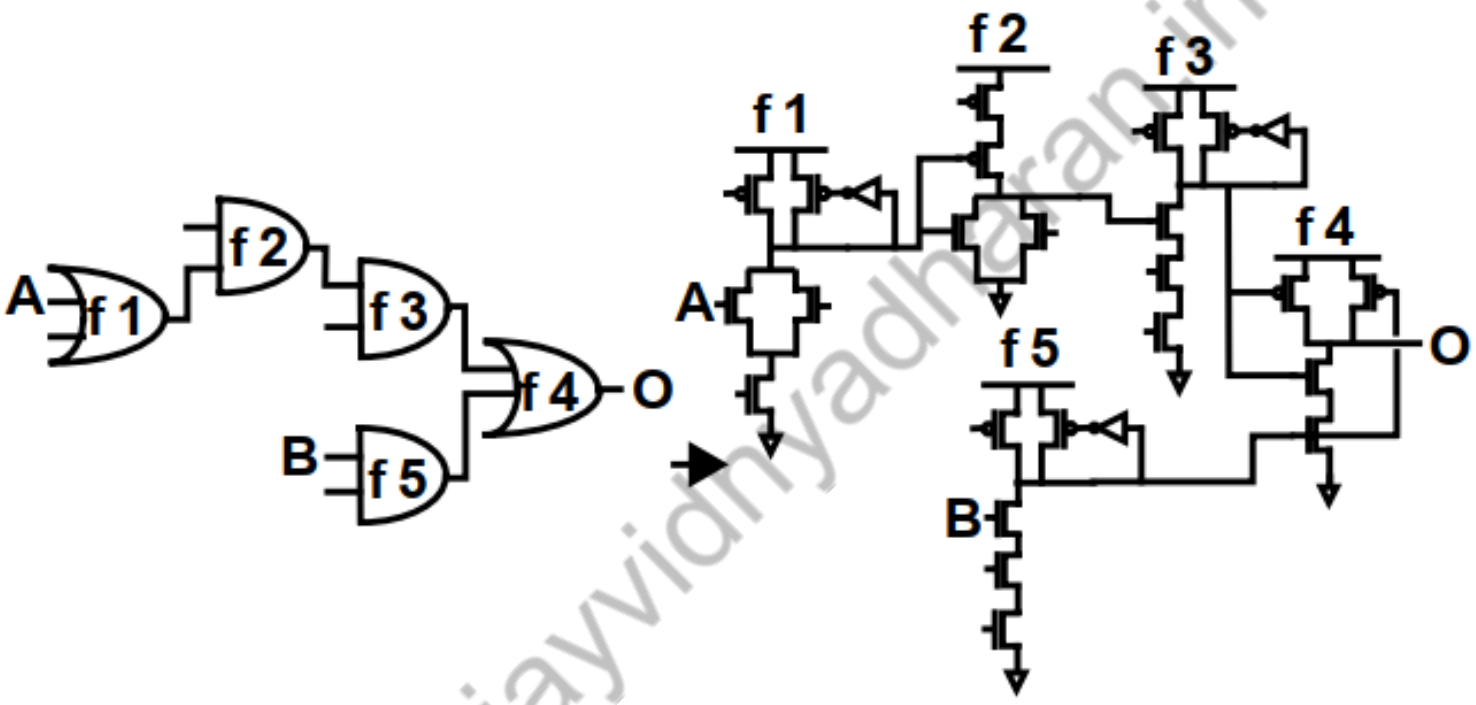
Designing Domino Logic



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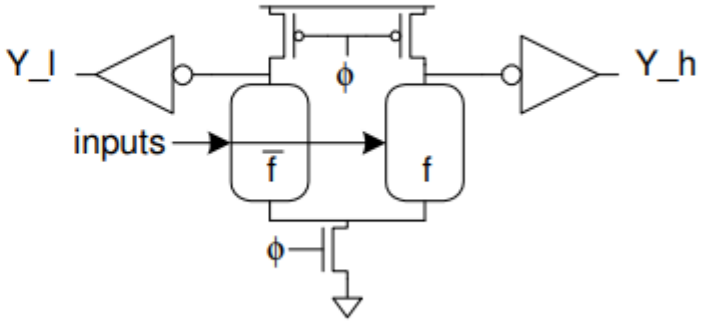
However, generating a unate network from a random logic network may require logic duplication since both positive and negative signal phases may be needed.

Dual-Rail Domino Logic

- Domino only performs noninverting functions:
  - AND, OR but not NAND, NOR, or XOR
- Dual-rail domino solves this problem
  - Takes true and complementary inputs
  - Produces true and complementary outputs

sig_h	sig_l	Meaning
0	0	Precharged
0	1	'0'
1	0	'1'
1	1	invalid



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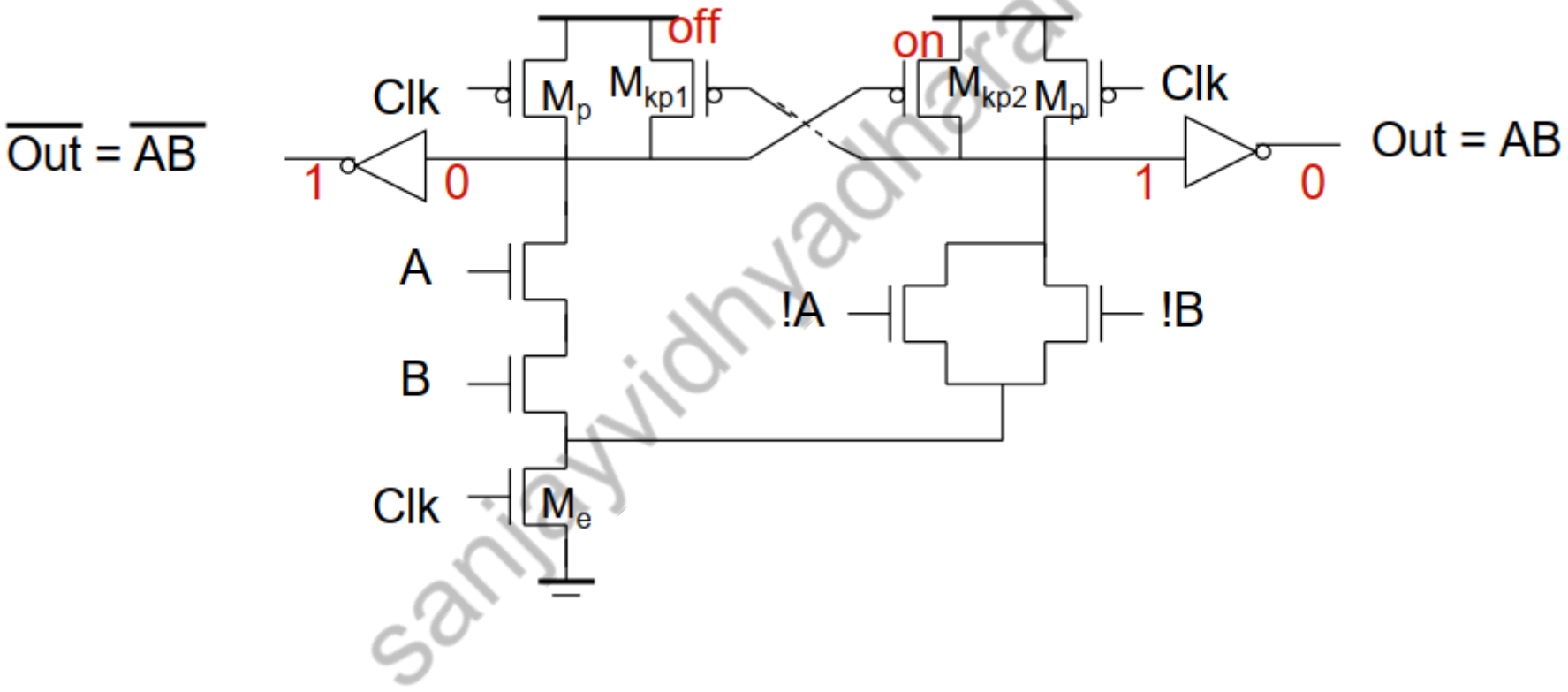
Differential (Dual Rail) Domino



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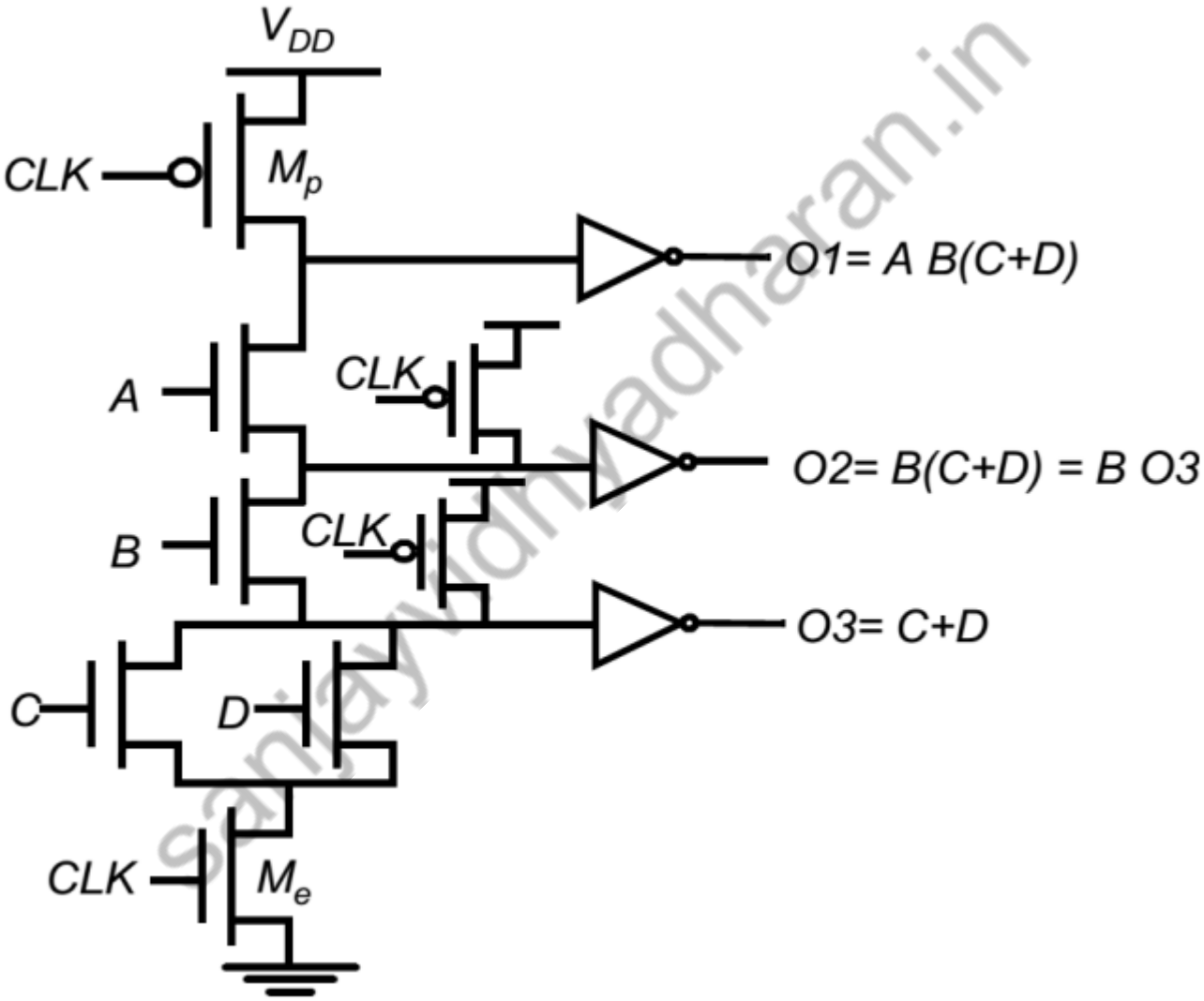
Multiple-Output Domino



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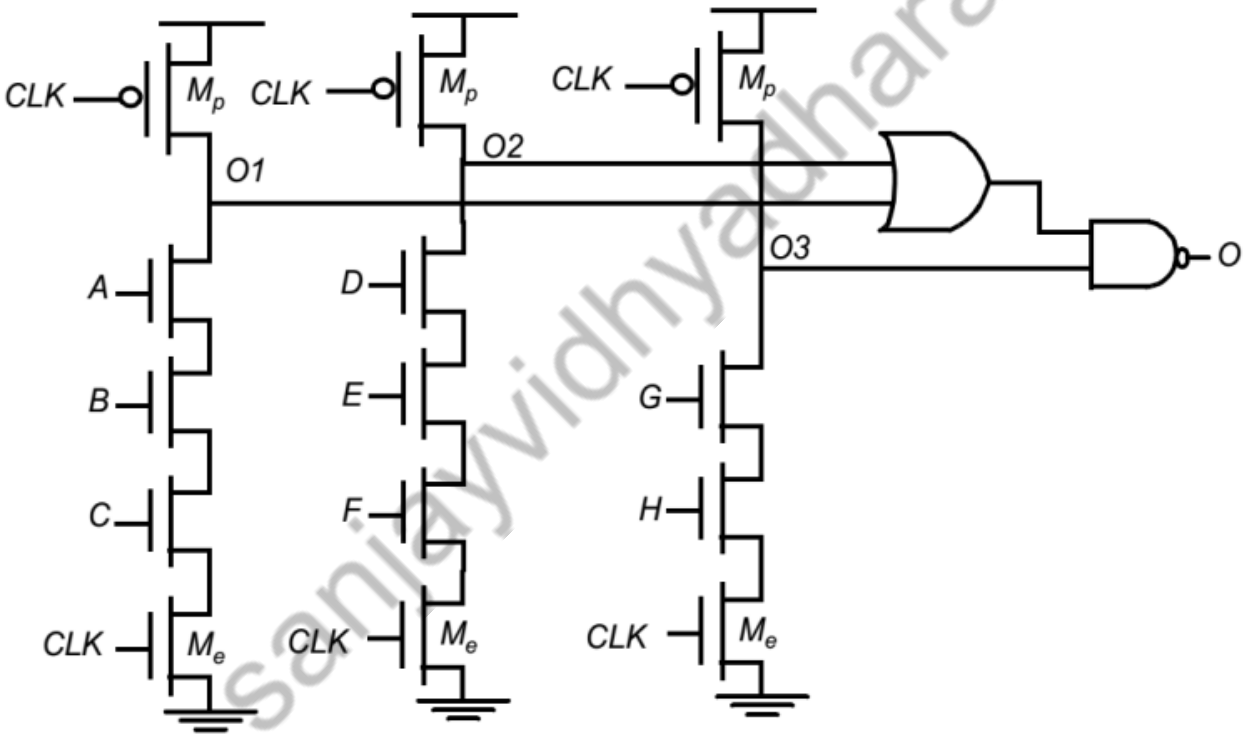
Compound Domino logic

$O = A\,B\,C\,D\,E\,F + GH.$

$O = ABC\,.\,DEF + GH$

$O = \{[(ABC)' + (DEF)']'.(GH)'\}'$



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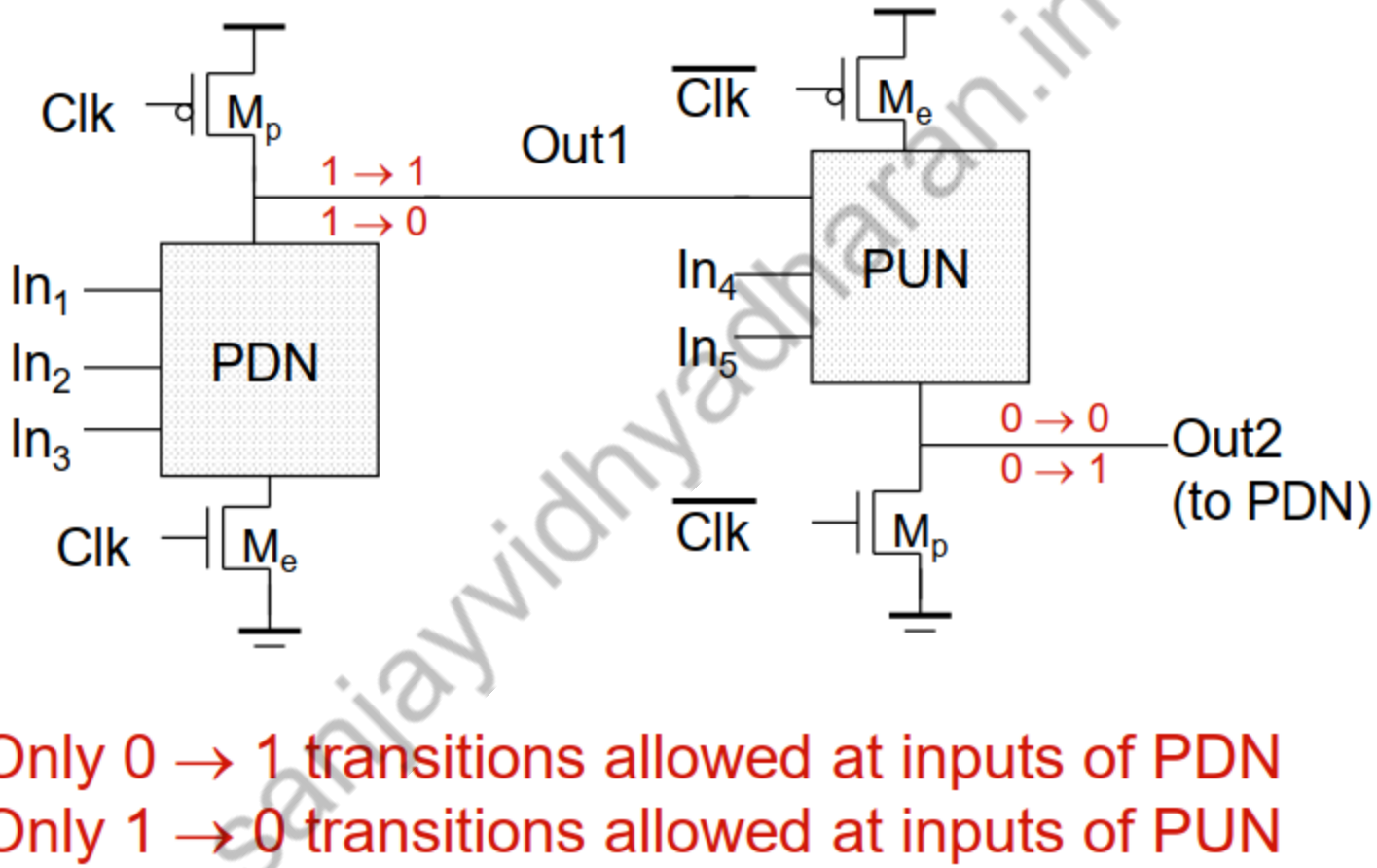
Large dynamic stacks are replaced by parallel structures with small fan-in and complex CMOS gates

np-CMOS



Only 0 → 1 transitions allowed at inputs of PDN

Only 1 → 0 transitions allowed at inputs of PUN

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A disadvantage of the *np*-CMOS logic style is that the *p*-tree blocks are slower than the *n*-tree modules, due to the lower current drive of the PMOS transistors in the logic network. Equalizing the propagation delays requires extra area.

Thank you

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