Advanced VLSI Design: 2021-22
Lecture 12-B: Low Power VLSI Design
Part-2: Architecture, Algorithmic & RTL Level Optimization

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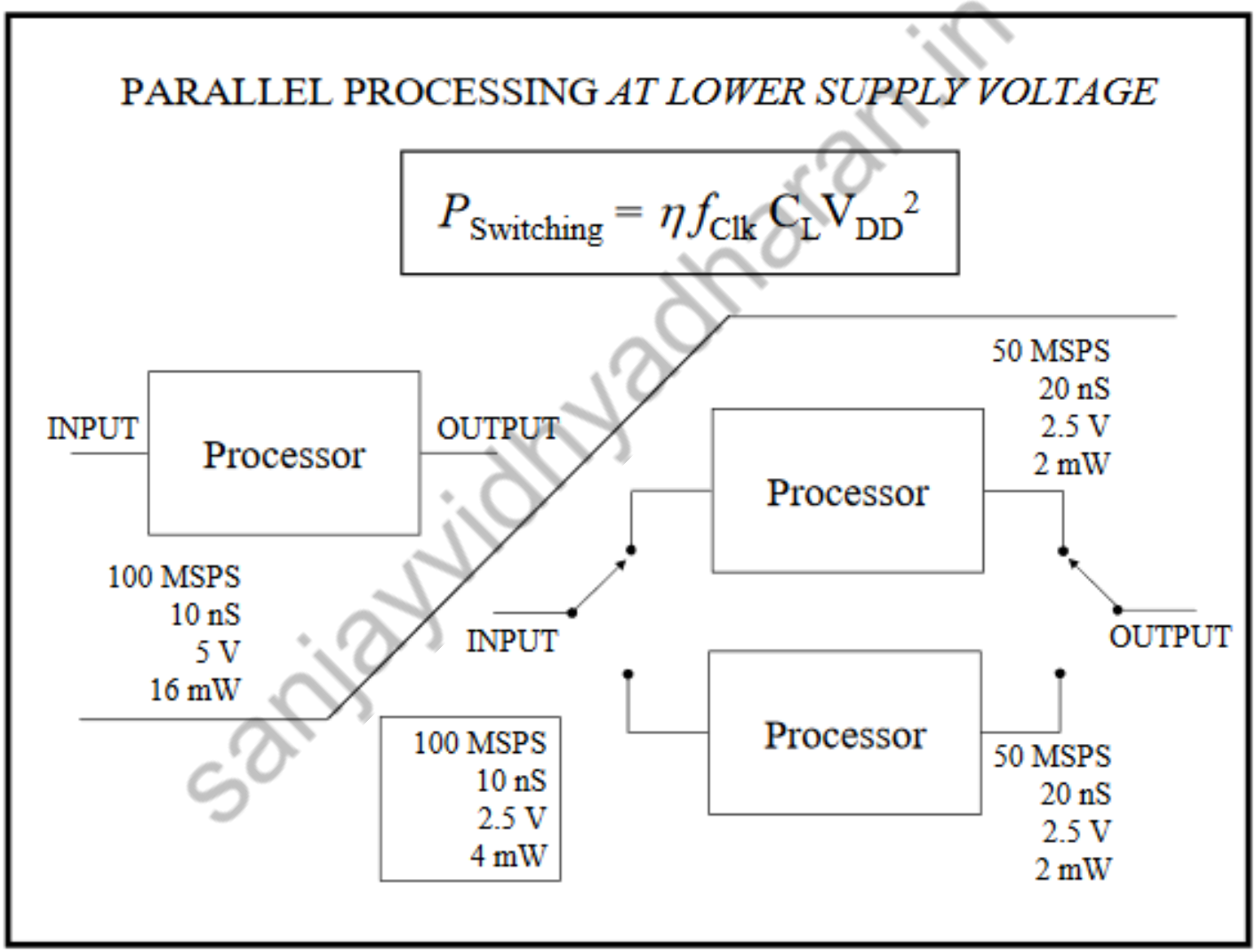
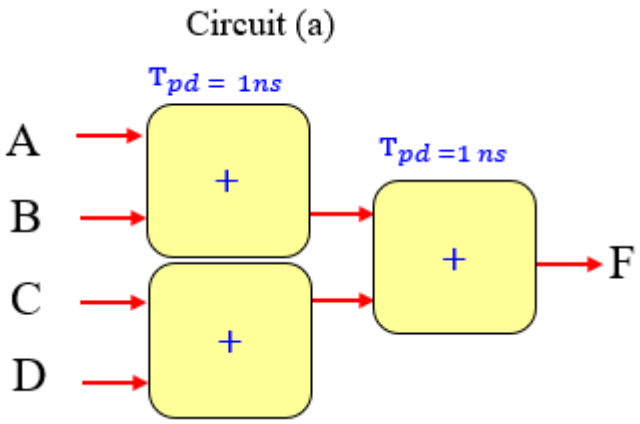
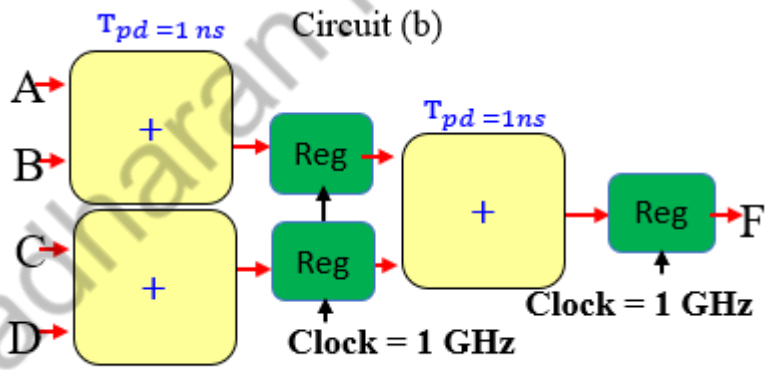
Architecture-Level Design – Parallelism



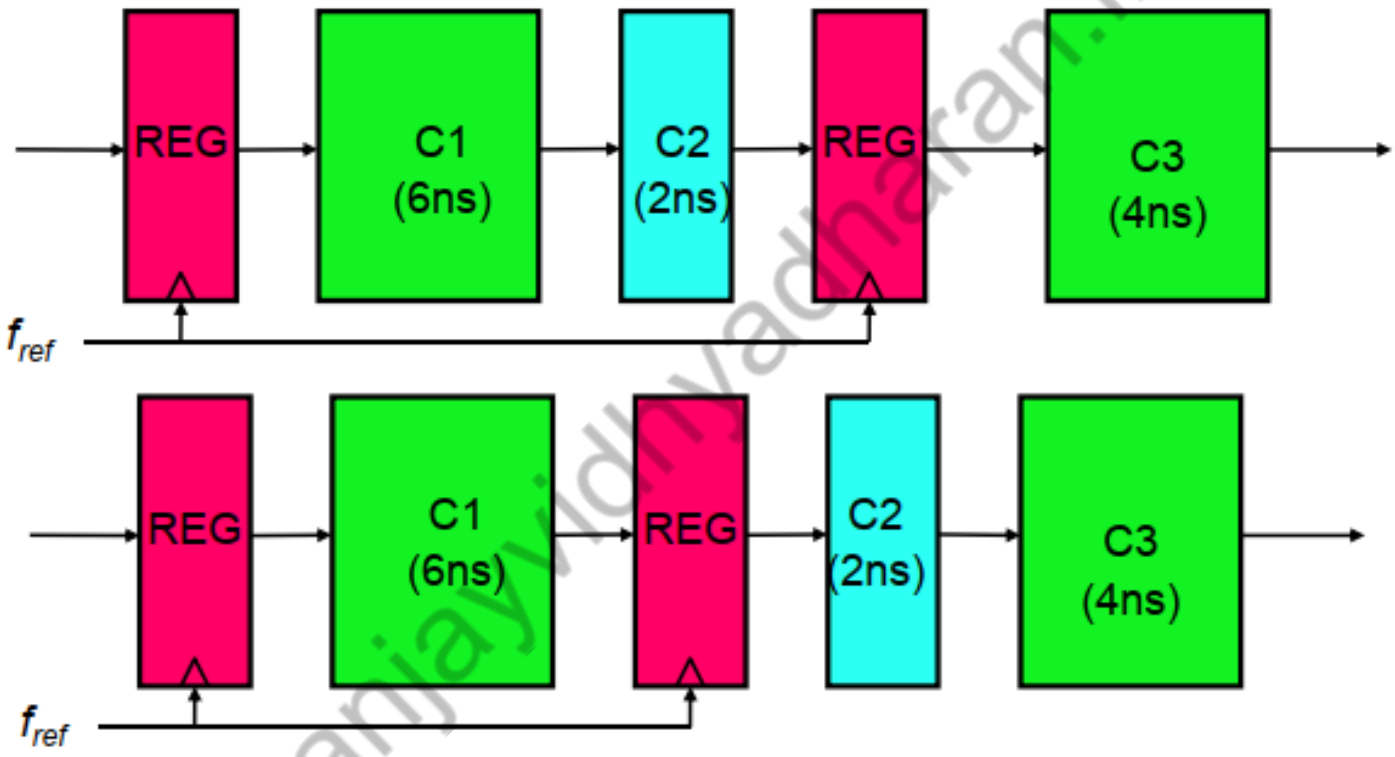
Architecture-Level Design – Pipelining



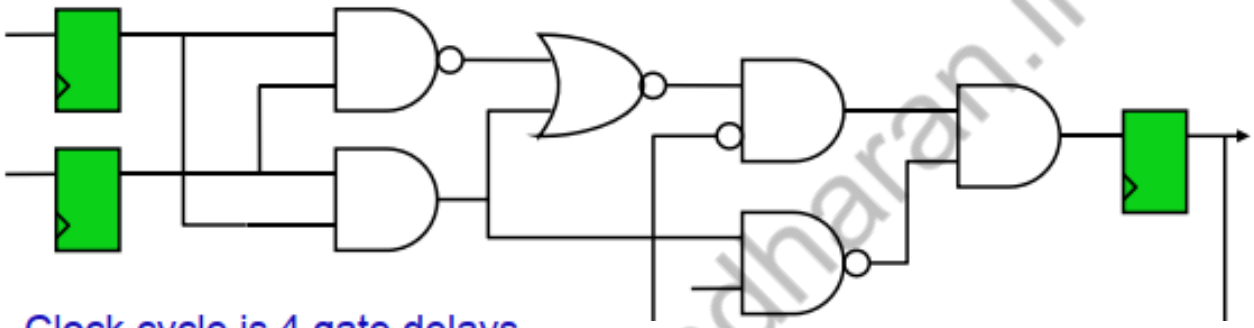


Performance Figure	Circuit (a)	Circuit (b)
Function Delay in ns	2 ns	2 ns
Throughput	@ 2ns	@ 1 ns

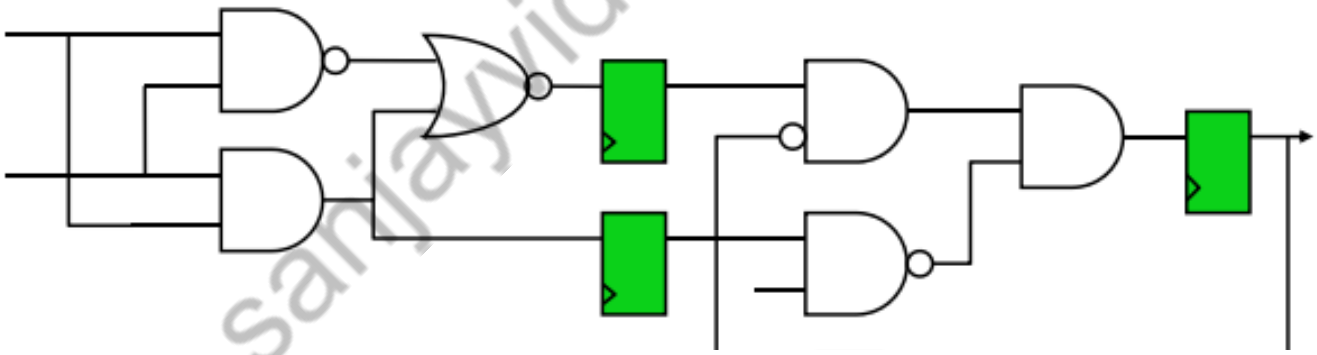
Architecture-Level Design – Retiming



Architecture-Level Design – Retiming



Clock cycle is 4 gate delays

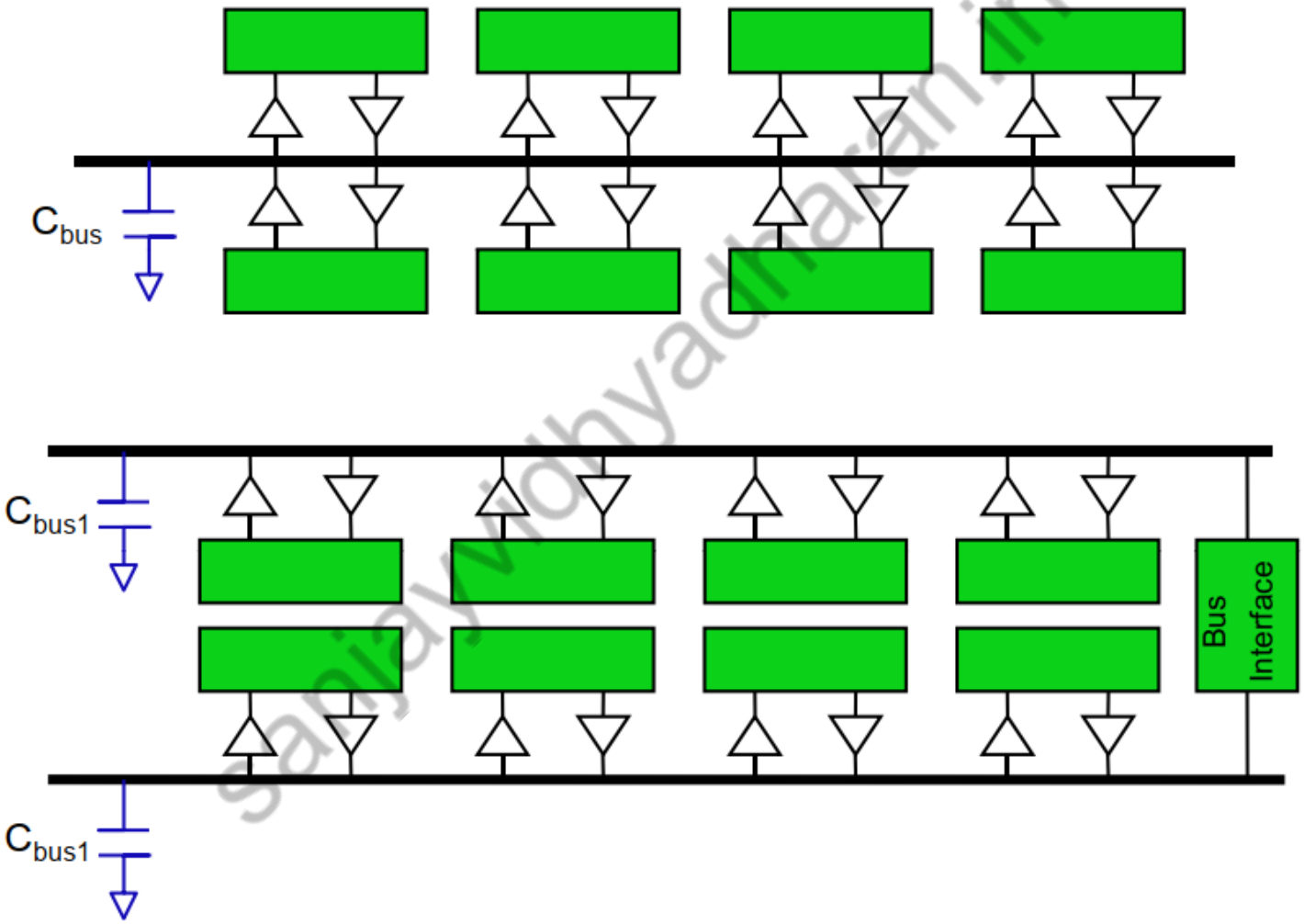


Clock cycle is 2 gate delays

Architecture-Level Design – Bus Segmentation

- Avoid the sharing of resources
  - Reduce the switched capacitance
- For example: a global system bus
  - A single shared bus is connected to all modules, this structure results in a large bus capacitance due to
    - The large number of drivers and receivers sharing the same bus
    - The parasitic capacitance of the long bus line
- A segmented bus structure
  - Switched capacitance during each bus access is significantly reduced
  - Overall routing area may be increased

Architecture-Level Design – Bus Segmentation



Algorithmic-Level Design – $f_{activity}$ Reduction

Binary Code	Gray Code	Decimal Equivalent
000	000	0
001	001	1
010	011	2
011	010	3
100	110	4
101	111	5
110	101	6
111	100	7

- Two-bit binary counter:

  State sequence, 00 → 01 → 10 → 11 → 00
  Six bit transitions in four clock cycles
  6/4 = 1.5 transitions per clock

- Two-bit Gray-code counter

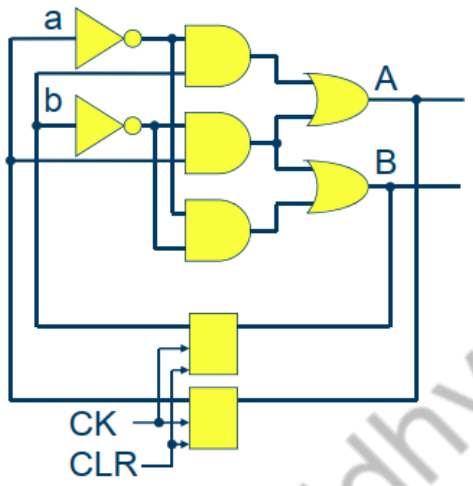
  State sequence, 00 → 01 → 11 → 10 → 00
  Four bit transitions in four clock cycles
  4/4 = 1.0 transitions per clock

Algorithmic-Level Design – $f_{activity}$ Reduction

Binary Counter

Present state		Next state	
a	b	A	B
0	0	0	1
0	1	1	0
1	0	1	1
1	1	0	0

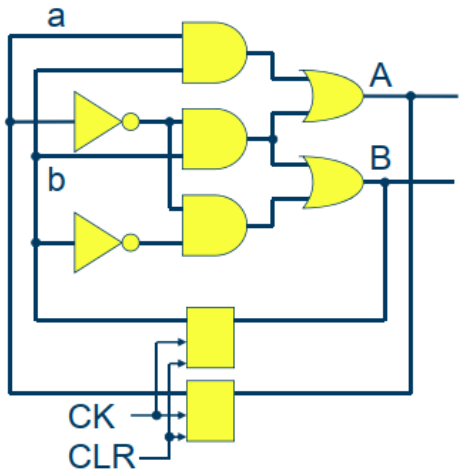
A = a'b + ab'
B = a'b' + ab'



Gray Counter

Present state		Next state	
a	b	A	B
0	0	0	1
0	1	1	1
1	0	0	0
1	1	1	0

A = a'b + ab
B = a'b' + a'b



Algorithmic-Level Design – $f_{activity}$ Reduction

Binary		Gray-code	
State	No. of toggles	State	No. of toggles
000	-	000	-
001	1	001	1
010	2	011	1
011	1	010	1
100	3	110	1
101	1	111	1
110	2	101	1
111	1	100	1
000	3	000	1
Av. Transitions/clock = 1.75		Av. Transitions/clock = 1	

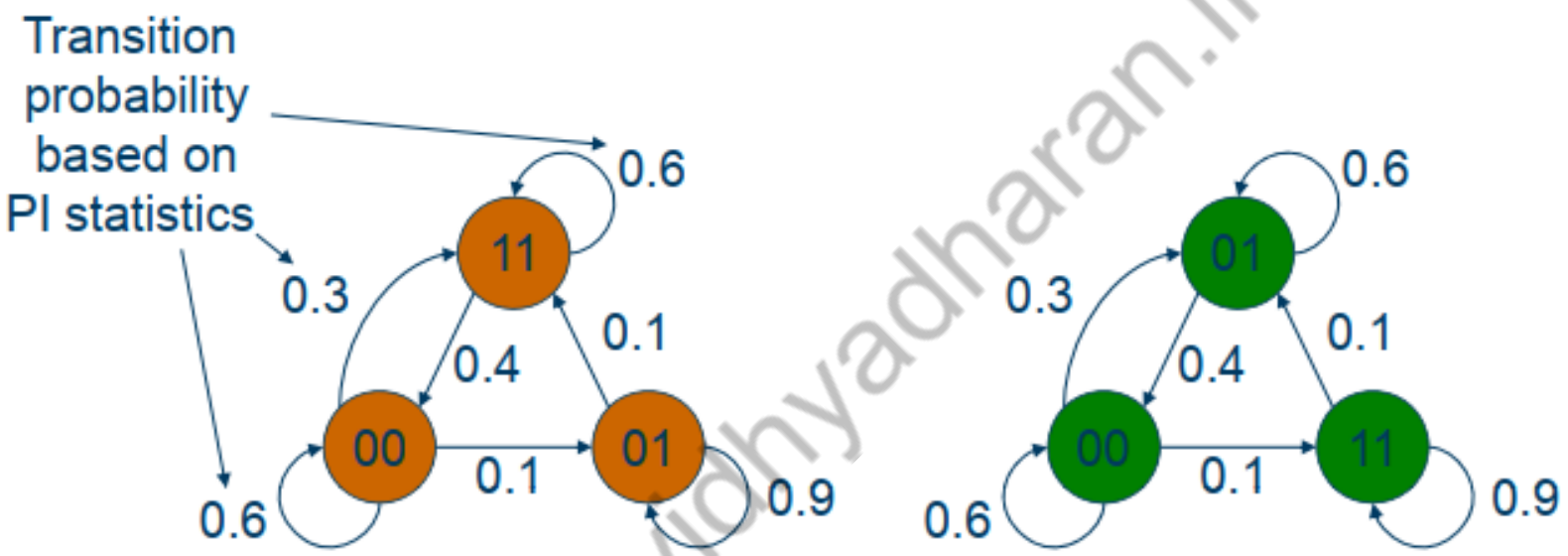
Algorithmic-Level Design – $f_{activity}$ Reduction

N-Bit Counter: Toggles in Counting Cycle

- Binary counter: $T(binary) = 2(2^N - 1)$
- Gray-code counter: $T(gray) = 2^N$
- $T(gray)/T(binary) = 2^{N-1}/(2^N - 1) \rightarrow 0.5$

Bits	T(binary)	T(gray)	T(gray)/T(binary)
1	2	2	1.0
2	6	4	0.6667
3	14	8	0.5714
4	30	16	0.5333
5	62	32	0.5161
6	126	64	0.5079
∞	-	-	0.5000

FSM State Encoding



Expected number of state-bit transitions:

2(0.3+0.4) + 1(0.1+0.1) = 1.6

1(0.3+0.4+0.1) + 2(0.1) = 1.0

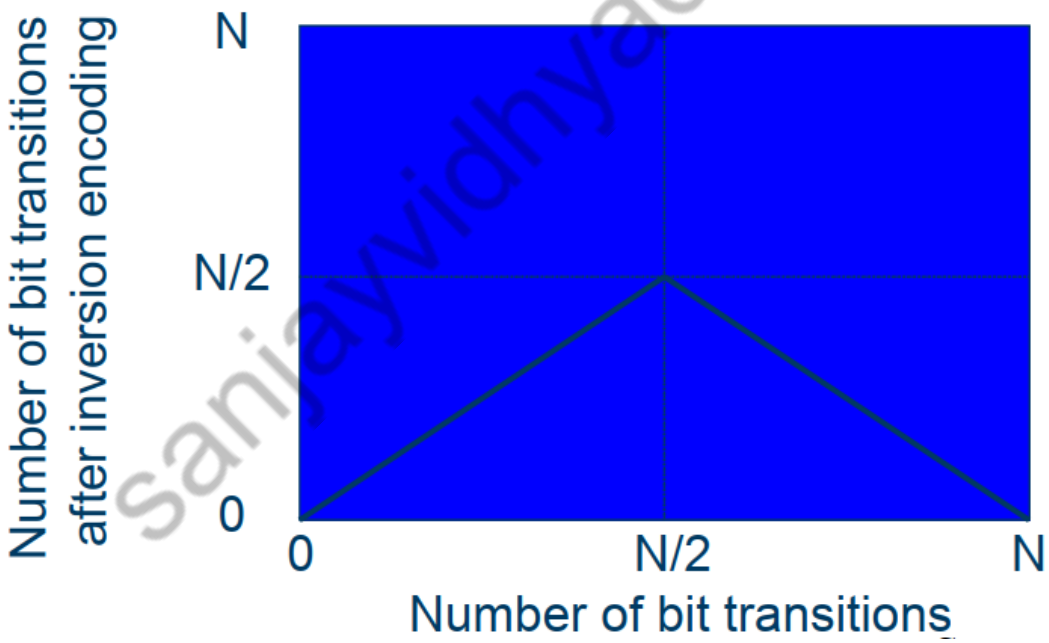
State encoding can be selected using a power-based cost function.

Bus Encoding for Reduced Power

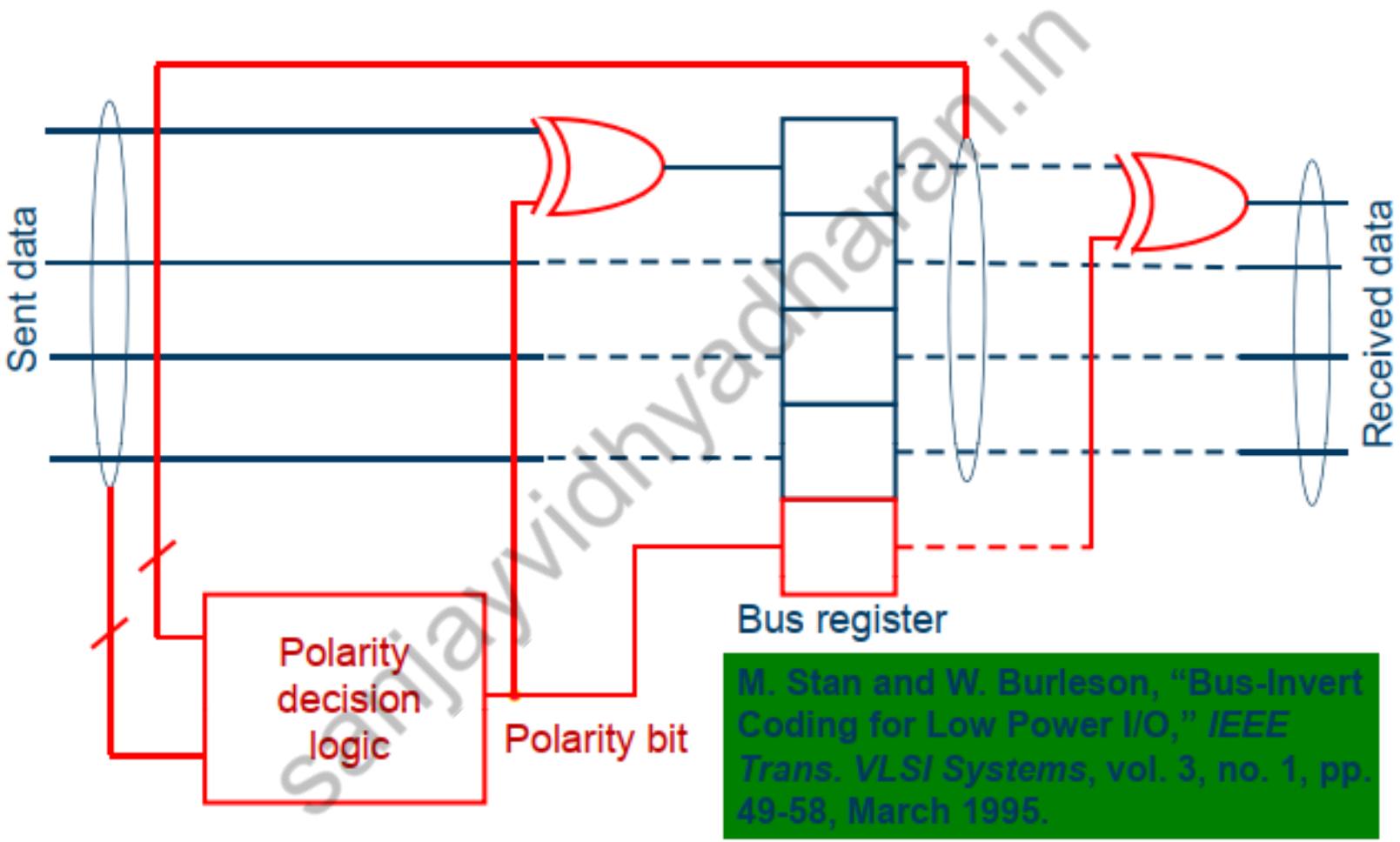
- Example: Four bit bus

  0000 → 1110 has three transitions.
  If bits of second pattern are inverted then 0000 ,
  then 0000 → 0001 will have only one transition.

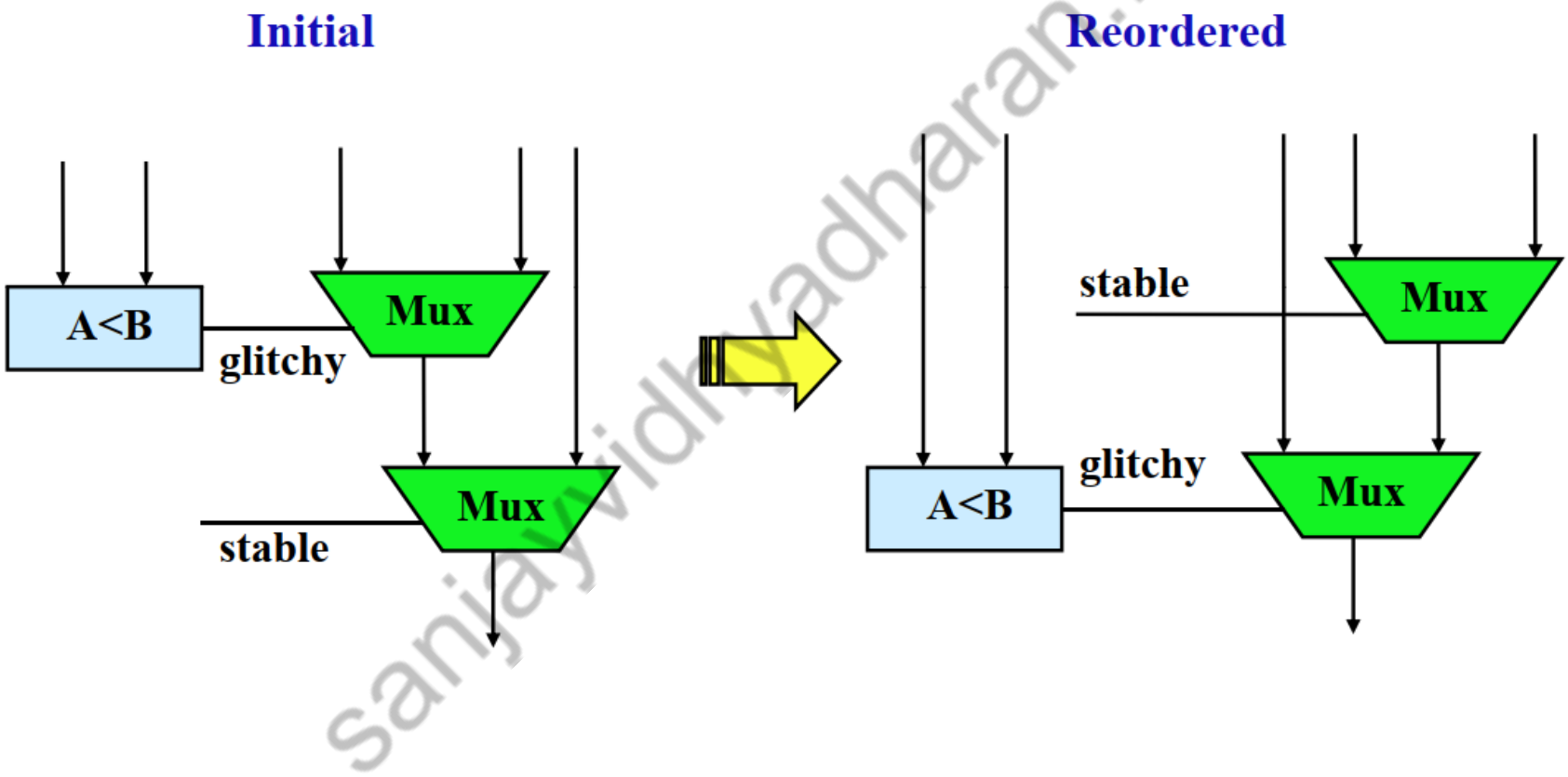
- Bit-inversion encoding for N-bit bus



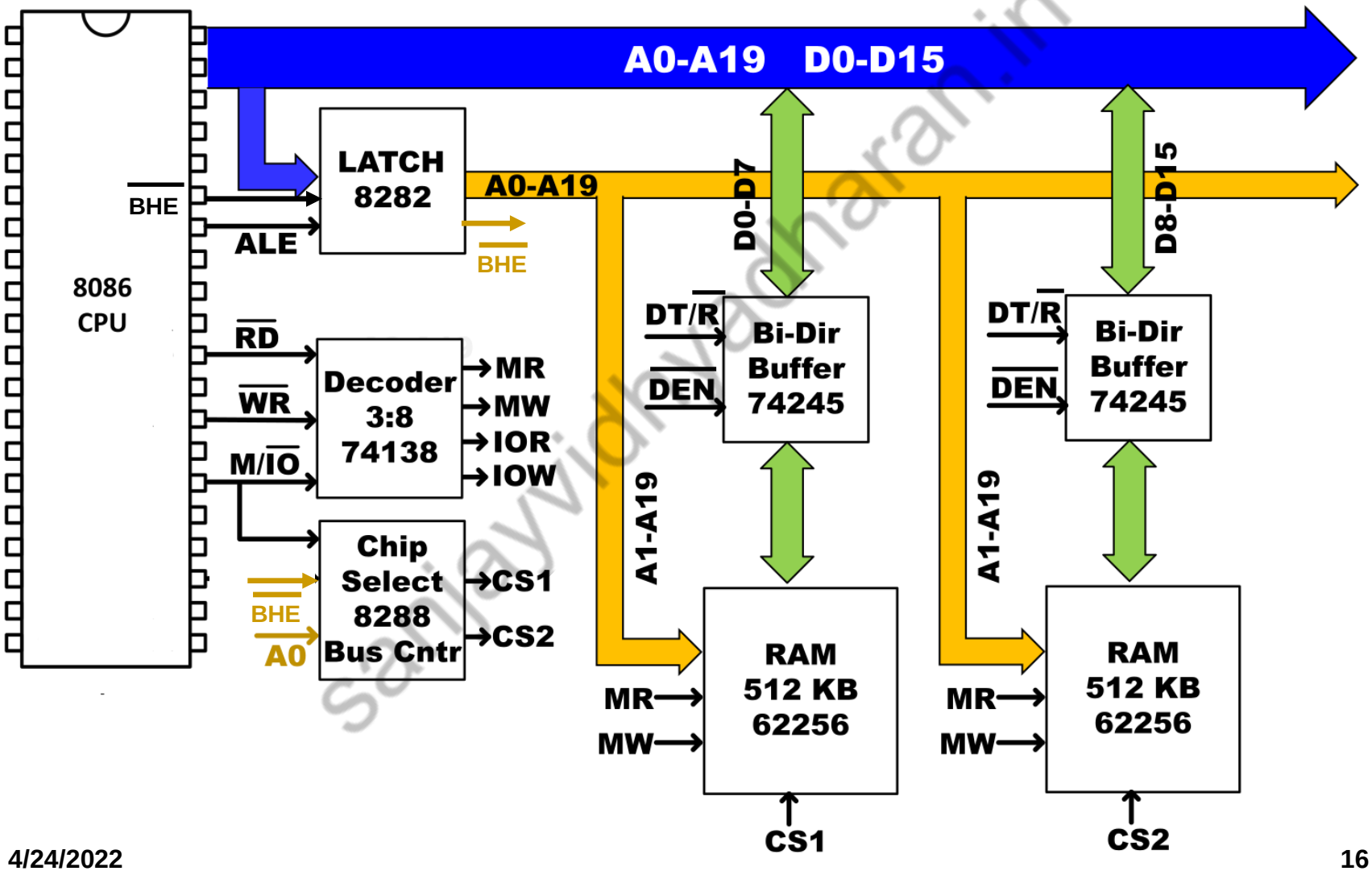
Bus Encoding for Reduced Power



RTL-Level Design – Datapath Reordering

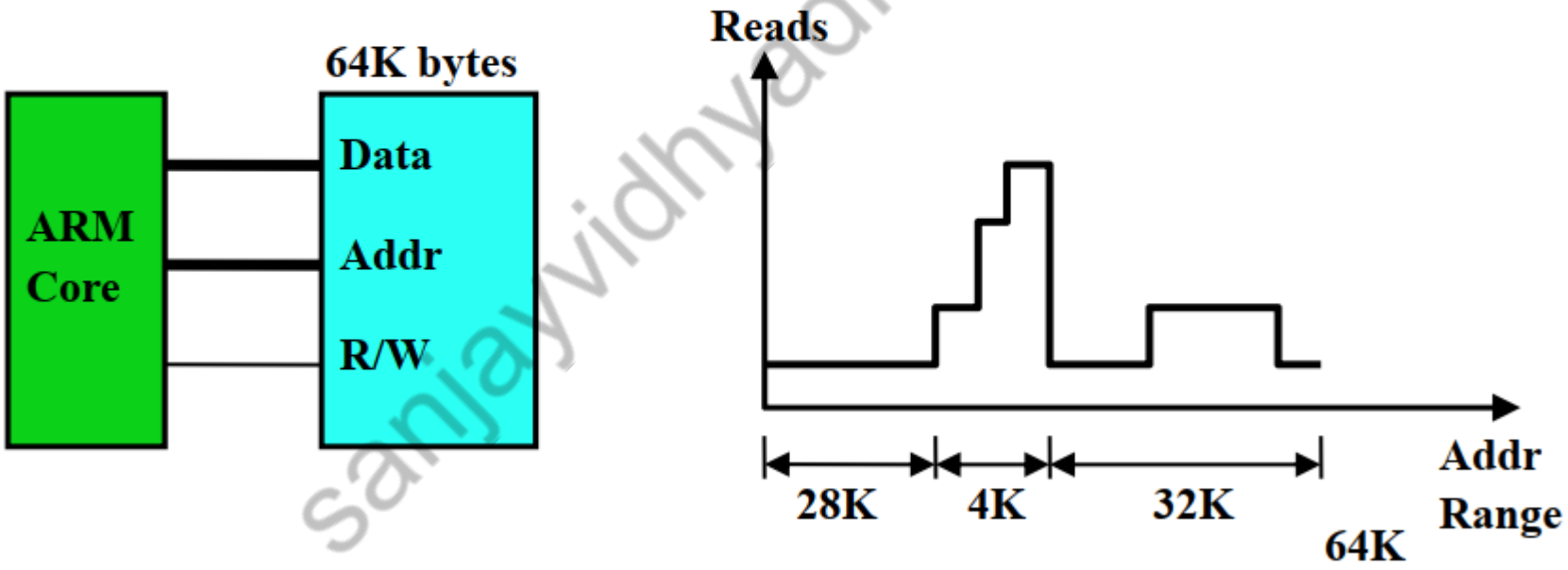


RTL-Level Design – Memory Partition



RTL-Level Design – Memory Partition

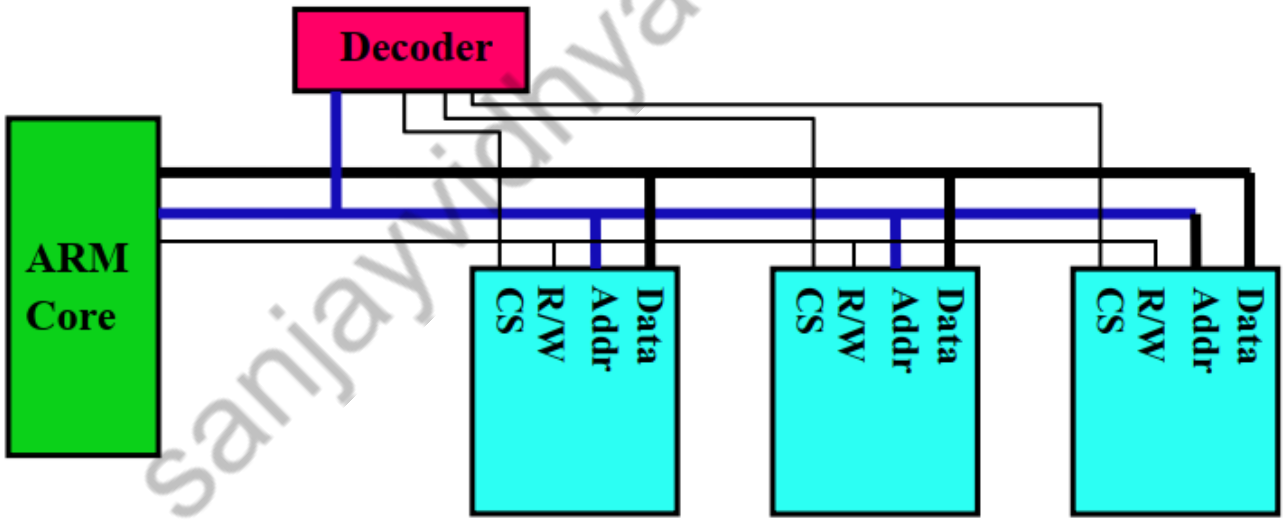
- Application-driven memory partition



RTL-Level Design – Memory Partition

RTL-Level Design – *Memory Partition*

- A power-optimal partitioned memory organization



Thank you