Advanced VLSI Design: 2021-22
Lecture 12-A: Low Power VLSI Design
Part-1: Gate Level Optimization

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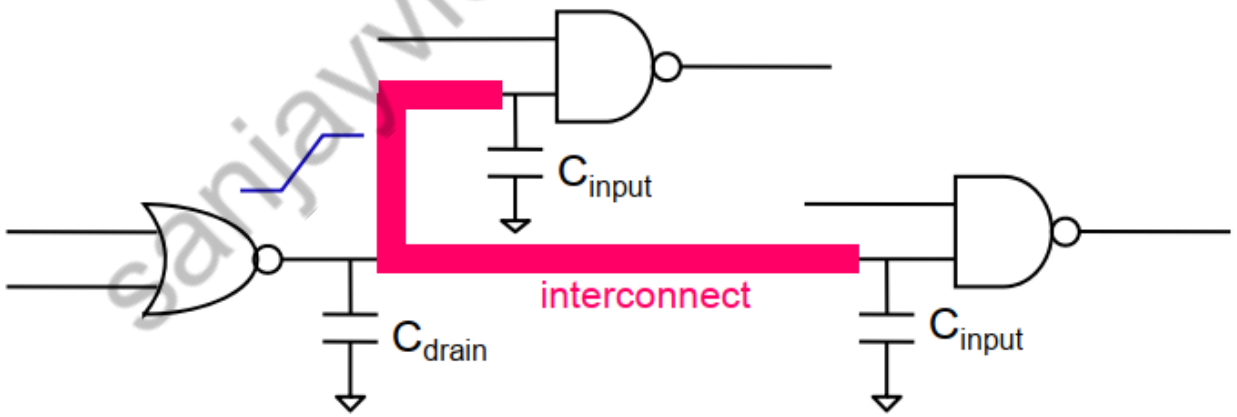
Overview of Power Consumption

- Average power consumption
  - Dynamic power consumption
  - Short-circuit power consumption
  - Leakage power consumption
  - Static power consumption
- Dynamic power dissipation during switching



Overview of Power Consumption

- The average power consumption can be expressed as

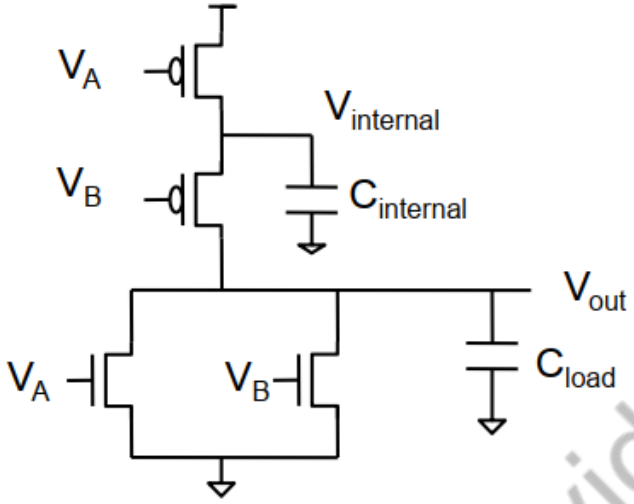
$$P_{avg} = \frac{1}{T} C_{load} V_{DD}^2 = C_{load} V_{DD}^2 f_{CLK}$$

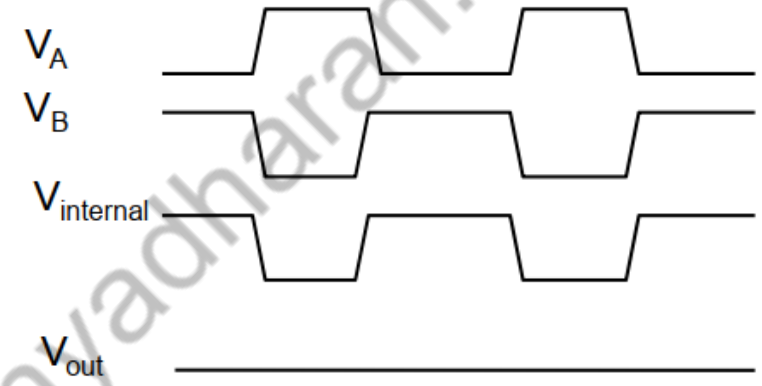
- The node transition rate can be slower than the clock rate. To better represent this behavior, a node transition factor (α_T) should be introduced

$$P_{avg} = \alpha_T C_{load} V_{DD}^2 f_{CLK}$$

- The switching power expressed above are derived by taking into account the output node load capacitance

Overview of Power Consumption





The generalized expression for the average power dissipation can be rewritten as

$$P_{avg} = \left(\sum_{i=1}^{\#ofnodes} \alpha_{Ti} C_i V_i \right) V_{DD} f_{CLK}$$

Transition Activity

- Switching activity, $P_{0\rightarrow1}$, has two components
  - A static component – function of the logic topology
  - A dynamic component – function of the timing behavior (glitching)

2-input NOR Gate

A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

Static transition probability

$$P_{0\rightarrow1} = P_{out=0} \times P_{out=1}$$
$$= P_0 \times (1-P_0)$$

With input signal probabilities

$P_{A=1} = 1/2$

$P_{B=1} = 1/2$

NOR static transition probability

$= 3/4 \times 1/4 = 3/16$

Transition Activity

A	B	Out
0	0	0
0	1	1
1	0	1
1	1	0

Assume signal probabilities

$p_{A=1} = 1/2$

$p_{B=1} = 1/2$

Then transition probability

$p_{0\to1} = p_{Out=0} \times p_{Out=1}$

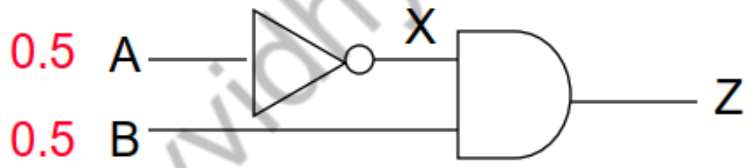
$= 1/2 \times 1/2 = 1/4$

If inputs switch in every cycle

$P_{0\to1} = 1/4$

Transition Activity

	$P_{0\rightarrow1} = P_{out=0} \times P_{out=1}$
NOR	$(1 - (1 - P_A)(1 - P_B)) \times (1 - P_A)(1 - P_B)$
OR	$(1 - P_A)(1 - P_B) \times (1 - (1 - P_A)(1 - P_B))$
NAND	$P_A P_B \times (1 - P_A P_B)$
AND	$(1 - P_A P_B) \times P_A P_B$
XOR	$(1 - (P_A + P_B - 2P_A P_B)) \times (P_A + P_B - 2P_A P_B)$



For X: $P_{0\rightarrow1} = P_0 \times P_1 = (1-P_A)\,P_A$

$= 0.5 \times 0.5 = 0.25$

For Z: $P_{0\rightarrow1} = P_0 \times P_1 = (1-P_X P_B)\,P_X P_B$

$= (1 - (0.5 \times 0.5)) \times (0.5 \times 0.5) = 3/16$

Transition Activity

- Low-Power Gate-Level Design
- Low-Power Architecture-Level Design
- Algorithmic-Level Power Reduction
- RTL Techniques for Optimizing Power

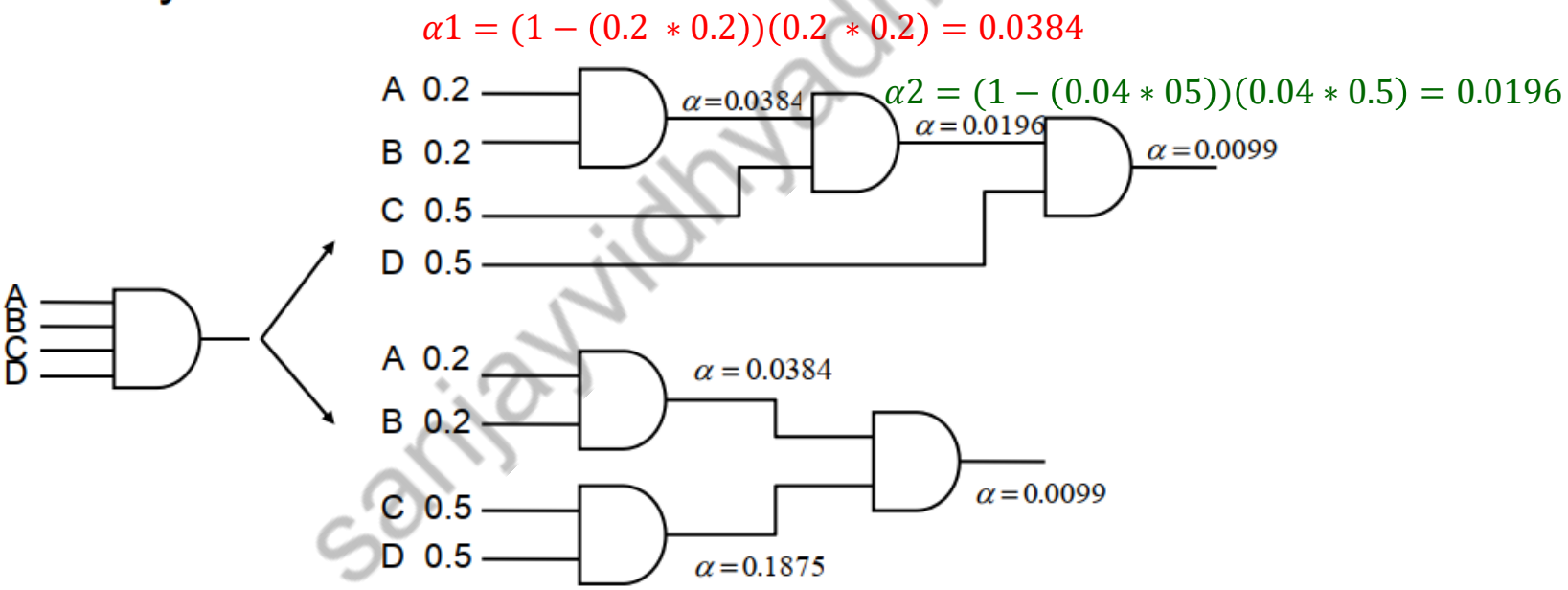
Gate-Level Design – Technology Mapping

- The objective of logic minimization is to reduce the boolean function.
- For low-power design, the signal switching activity is minimized by restructuring a logic circuit
- The power minimization is constrained by the delay, however, the area may increase.
- During this phase of logic minimization, the function to be minimized is

$$\sum_i P_i (1 - P_i) C_i$$

Gate-Level Design – Technology Mapping

- The first step in technology mapping is to decompose each logic function into two-input gates
- The objective of this decomposition is to minimizing the total power dissipation by reducing the total switching activity



Gate-Level Design – Technology Mapping

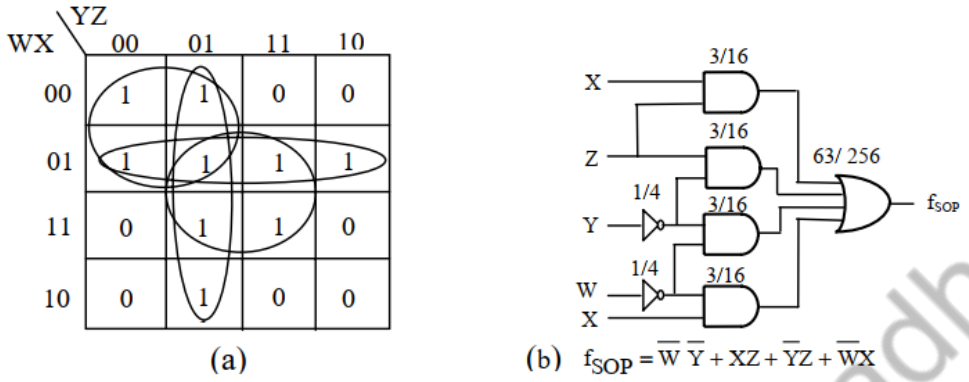
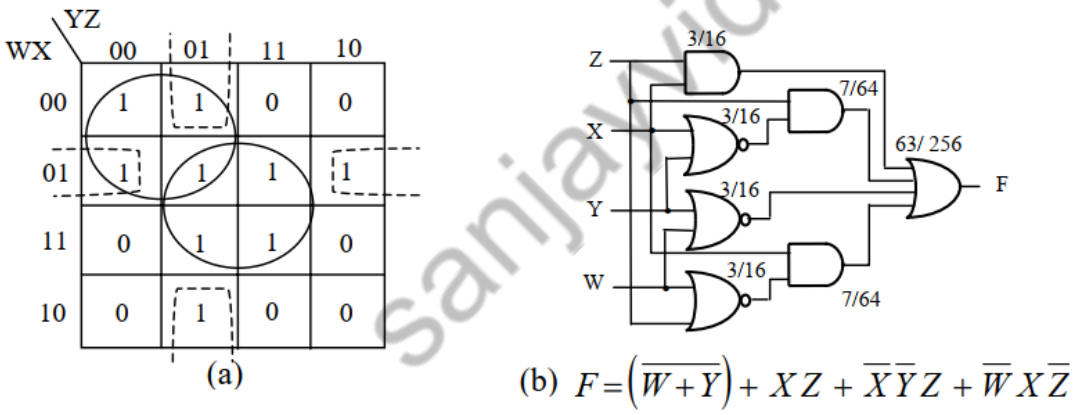
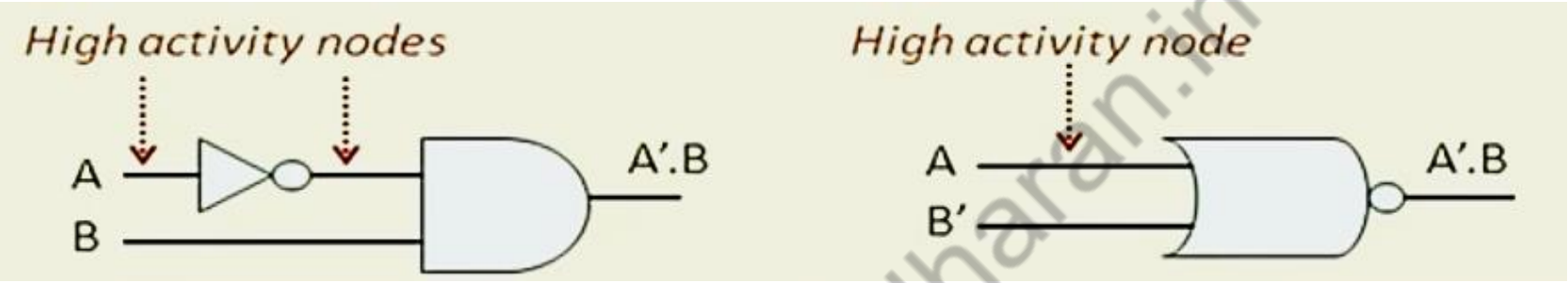


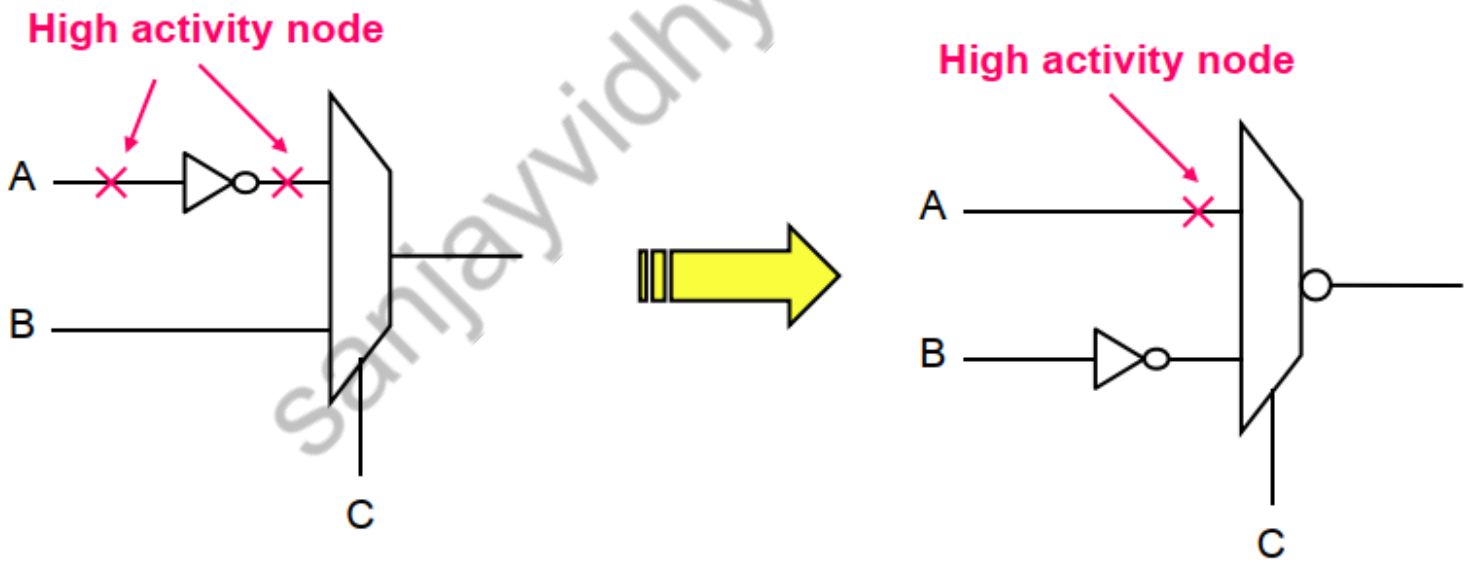
Figure 2. Minimal sum-of-products implementation for Example 3



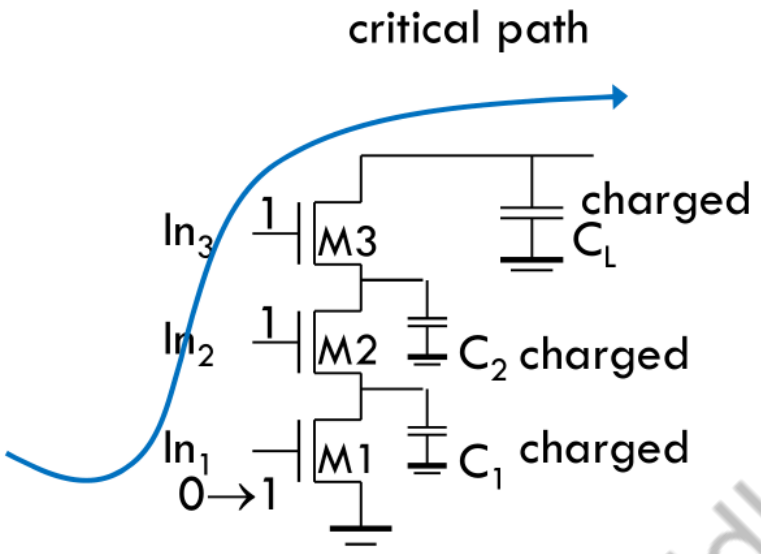
Switching Activity Minimization in Combinational Logic Design
R. V. Menon, S. Chennupati, N. K. Samala, D. Radhakrishnan and B. Izadi

Gate-Level Design – Phase Assignment

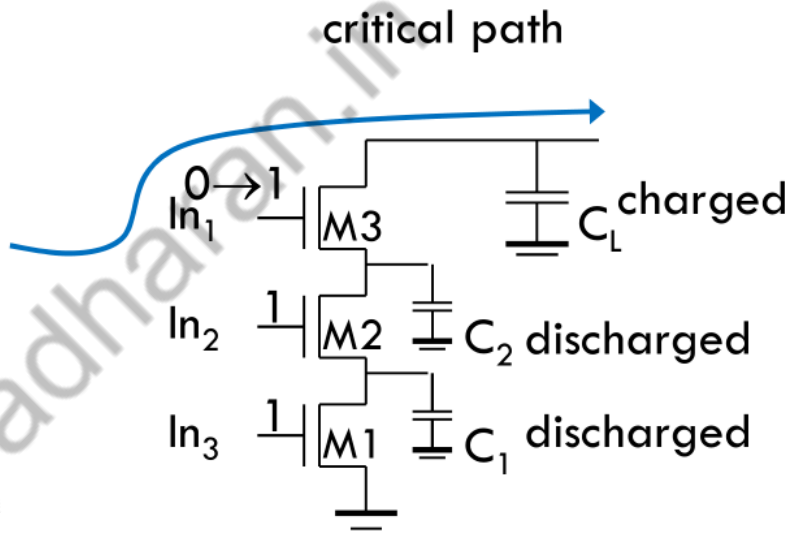




Gate-Level Design – Pin Swapping



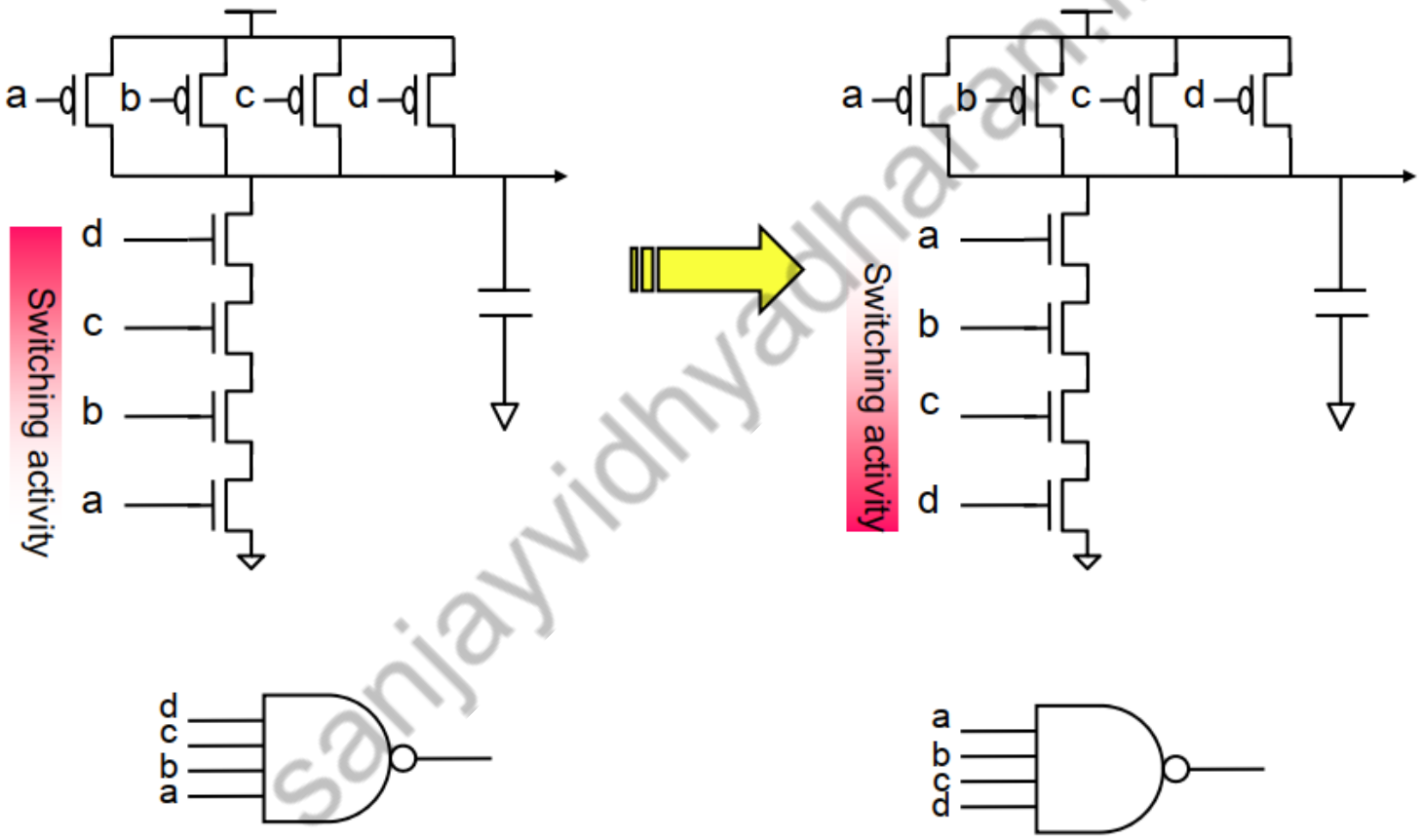
delay determined by time to discharge C_L, C_1 and C_2



delay determined by time to discharge C_L

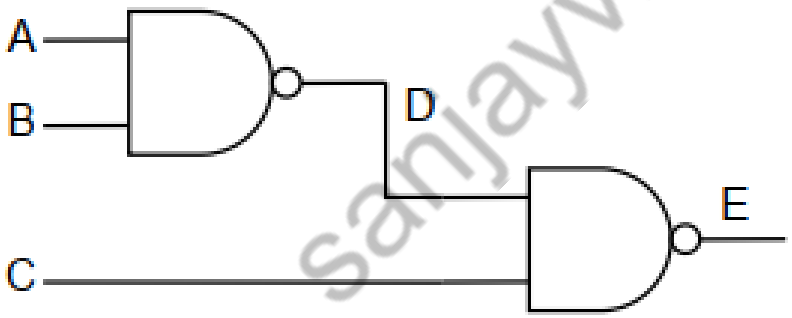
- An input signal to a gate is called critical if it is the last signal of all inputs to assume a stable value.
- The path through the logic which determines the ultimate speed of the structure is called the critical path.
- Putting the critical-path transistors closer to the output of the gate can result in a speed-up.

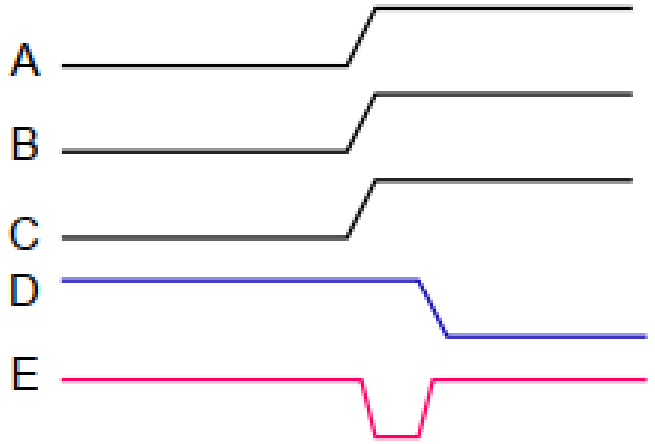
Gate-Level Design – Pin Swapping



Gate-Level Design – Glitching Power

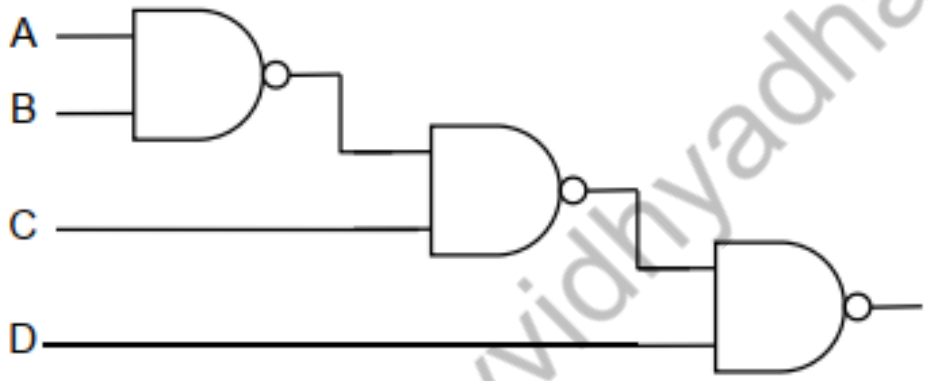
- Glitches
  - spurious transitions due to imbalanced path delays
- A design has more balanced delay paths
  - has fewer glitches, and thus has less power dissipation
- Note that there will be no glitches in a dynamic CMOS logic



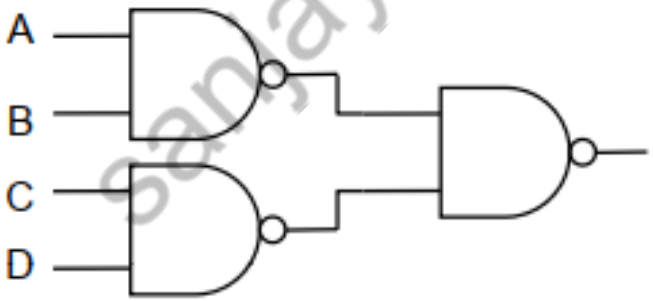


Gate-Level Design – Glitching Power

- A chain structure has more glitches
- A tree structure has fewer glitches



Chain structure



Tree structure

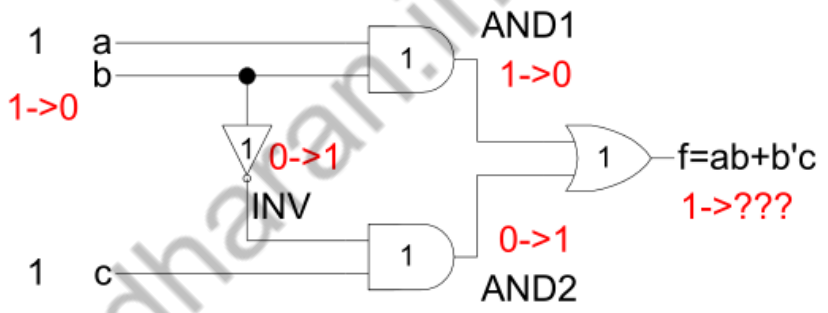
Static Glitch Example

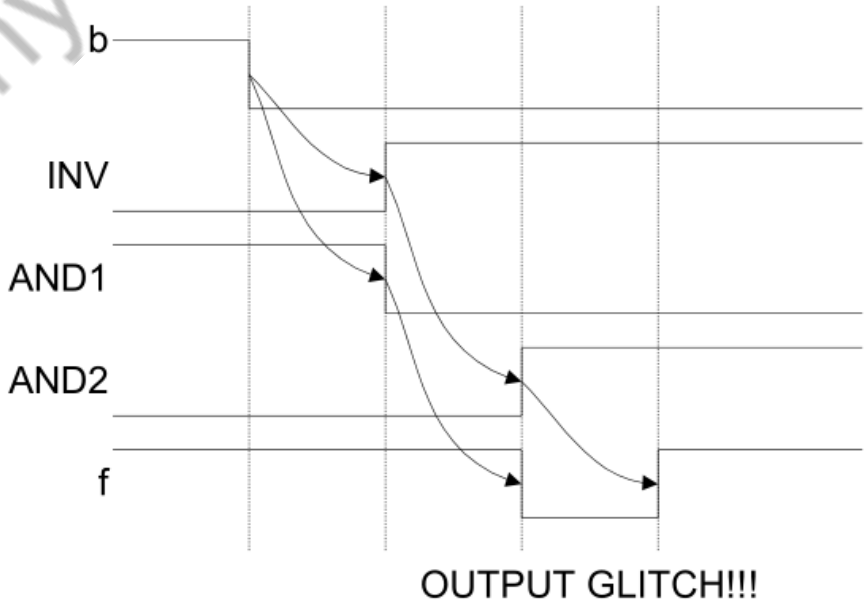
Consider the following circuit with delays where only one input (input b) changes…

Draw a timing diagram to see what happens at output with delays.

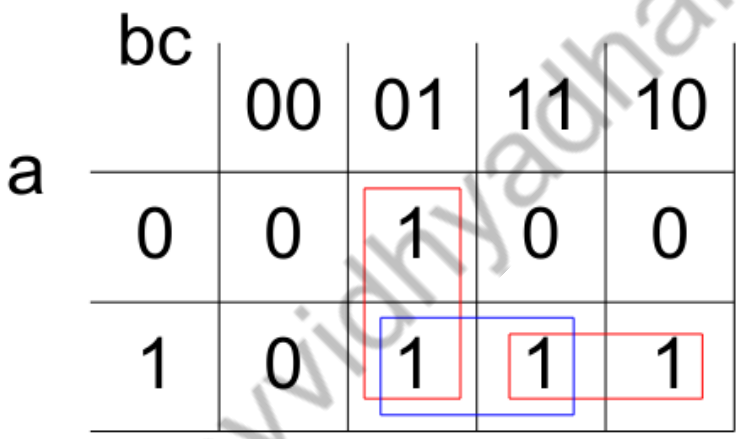
From the logic expression, we see that b changing should result in the output remaining at logic level 1…

Due to delay, the output goes 1->0->1 and this is an output glitch; **we see a static-1 hazard.**





Static Glitch Elimination



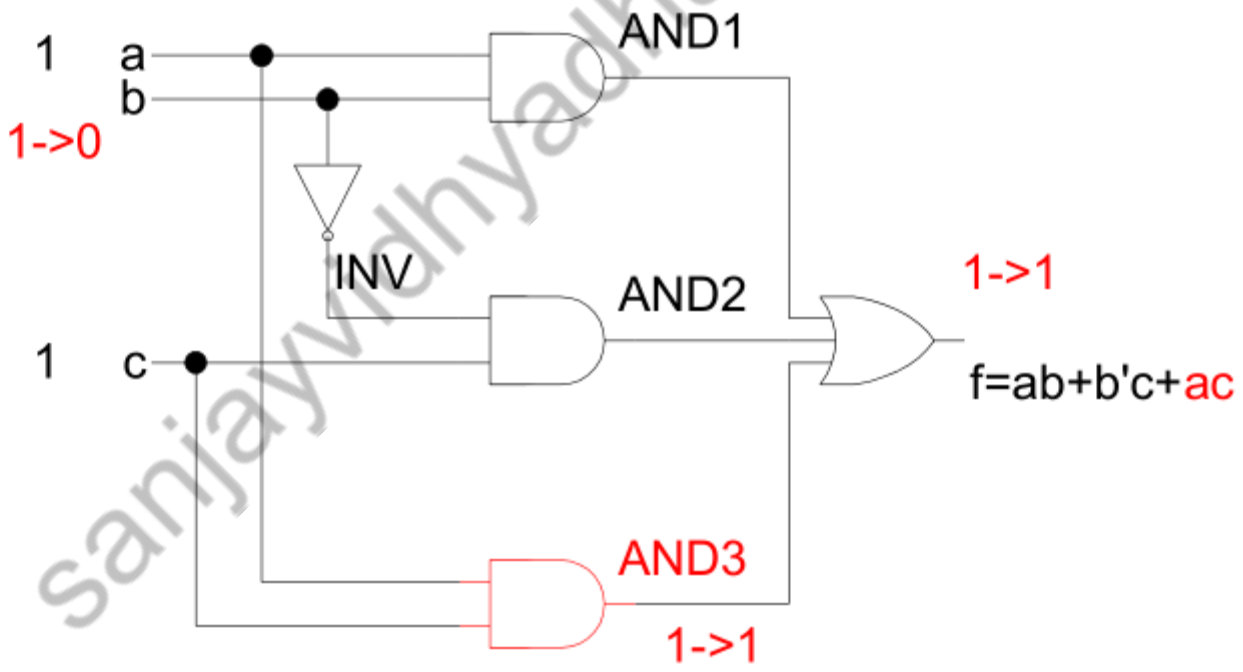
a \ bc	00	01	11	10
0	0	1	0	0
1	0	1	1	1

f=ab+b'c + ac

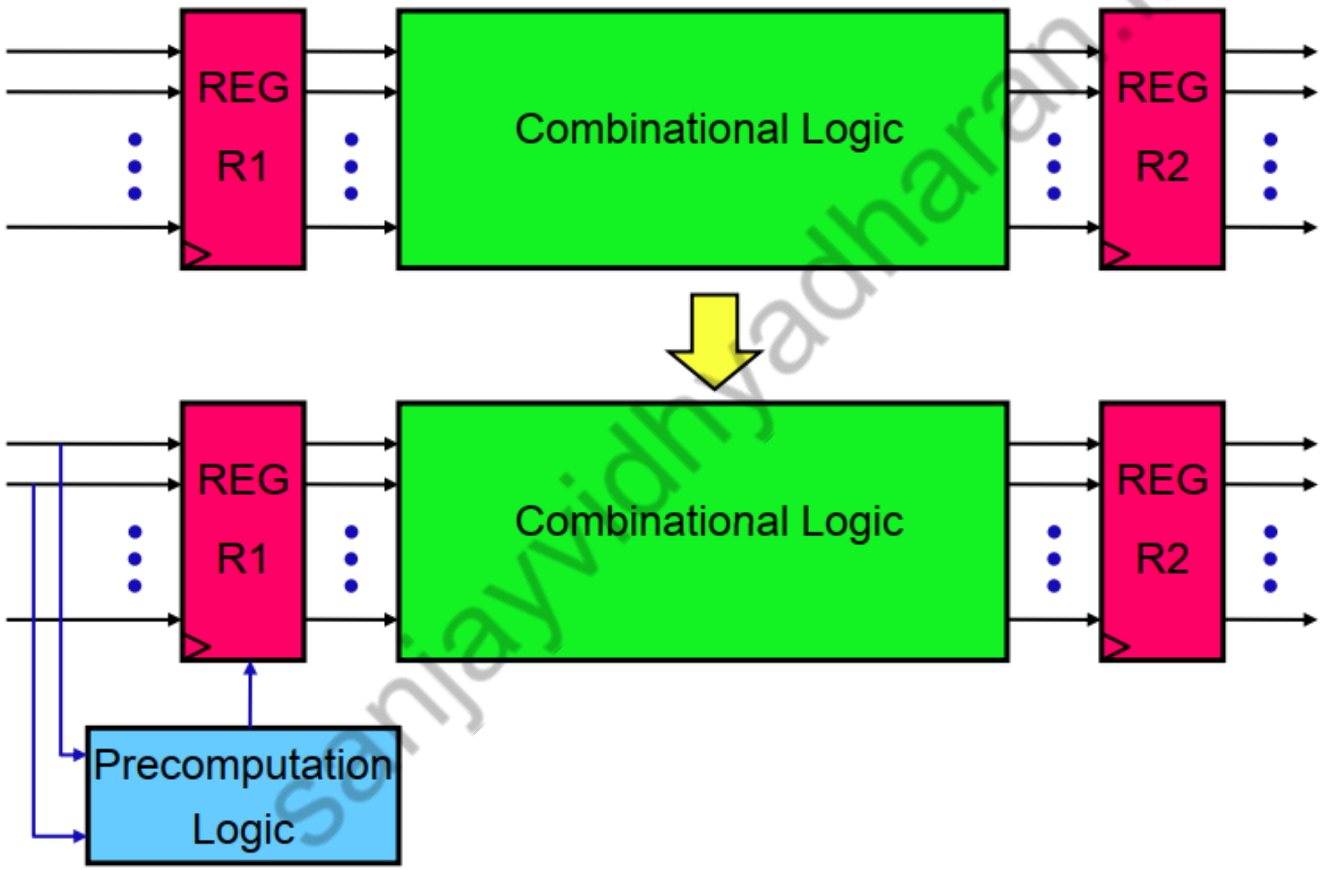
The extra product term does not include the changing input variable, and therefore serves to prevent possible momentary output glitches due to this variable.

Static Glitch Elimination

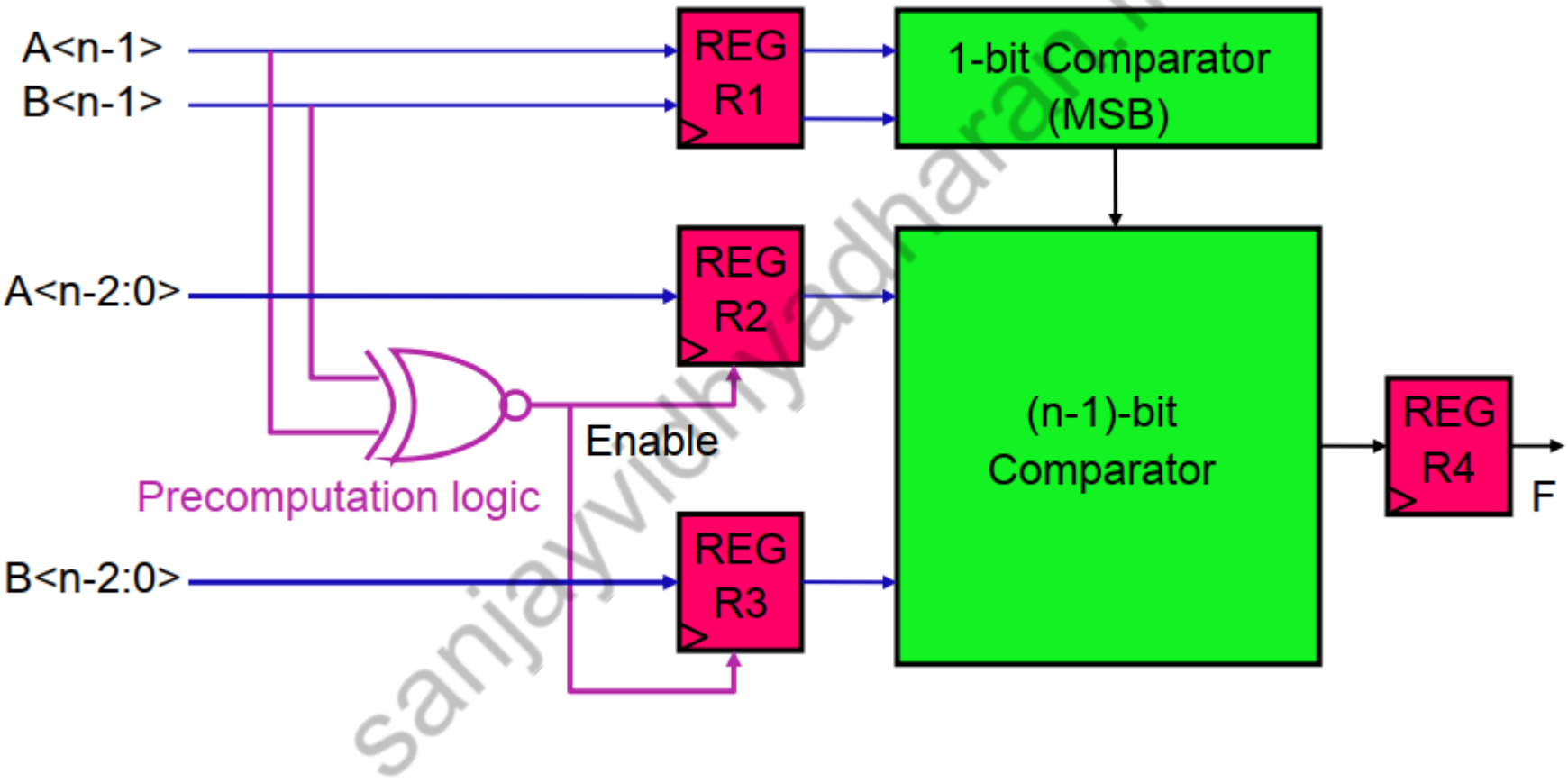
The redundant product term is not influenced by the changing input.



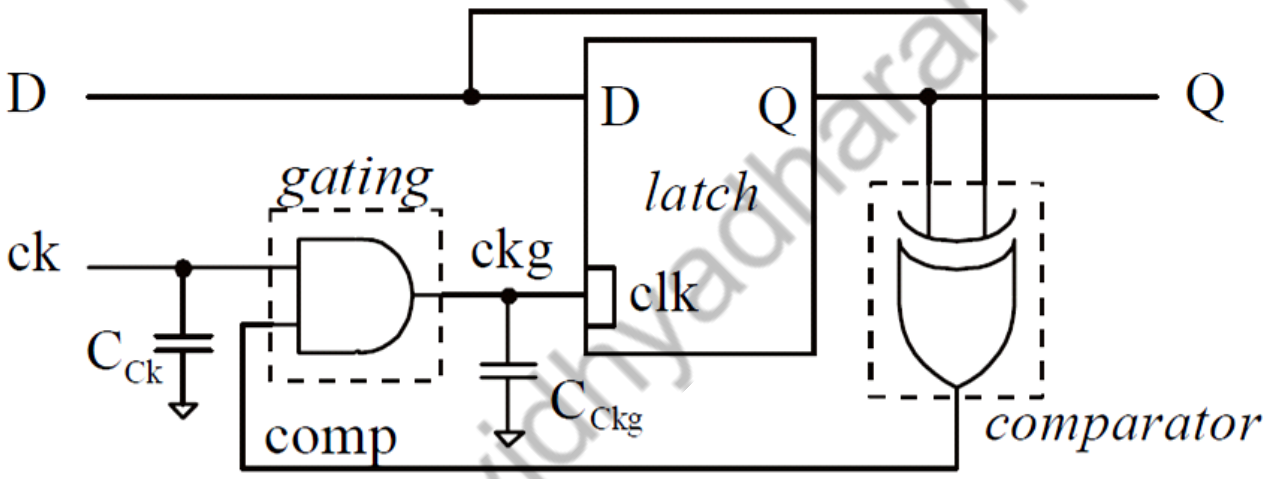
Gate-Level Design – Precomputation



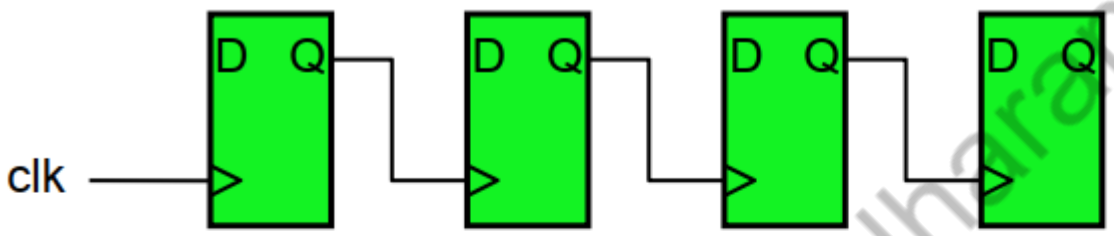
Gate-Level Design – Precomputation



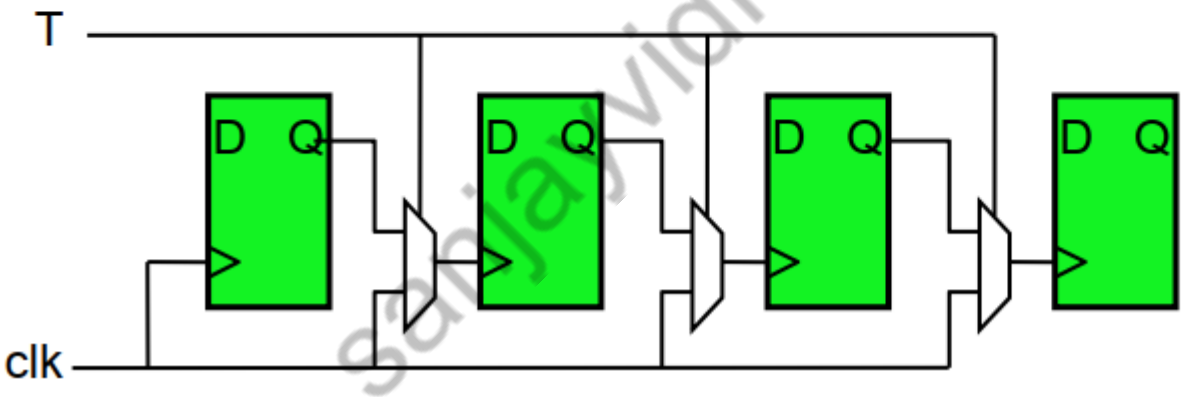
Gate-Level Design – Clock Gating



Gate-Level Design – Clock Gating

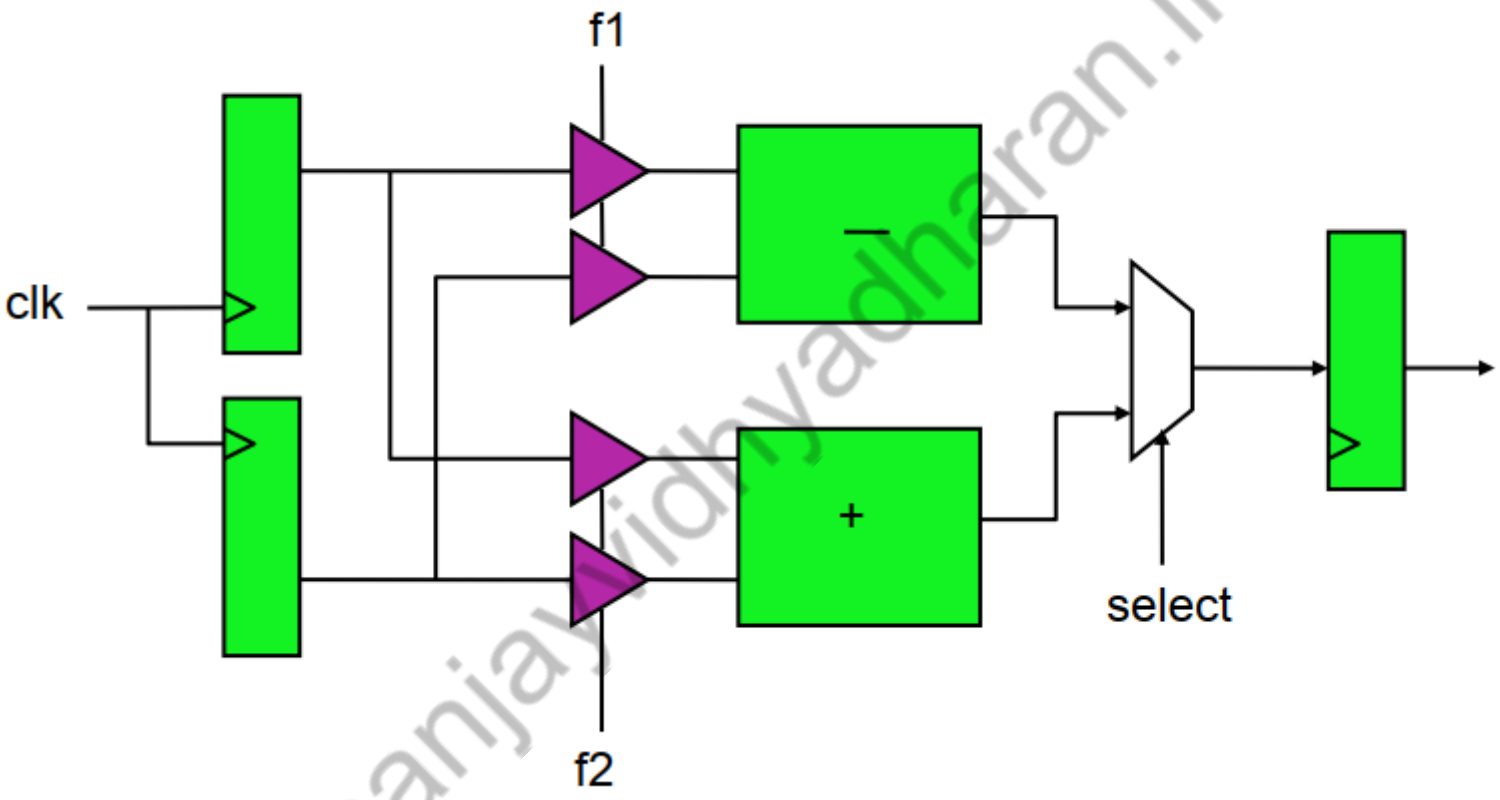


Fail DFT rule checking

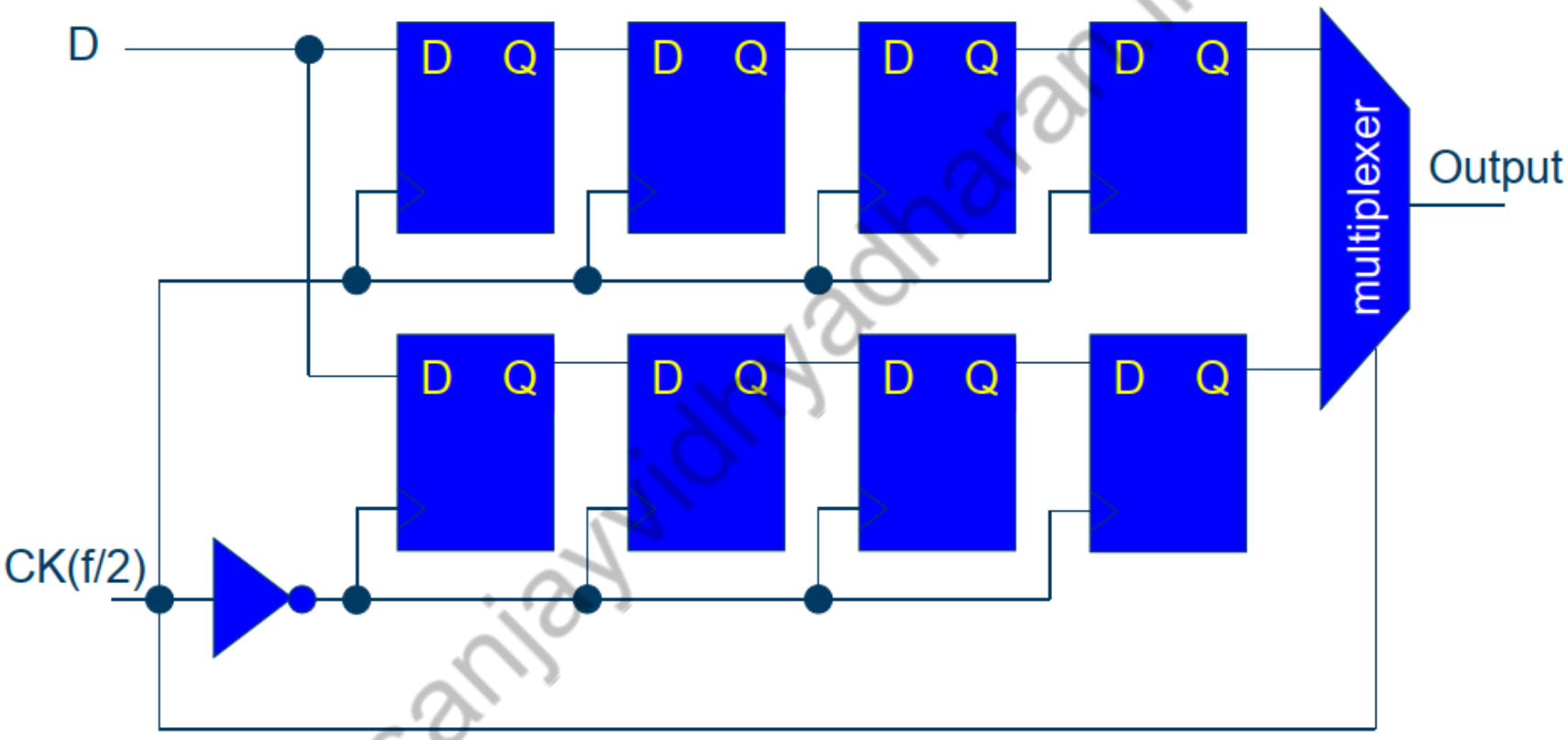


Add control pin to solve DFT violation problem

Gate-Level Design – Input Gating



Reduced-Power Shift Register



Flip-flops are operated at full voltage and half the clock frequency.

Thank you