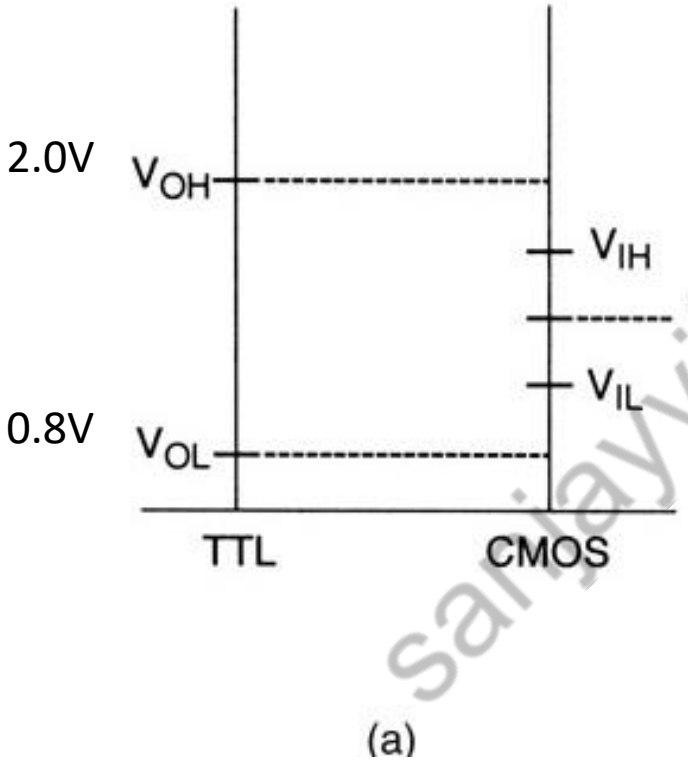
Advanced VLSI Design: 2021-22
Lecture 8
Interfacing Circuits – Part-3
Level Shifters and IO PADS

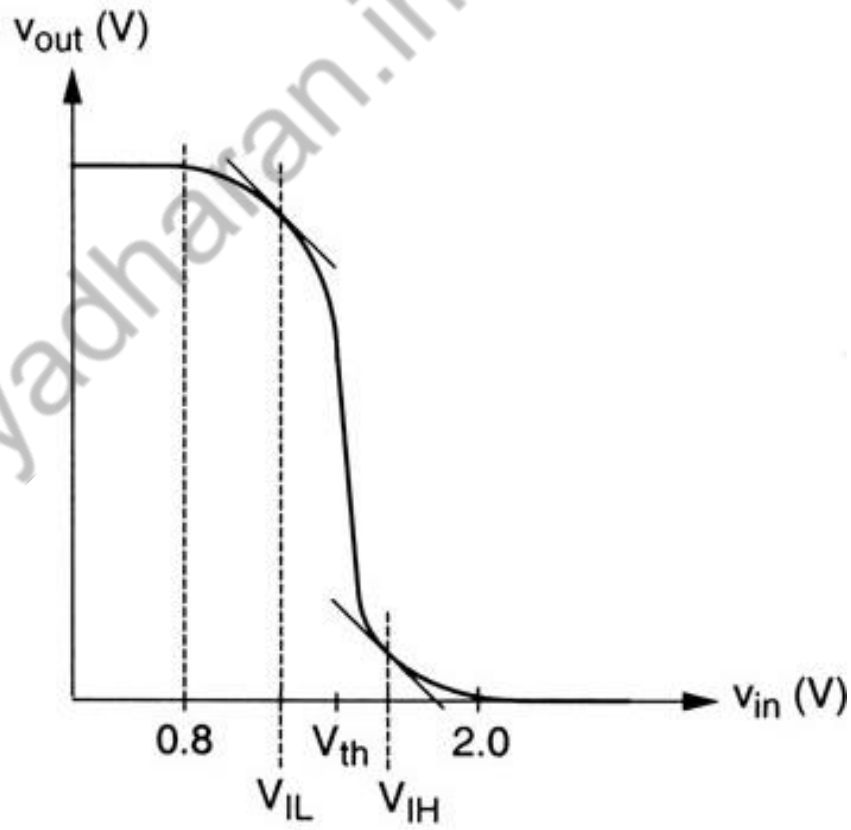
By Dr. Sanjay Vidhyadharan

TTL to CMOS Level Shifter



(a)

Voltage level of TTL and CMOS

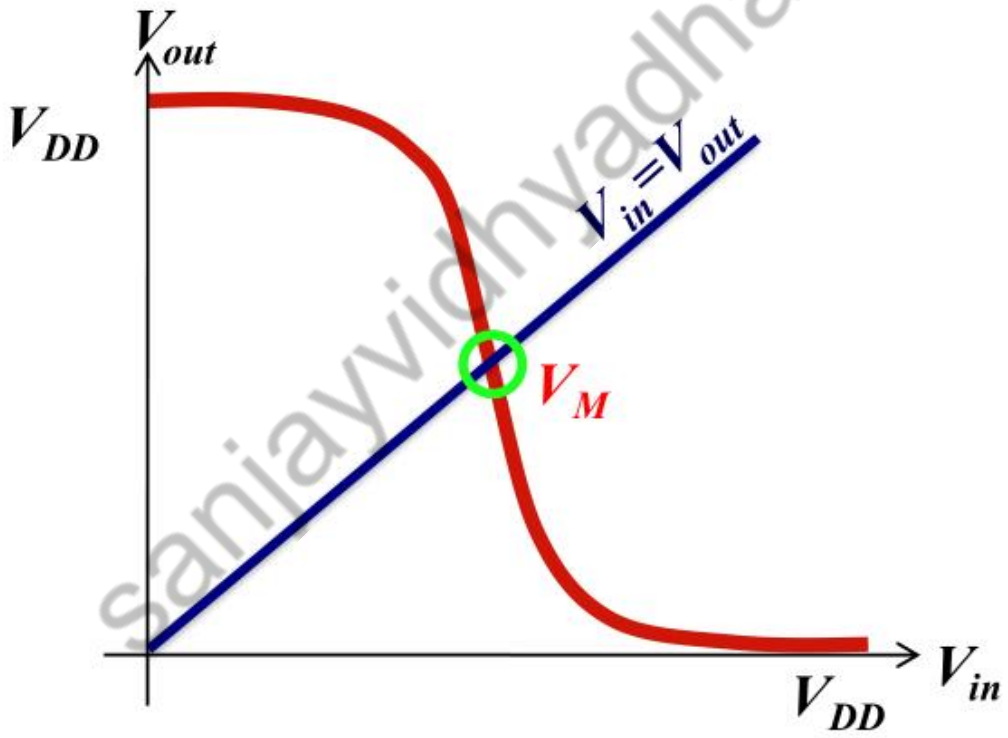


(b)

The corresponding VTC

CMOS Inverter Switching Threshold

The Switching Threshold, V_M , is the point where $V_{in} = V_{out}$.
This can be calculated:
» Graphically, at the intersection of the VTC with $V_{in} = V_{out}$



TTL to CMOS Level Shifter

Designing the Receiving Inverter Gate

- Adjust the TR ratio such that the Inverter Threshold V_M is midpoint between 0.8V and 2.0V
  - Let's analytically compute V_M.
    - Remember, the saturation current for a MOSFET is given

$$I_{DS} = \frac{k}{2}\left(V_{GS} - V_T\right)^2\left(1 + \lambda V_{DS}\right)$$

    - Lets assume $\lambda = 0$ and we'll equate the two currents:

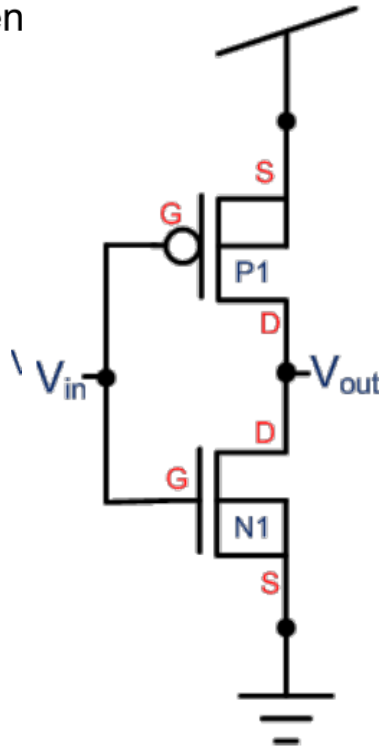
$$I_D = \frac{k_n}{2}\left(V_{GSn} - V_{Tn}\right)^2 = \frac{k_p}{2}\left(V_{SGp} - V_{Tp}\right)^2$$

    - Now we'll substitute:

$$V_{GSn} = V_{in} = V_M \qquad V_{SGp} = V_{DD} - V_{in} = V_{DD} - V_M$$

    - And we'll arrive at:

$$V_M = \frac{V_{Tn} + r\left(V_{DD} - V_{Tp}\right)}{1 + r} \qquad r \triangleq \sqrt{\frac{k_p}{k_n}}$$



TTL to CMOS Level Shifter

$$V_M = \frac{V_{DD}+V_{Tp}+rV_{Tn}}{1+r}$$

$$For\ V_{DD} = 5\ V\ and\ \ V_M = \frac{0.8+2}{2} = 1.4\ V\ ,\ VTn = 1\ V,\ \ and\ V_{Tpn} = -1\ V$$

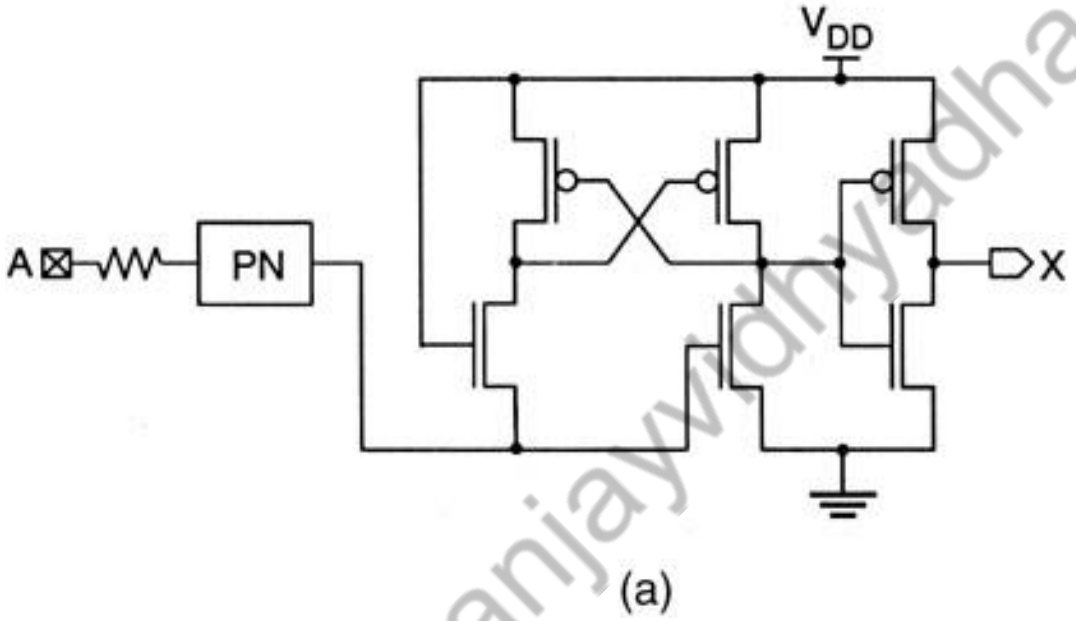
$$r = 6.5$$

$$r = \sqrt{\frac{\mu_n C_{ox} W_n/L_n}{\mu_p C_{ox} W_p/L_p}}$$

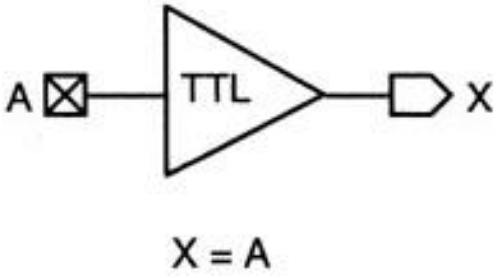
$$\frac{W_n/L_n}{W_p/L_p} = \frac{1}{3}6.5^2 = \frac{169}{12}$$

TTL to CMOS Level Shifter

Non-inverting TTL Level-shifting Circuit



(a)

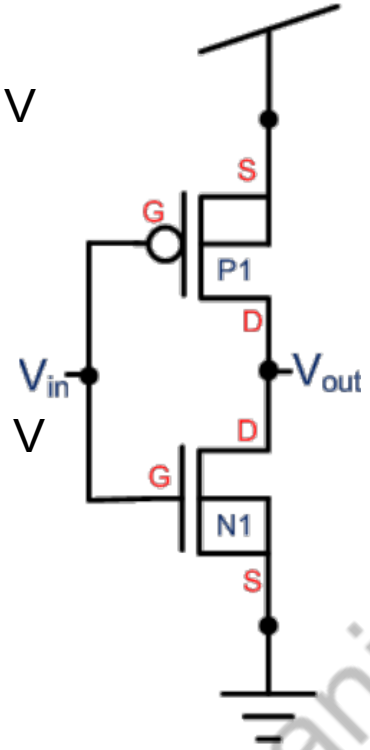


(b)

CMOS Level Shifter

V_{DDH} = 1.8 V

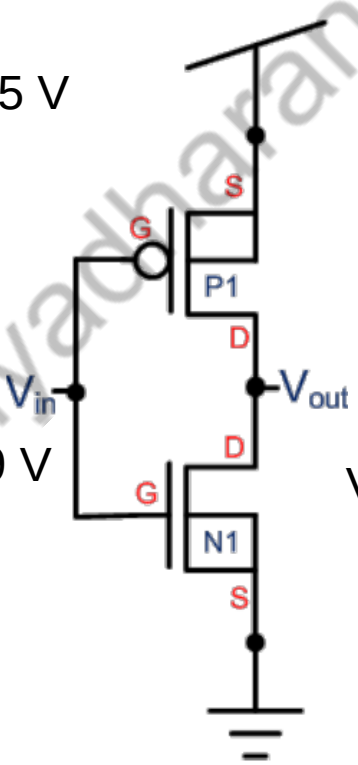
V_T = 0.75 V



V_{DDL} = 1.2 V

V_{DDH} = 1.8 V

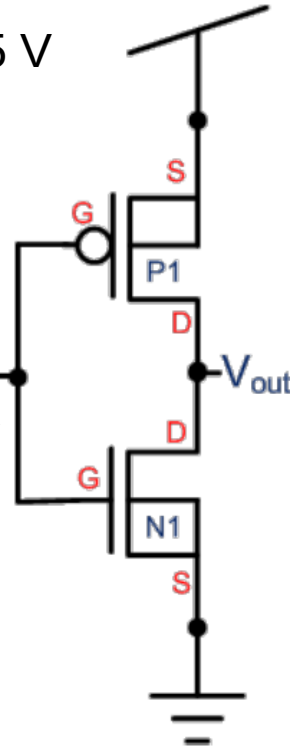
V_T = 0.75 V



V_{DDL} = 0.9 V

V_{DDH} = 1.8 V

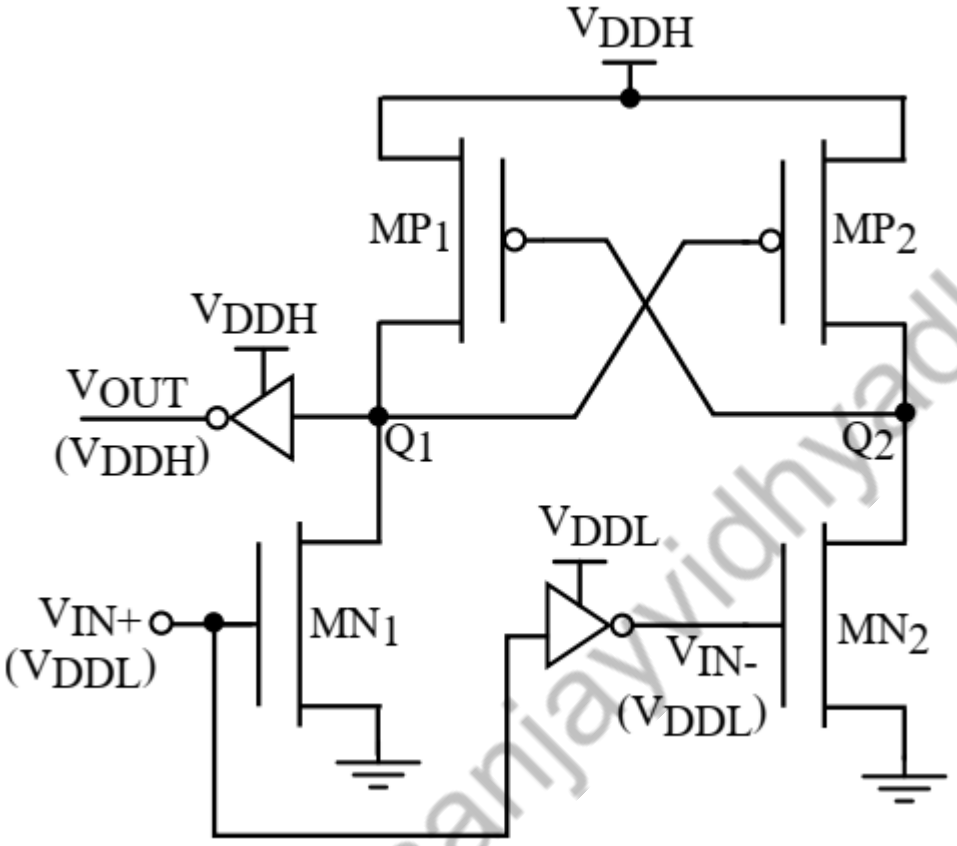
V_T = 0.75 V



V_{DDL} = 0.7 V

Works Fine V_{DDH} and V_{DDL} are Close.

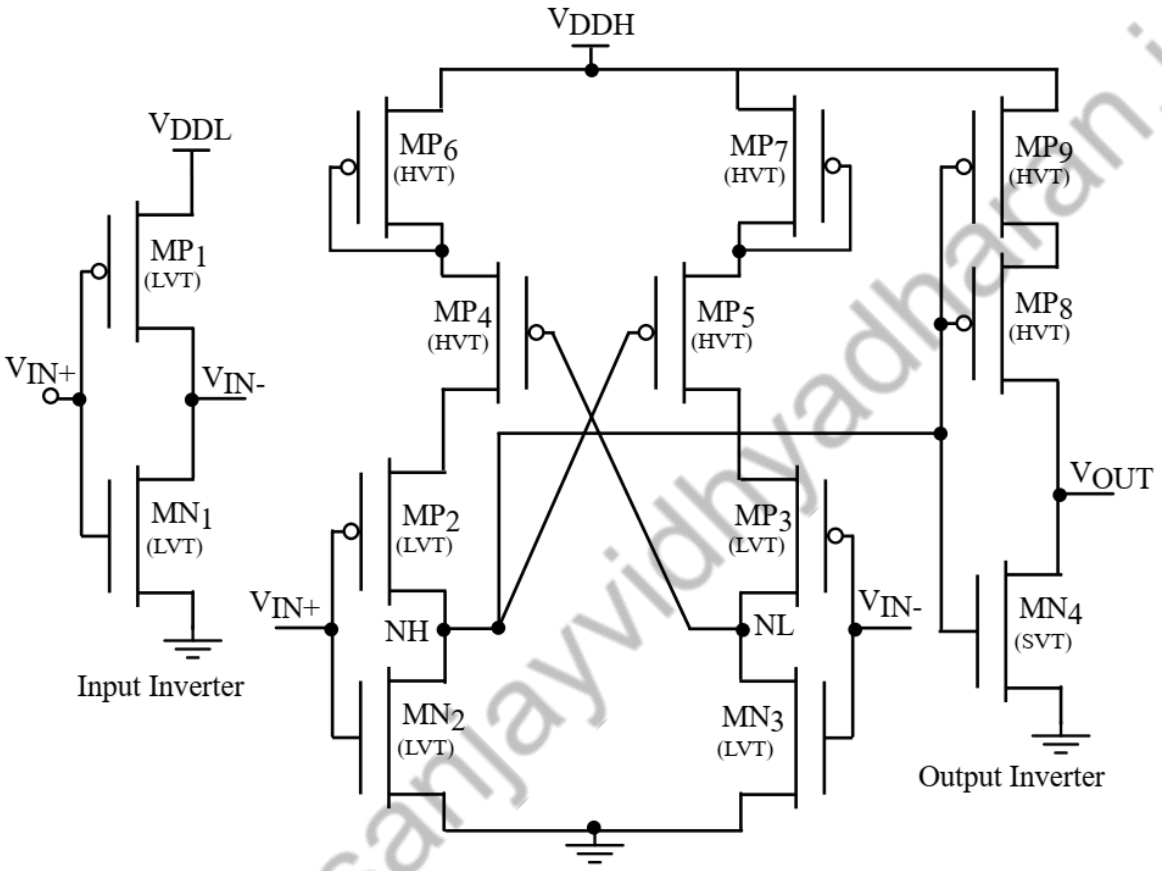
CMOS Level Shifter



Works Fine for $V_{DDL} > V_T$.

P.O. Pouliquen, in Proceedings of 2010 IEEE International Symposium on Circuits and Systems (2010), pp. 40974100. DOI 10.1109/ISCAS.2010.5537627

CMOS Level Shifter



V_{DDH} = 1 V (90 nm)

V_{DDL} = 0.18 V

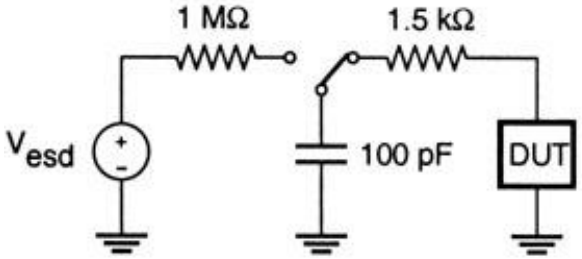
V_{HVT} = 0.535 V

V_{SVT} = 0.360 V

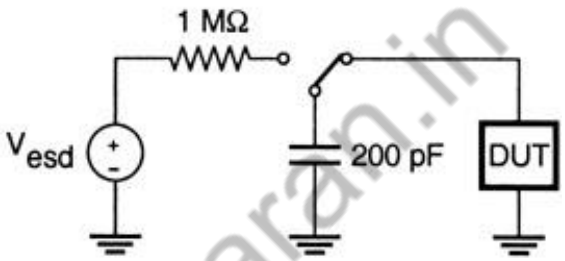
V_{LVT} = 0.230 V

M. Lanuzza, P. Corsonello, S. Perri, IEEE Transactions on Circuits and Systems II: Express Briefs 59(12), 922 (2012). DOI 10.1109/TCSII.2012.2231037

Electrostatic Discharge (ESD)



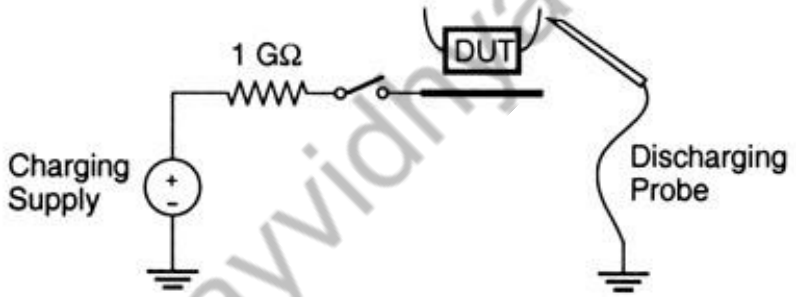
(a)



(b)

(b) machine model

(a) Human Body 1.5 kV of static voltage stress



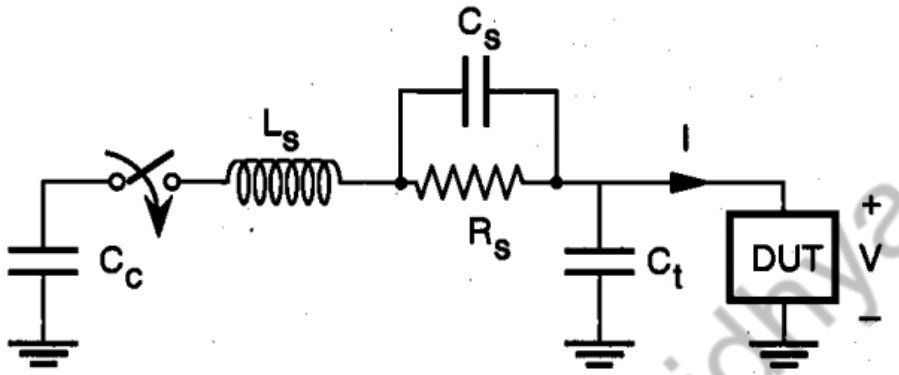
(c)

(c) charged device model, for ESD testing

Effective protection networks can withstand as high as 8-kV

Electrostatic Discharge (ESD)

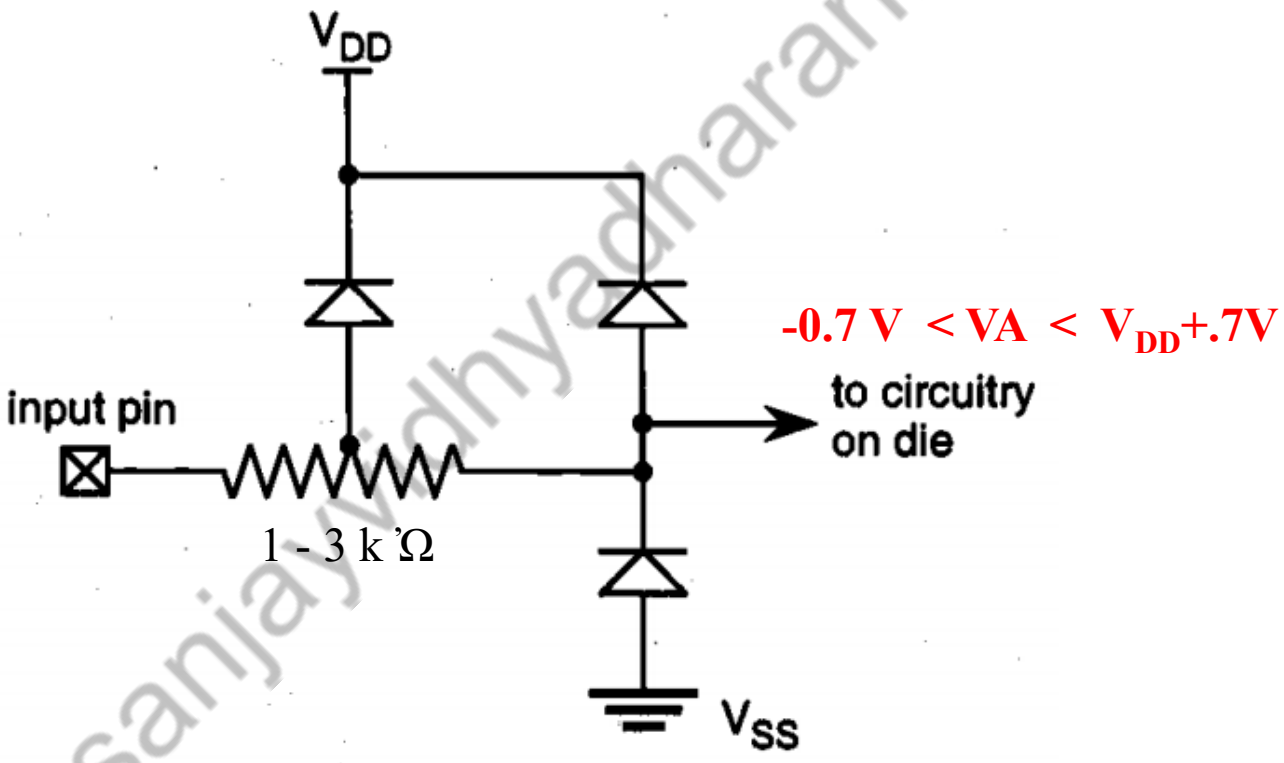
Models for ESD testing



Component	HBM	MM
C_c (pF)	100	200
R_s (Ω)	1500	25
L_s (μH)	5	2.5
C_s (pF)	1	0
C_t (pF)	10	10

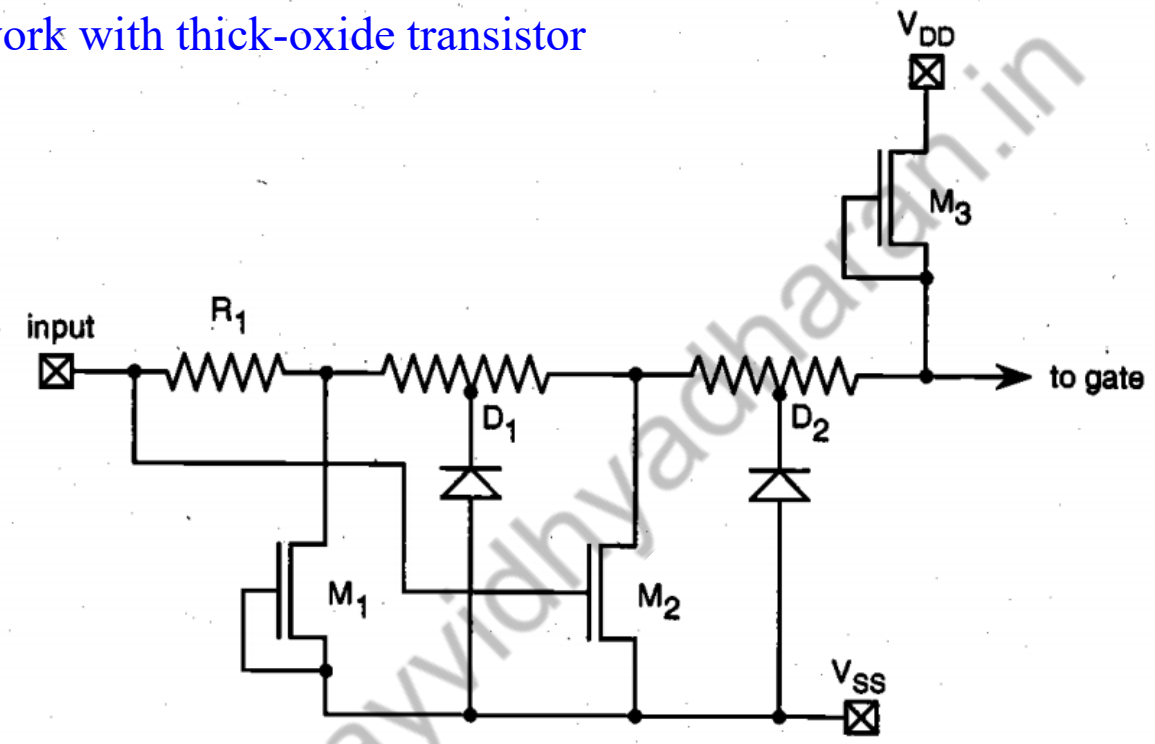
Electrostatic Discharge (ESD)

ESD Protection Network



Electrostatic Discharge (ESD)

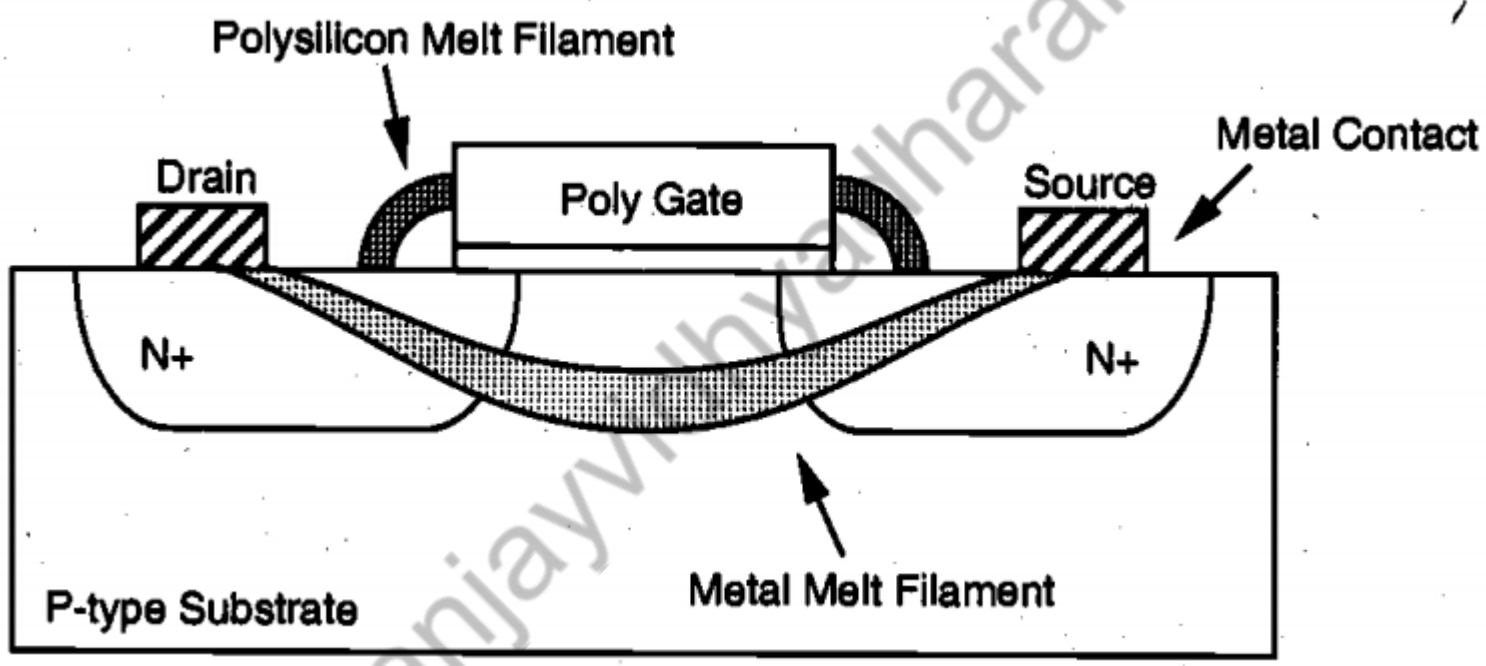
Protection network with thick-oxide transistor



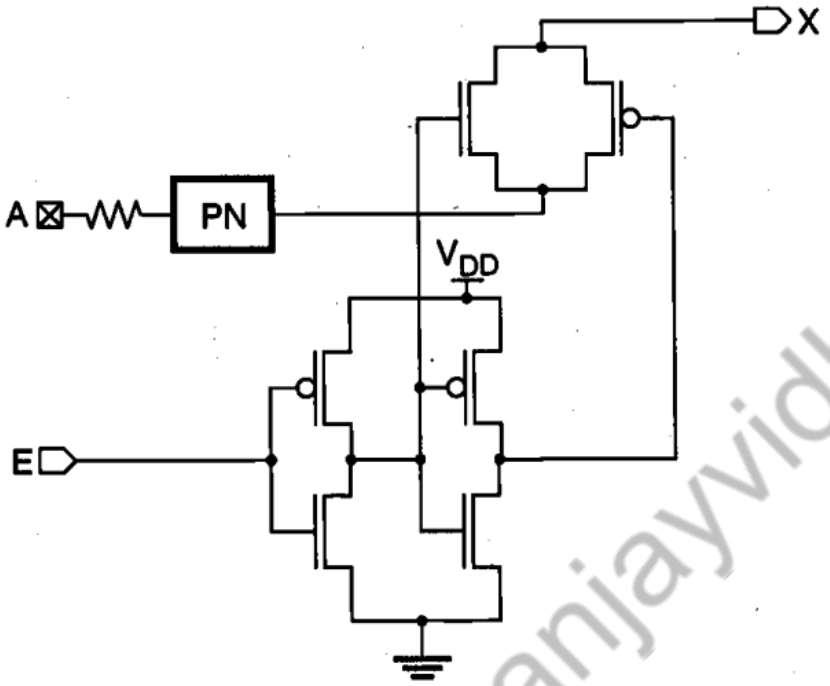
Ml and M2 have threshold values of 20 to 30 V.

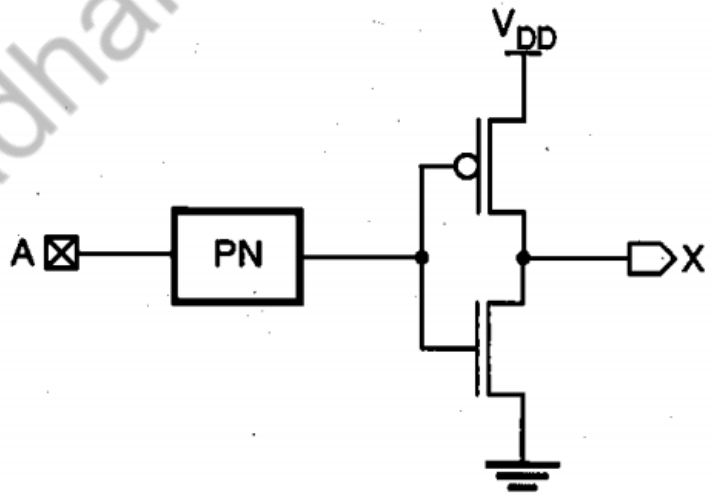
Electrostatic Discharge (ESD)

Typical ESD failure modes.



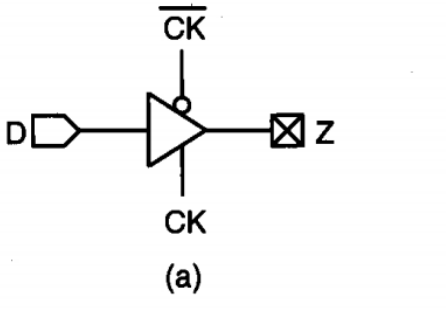
Input Circuits

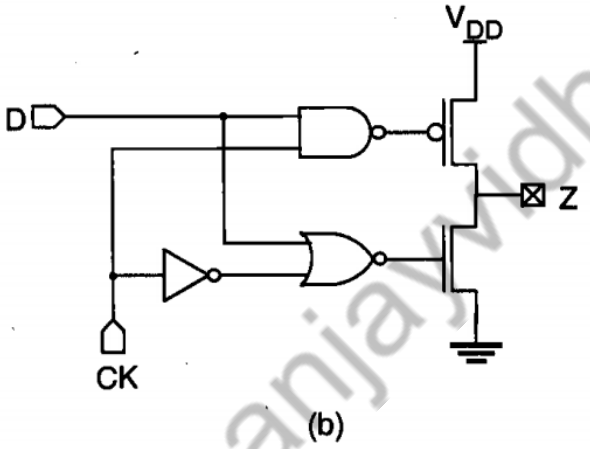




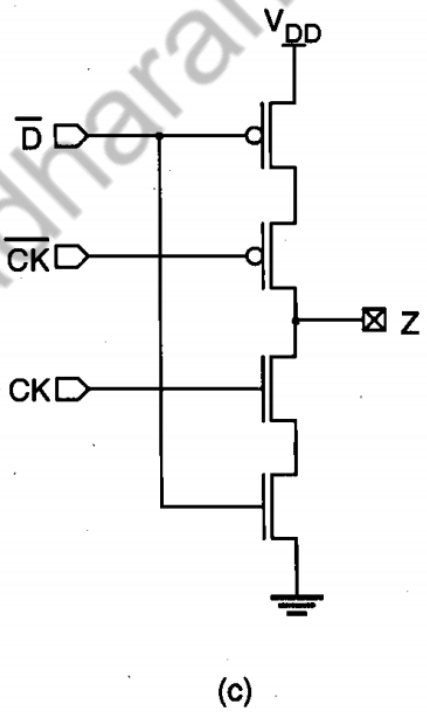
Internal Drivers to Prevent
Voltage drop in bonding wires

Output Circuits





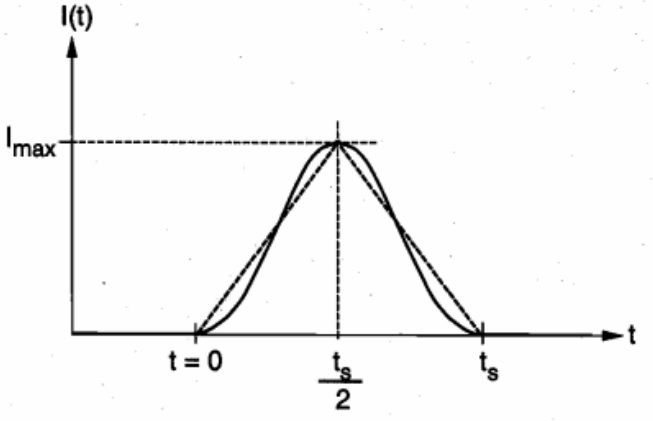
12 transistors



Four Very large Sized transistors

Output Circuits

High rate of change in the current ***di/dt*** and can cause significant on-chip noise problems due to the *L(di/dt)*drop across the bonding wire connecting the output pad to the package.



$$Q = CV$$

$$\frac{I_{max}}{2} * \frac{t_s}{2} = C_{load}\frac{V_{DD}}{2}$$

$$I_{max}\frac{t_s}{2} = C_{load}V_{DD}$$

$$\left[\frac{di}{dt}\right]_{max} \geq \frac{I_{max}}{t_s/2} = \frac{2I_{max}}{t_s}$$

$$\left[\frac{di}{dt}\right]_{max} \geq \frac{4C_{load}V_{DD}}{t_s^2}$$

C_{load} = 100 pF and t = 5 ns, then

$$\left[\frac{di}{dt}\right]_{max} \geq \frac{4\times100\times10^{-12}\times5}{\left(5\times10^{-9}\right)^2} = 80\ \frac{\text{mA}}{\text{ns}}$$

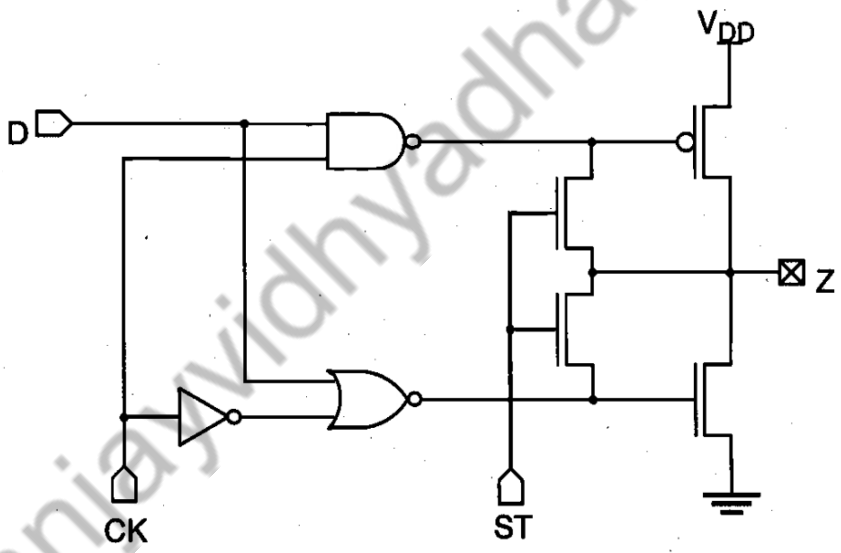
for a bonding wire with L = 2 nH,

$$L\left[\frac{di}{dt}\right]_{max} \geq 160\ \text{mV}$$

This voltage drop would be quadrupled if t were reduced by a factor of two.
Trade-off between the delay time and the noise

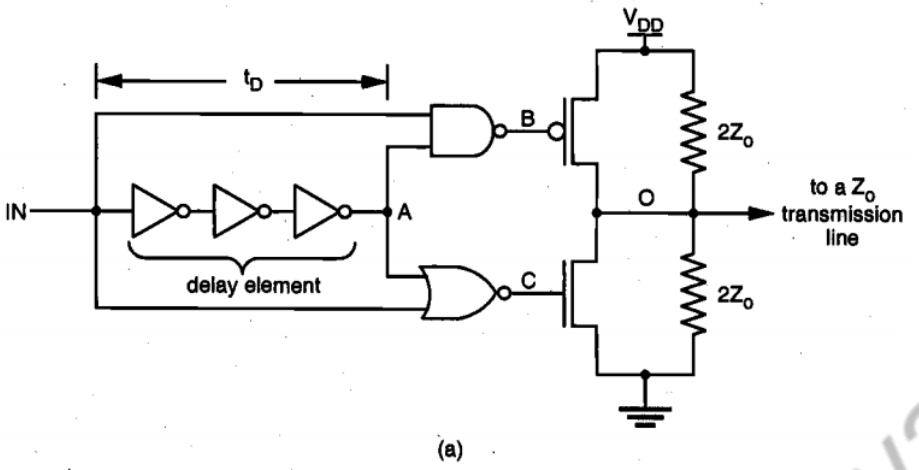
Output Circuits

In a CMOS chip the current surge can be as high as 1100 mA/ns at power and ground terminals. For a microprocessor with 32 bits or higher number of data bus lines, the noise problem can be significantly escalated if all output drivers are driven simultaneously. In such cases, it is desirable to stagger the switching times with built-in delays

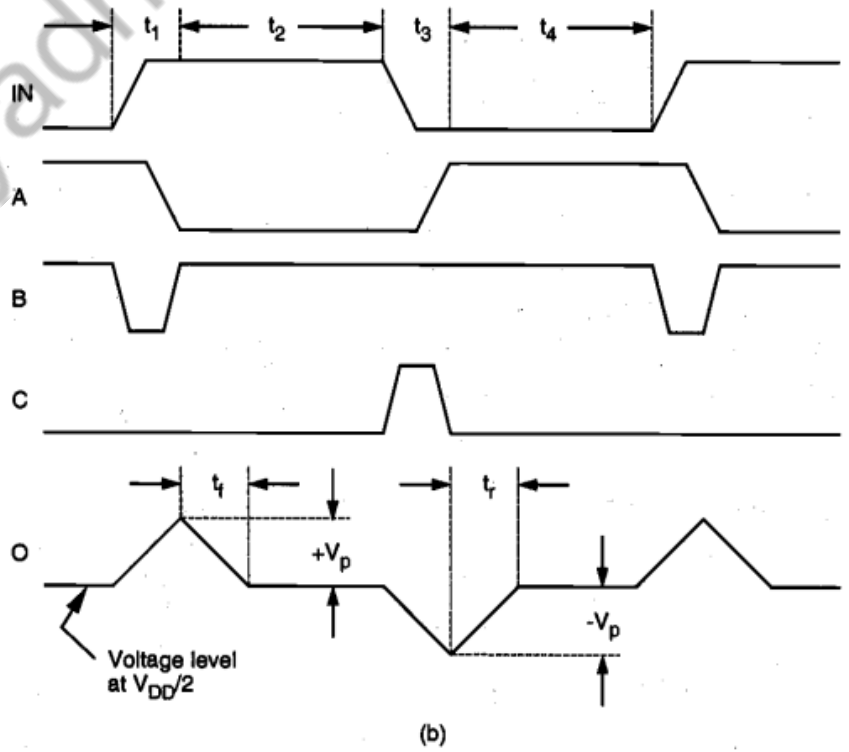


The role of two nMOS transistors controlled by the strobe signal (ST) is to pre-charge the gate potentials of the last-stage driver transistors at an approximate midpoint between the initial and final potentials of the load capacitor.

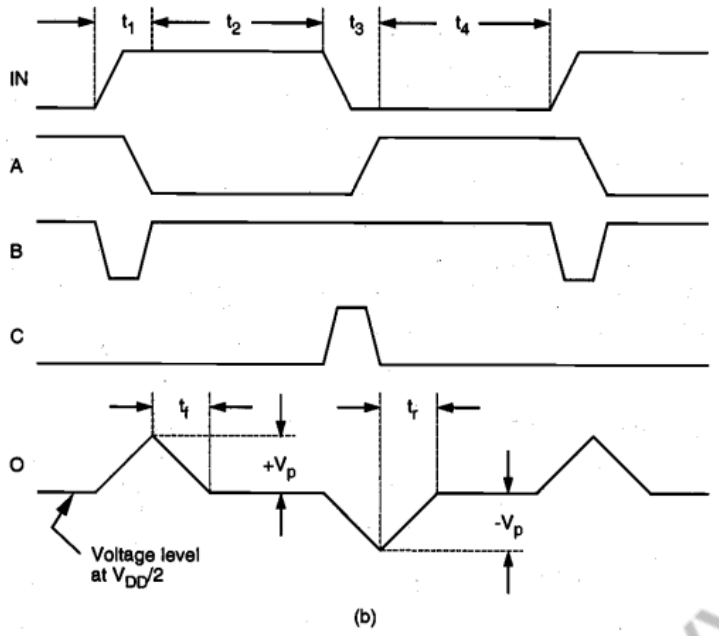
Output Circuits

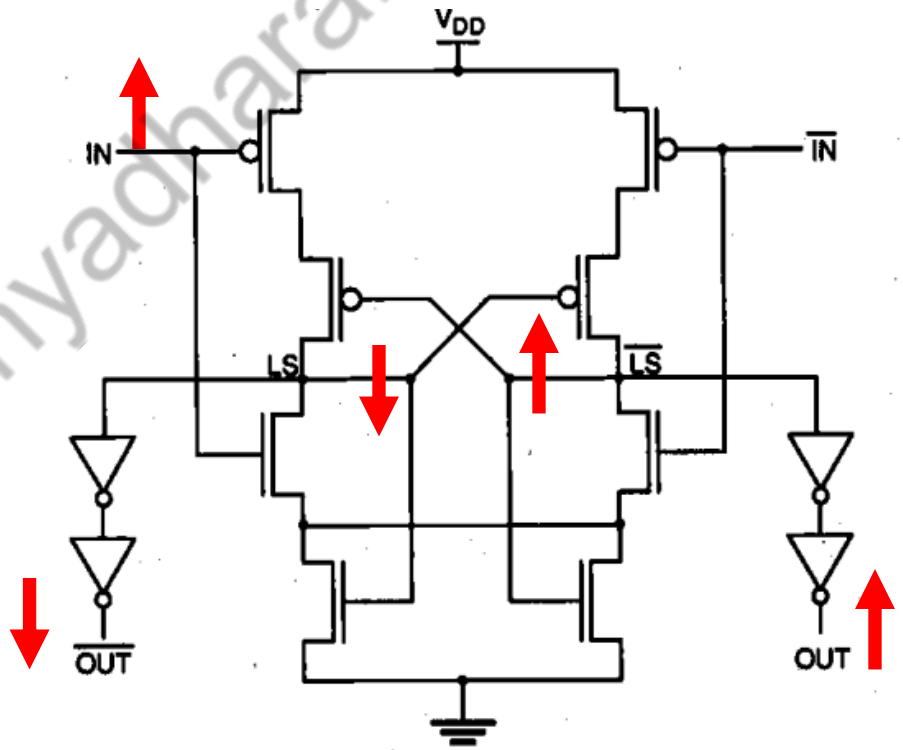


The circuit sends out only changes in the data pattern



Output Circuits





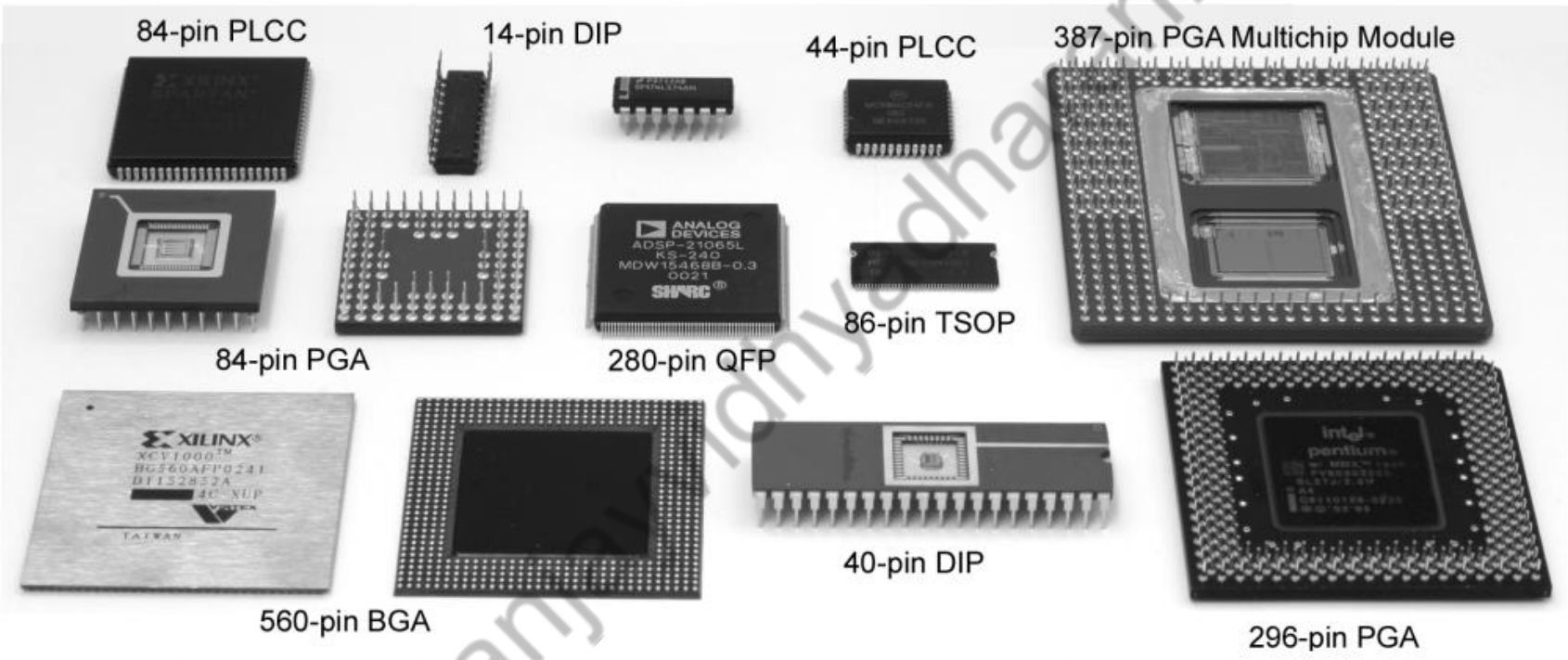
Packages

Package functions

– Electrical connection of signals and power from chip to board
– Little delay or distortion
– Mechanical connection of chip to board
– Removes heat produced on chip
– Protects chip from mechanical damage
– Compatible with thermal expansion
– Inexpensive to manufacture and test

Package Types

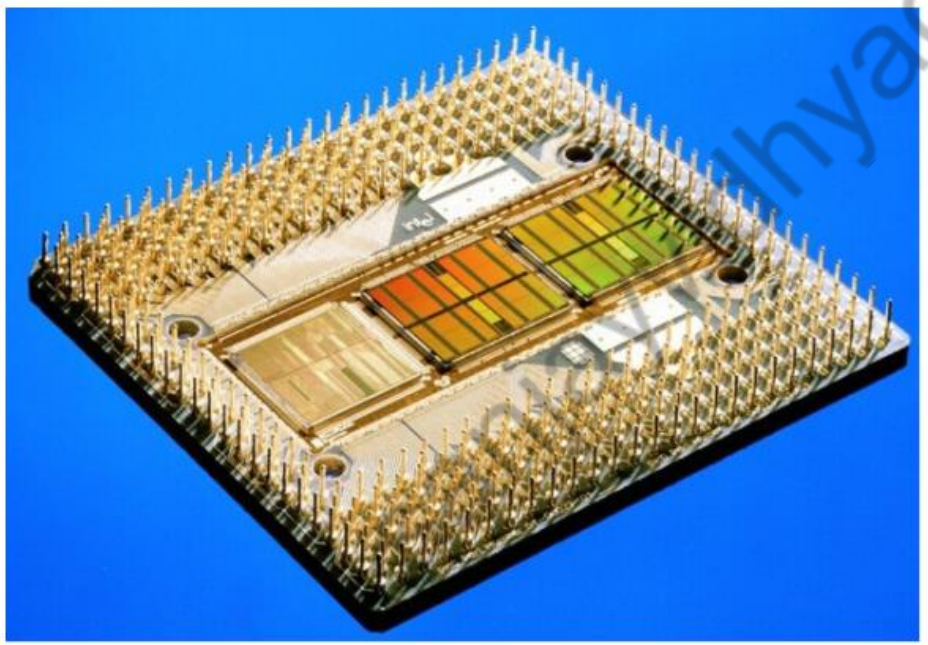
- Through-hole vs. surface mount



DIP: Dual-inline package, PGA: Pin grid array; PLCC: Plastic leadless chip carrier
BGA: Ball grid array, QFP: Quad flat pack, TSOP: Thin small outline package

Multichip Modules

- Pentium Pro MCM
  - Fast connection of CPU to cache
  - Expensive, requires known good dice

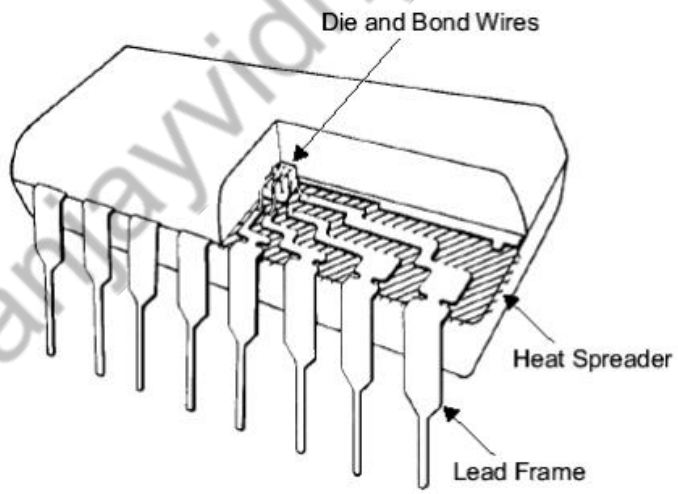


Microprocessor +
one or two external cache die

IBM z900 mainframe:
20 CPUs, 8 cache chips, 1km of Interconnect, 127mm on a side,
1.3 kW power

Chip-to-Package Bonding

- Traditionally, chip is surrounded by *pad frame*
  - Metal pads on 100 – 200 µm pitch
  - Gold *bond wires* attach pads to package
  - *Lead frame* distributes signals in package
  - Metal *heat spreader* helps with cooling



Heat Dissipation

- 60 W light bulb has surface area of 120 cm^2
- Itanium 2 die dissipates 130 W over 4 cm^2
  - Chips have enormous power densities
  - Cooling is a serious challenge
- Package spreads heat to larger surface area
  - Heat sinks may increase surface area further
  - Fans increase airflow rate over surface area
  - Liquid cooling used in extreme cases ($$$)
  - Smart and active cooling using microfluidics (our project as Duke University)

Thank you