VLSI SYSTEMS AND ARCHITECTURE
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Lab-6 : Multiplexer Design in Xilinx

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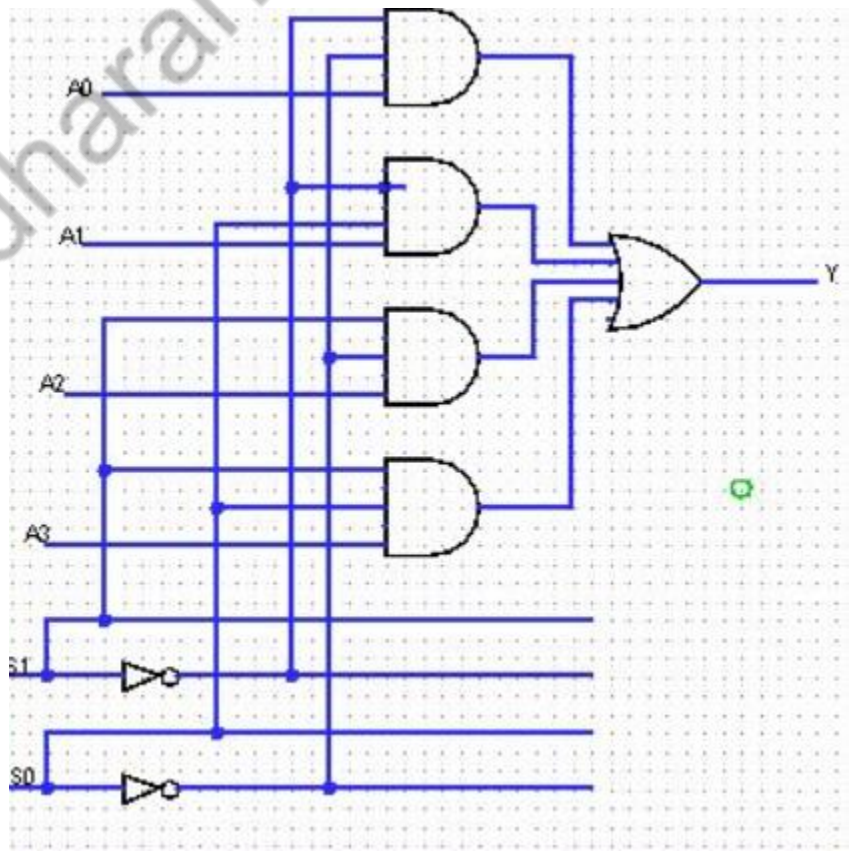
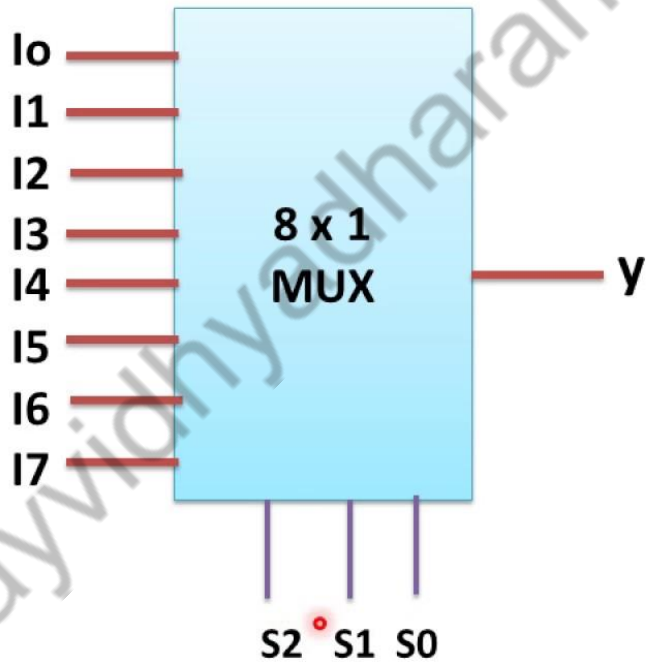
The Multiplexer

```
module m41 (out, a, b, c, d, s0, s1);
output out;
input a, b, c, d, s0, s1;
wire sobar, s1bar, T1, T2, T3, T4;
not (s0bar, s0), (s1bar, s1);
and (T1, a, s0bar, s1bar),
(T2, b, s0bar, s1),
(T3, c, s0, s1bar),
(T4, d, s0, s1);
or(out, T1, T2, T3, T4);
endmodule
```



The Multiplexer

```
module Mux(
    input [7:0] I,
    input [2:0] S,
    output Y
    );
assign Y = I[S];
endmodule
```



S2	S1	S0	Y
0	0	0	Io
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Full Adder

```
module FullAdder(
    input A,
    input B,
    input Cin,
    output Sum, Carry
    );
wire [7:0] s;
wire [7:0] c;
assign s = 8'b10010110;
Mux m1 (s,{A,B,Cin},Sum);
assign c = 8'b11101000;
Mux m2 (c,{A,B,Cin},Carry);
endmodule
```

```
module Mux(
    input [7:0] I,
    input [2:0] S,
    output Y
    );
assign Y = I[S];
endmodule
```

Inputs			Outputs	
A	B	C_{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Thank you