VLSI SYSTEMS AND ARCHITECTURE
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Lab-5 : Decoder Design in Xilinx

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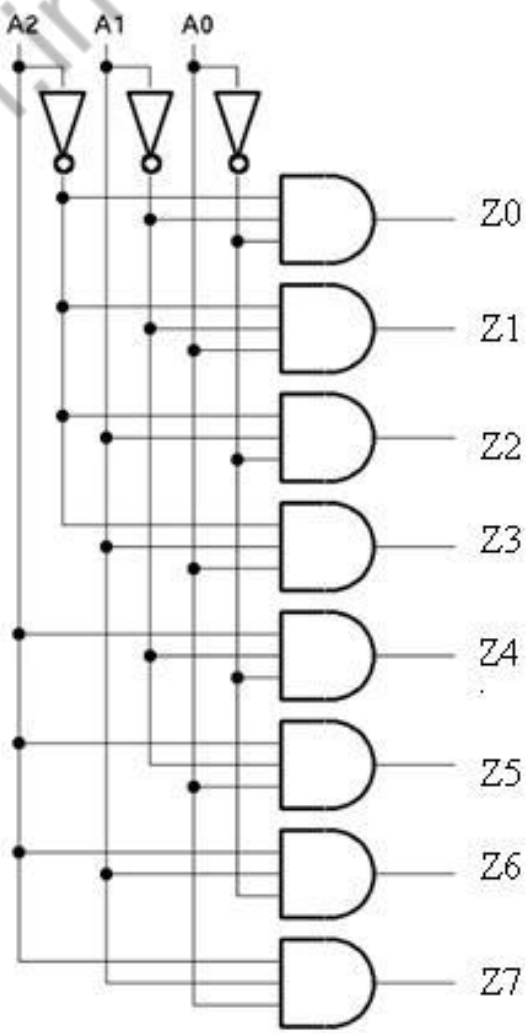
The Decoder

```
module
Decoder(a,b,c,d0,d1,d2,d3,d4,d5,d6,d7);
input a,b,c;
output d0,d1,d2,d3,d4,d5,d6,d7;
assign d0=(~a&~b&~c),
d1=(~a&~b&c),
d2=(~a&b&~c),
d3=(~a&b&c),
d4=(a&~b&~c),
d5=(a&~b&c),
d6=(a&b&~c),
d7=(a&b&c);
endmodule
```



The Conditional Statement

If statement in Verilog

```
if (sel == 1) f = a;
else f = b;
```

Example : X is output of a Decoder, Y is output Function

```
begin
        if (x[3] == 1'b1)  y = 2'b11;
        else if (x[2] == 1'b1)  y = 2'b10;
        else if (x[1] == 1'b1)  y = 2'b01;
        else  y = 2'b00;
end
```

The Decoder

```
module decoder (in,out);
input [2:0] in;
output [7:0] out;
assign out =
(in == 3'b000 ) ? 8'b0000_0001 :
(in == 3'b001 ) ? 8'b0000_0010 :
(in == 3'b010 ) ? 8'b0000_0100 :
(in == 3'b011 ) ? 8'b0000_1000 :
(in == 3'b100 ) ? 8'b0001_0000 :
(in == 3'b101 ) ? 8'b0010_0000 :
(in == 3'b110 ) ? 8'b0100_0000 :
(in == 3'b111 ) ? 8'b1000_0000 :
8'h00;
endmodule
```

Full Adder

```
module Full_Adder (

input [2:0] in,
output Sum, Carry);

wire[7:0]W;

decoder G (in,W);
assign Sum=(W[1]|W[2]|W[4]|W[7]);
assign Carry=(W[3]|W[5]|W[6]|W[7]);
endmodule
```

Thank you