



# **VLSI SYSTEMS AND ARCHITECTURE**

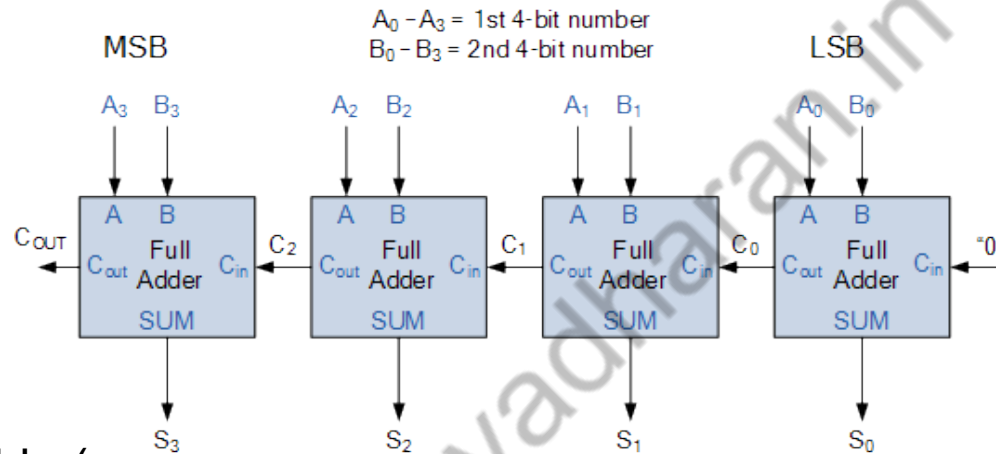
## **2021-22**

### **Lab-4 : Handling multi-bit data and Concatenation in Verilog**

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# Demonstration : 4-bit Adder



```

module Four_bit_adder(
    input [3:0] A,
    input [3:0] B,
    output [3:0] Sum,
    output Carry );

assign {Carry,Sum}=A+B;

endmodule
    
```

## Remarks

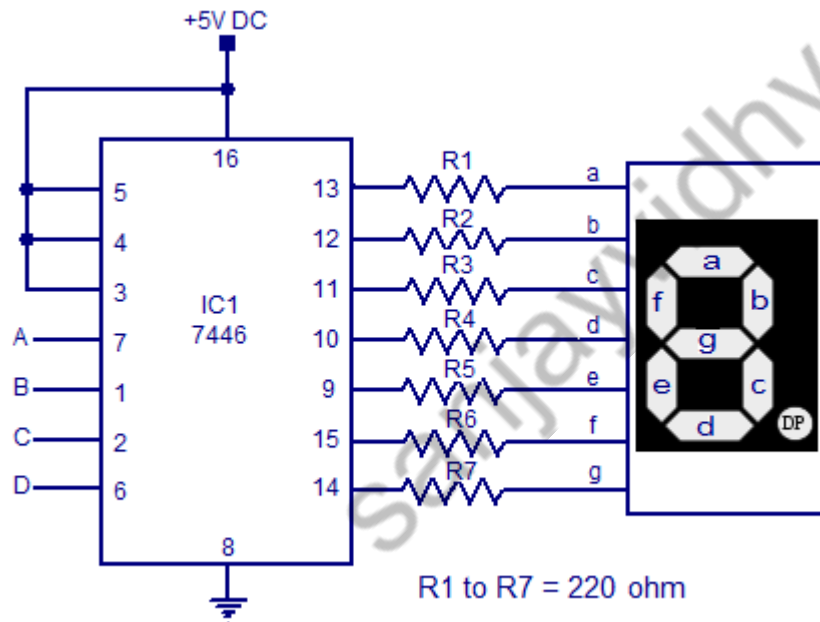
[3:0] [MSB:LSB]

Concatenation

# Binary Coded Decimal

## General digital systems

User enters decimal  $\rightarrow$  BCD i/p  $\rightarrow$  Binary i/p  $\rightarrow$  compute in binary  $\rightarrow$  Binary o/p  $\rightarrow$  BCD o/p  $\rightarrow$  Decimal output shown to user



# Binary Coded Decimal

## BCD addition

$$4 + 5$$

4 0 1 0 0

5 0 1 0 1

9 1 0 0 1      Expected Result

$$4 + 8$$

4 0 1 0 0

8 1 0 0 0

1 1 0 0      Is this expected Result ?

Expected answer    0001 0010  
is BCD of 12

# Binary Coded Decimal

## BCD addition

4 + 8            4 0 1 0 0

8 1 0 0 0

Greater than 9

1 1 0 0

0 1 1 0

0 0 0 1 0 0 1 0

1            2

Add correction of +6

= To skip 6 invalid  
states (10 - 15) BCDs

# Binary Coded Decimal

## BCD addition

9 + 9            9 1 0 0 1

9 1 0 0 1

Carry out generated    1 0 0 1 0

Expected result ?

0 1 1 0

Add correction of +6

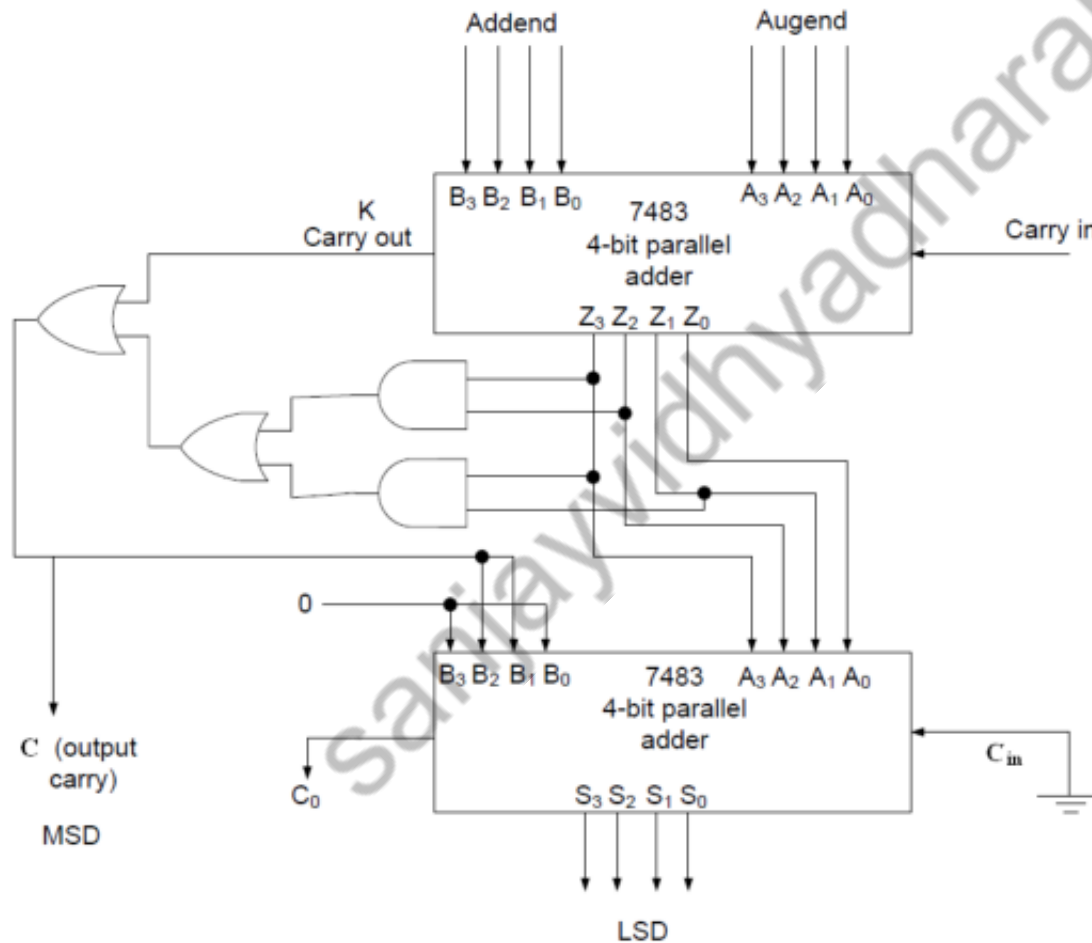
0 0 0 1 1 0 0 0

1            8

After addition if carry out is generated or if sum is greater than 9 there is need for correction

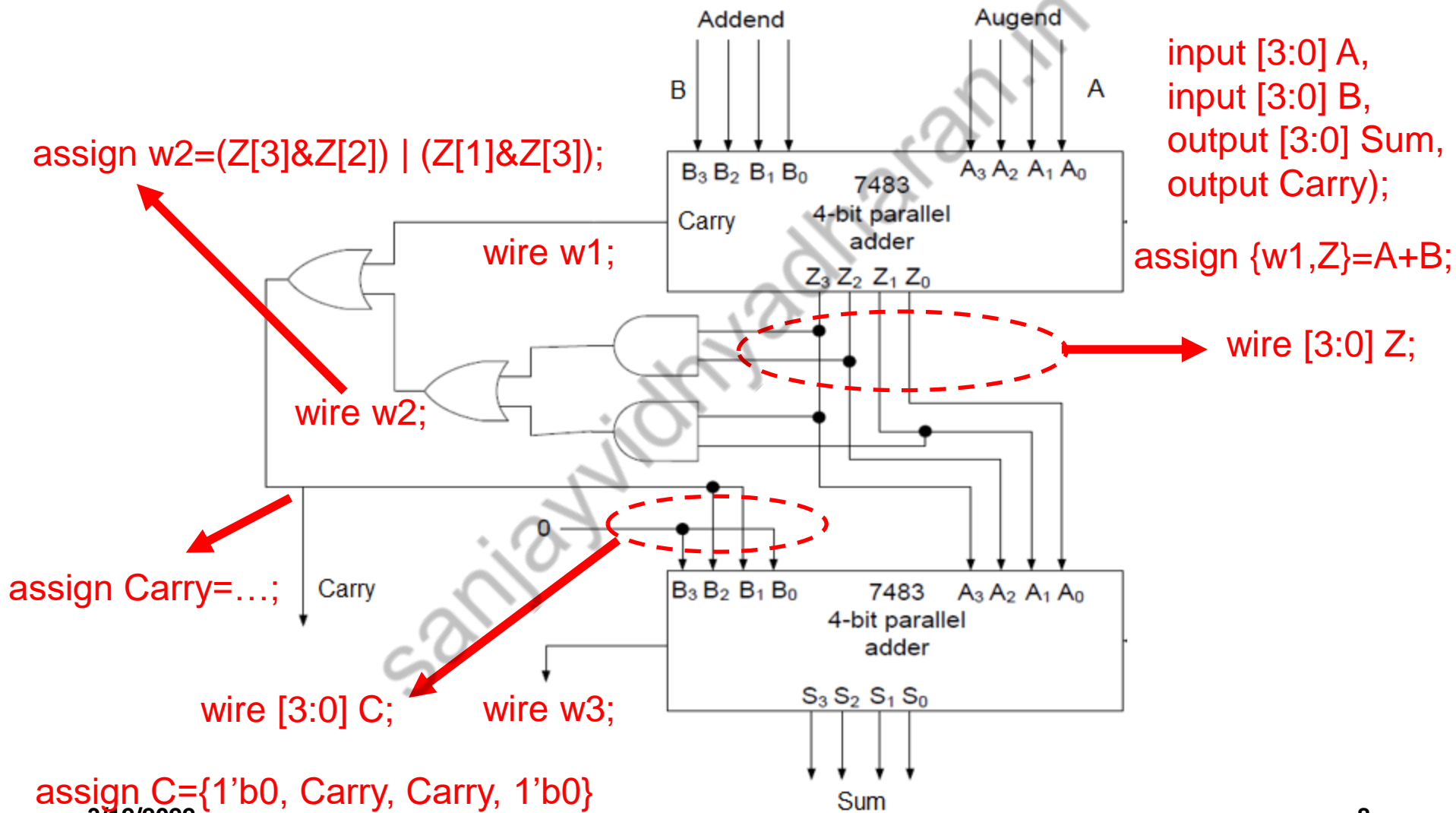
# Binary Coded Decimal

## BCD addition



0 0 0 0  
 0 0 0 1  
 0 0 1 0  
 0 0 1 1  
 0 1 0 0  
 0 1 0 1  
 0 1 1 0  
 0 1 1 1  
 1 0 0 0  
 1 0 0 1

# Problem 1: BCD Adder



3/12/2022



**Thank you**