VLSI SYSTEMS AND ARCHITECTURE
2021-22
Lab-3 : Initialization in Verilog

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Simple Circuit for Demonstration

Initialization:

$$Y=(AB+\overline{C}).(CD+\overline{E})$$

```
module    F1 (input A, input B, input C,
output X );
wire      w1, w2 ;
and       g1 (w1,A,B); // and gate instance
not       g2 (w2,C);
or        g3 (X,w1,w2);
endmodule
```

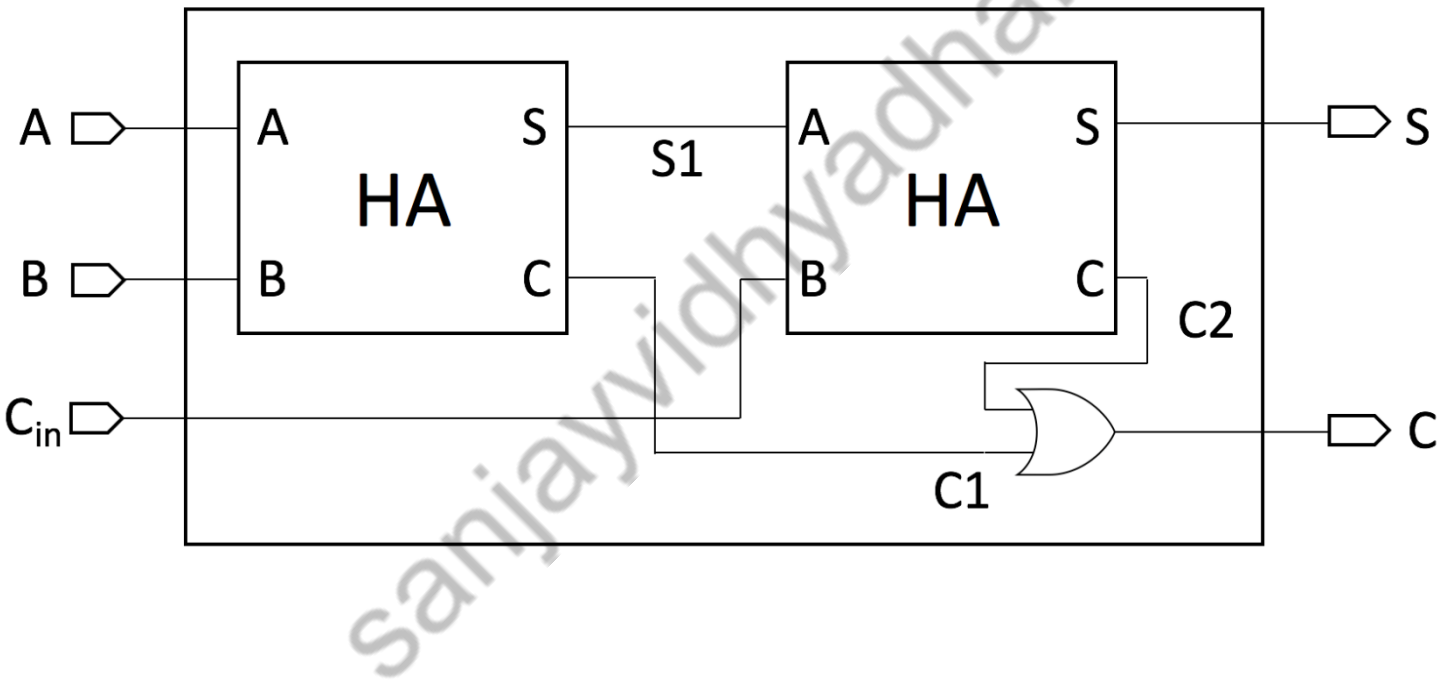
Gate level modeling

```
module   F2 (input A,B,C,D,E, output Y);
wire      w1,w2;

F1 g1 (A,B,C,w1);
F1 g2 (C,D,E,w2);
and  g3 (Y,w1,w2);
endmodule
```

Problem Definition

1. Full Adder with two half adders



Thank you