VLSI Design : 2021-22
Lecture 9
CMOS Static Logic

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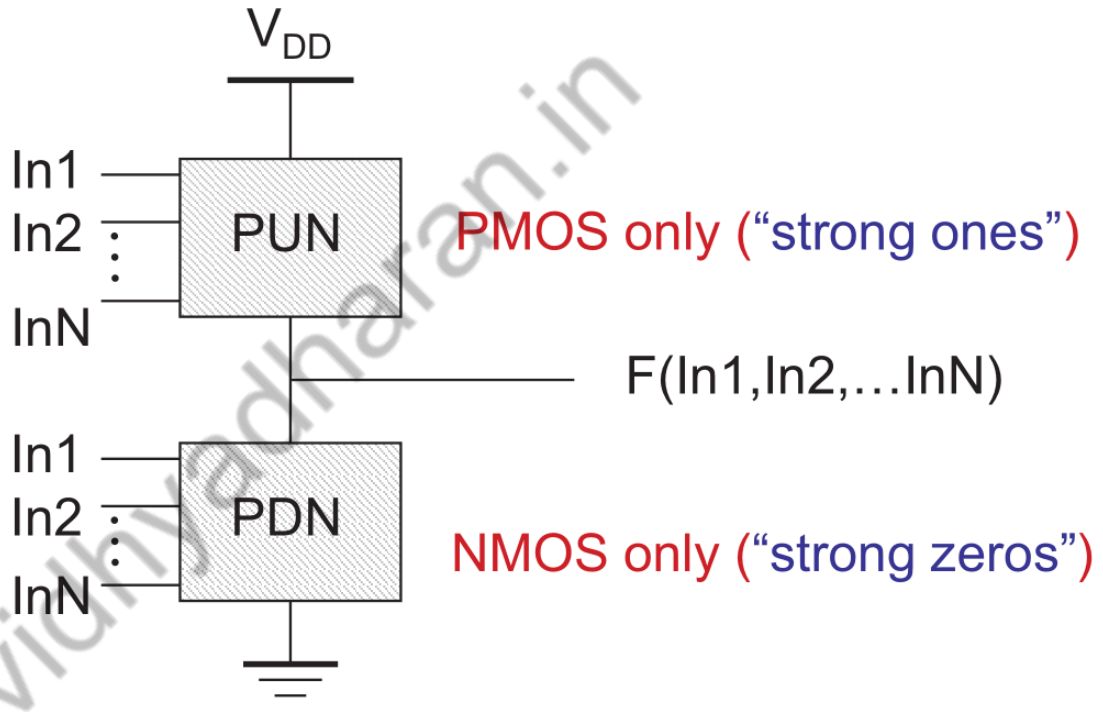
Static CMOS

Pull UP Network
– Build using p-MOS
– Turns ON when Function is TRUE
• Pull DOWN Network
– Build using n-MOS
– Turns ON when Function is FALSE
• Operationally Complement
• Topologically Dual (n)

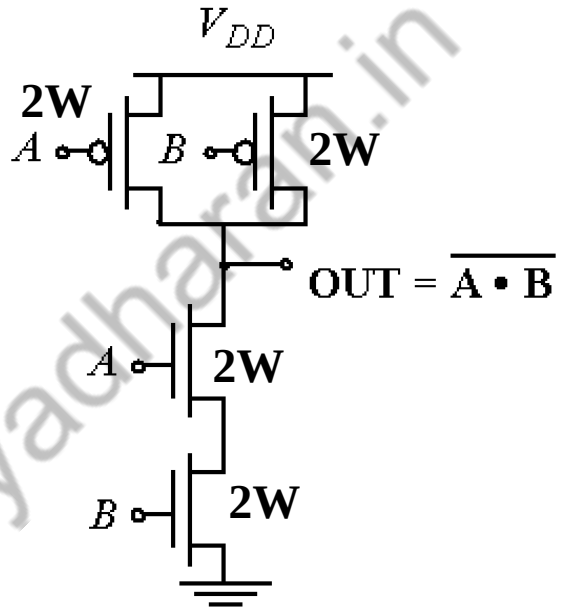


Pull-up Network (PUN) and Pull-down Network (PDN) connected in a Mutually exclusive fashion

STATIC CMOS

A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

Truth Table of a 2 input NAND gate



PDN By Taking complementary of the Required Function = A.B

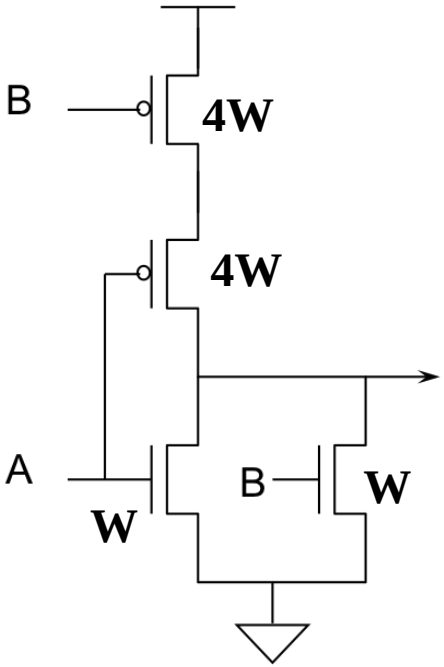
PUP By Taking the Function Directly = A' + B'

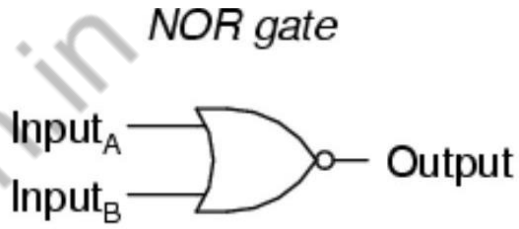
(Inversion of Function Taken care of by PMOS)

AND Implemented by Series Connection

OR Implemented by Parallel Connection

STATIC CMOS





A	B	Output
0	0	1
0	1	0
1	0	0
1	1	0

PDN By Taking complementary of the Required Function = A+B

PUP By Taking the Function Directly = A' . B'

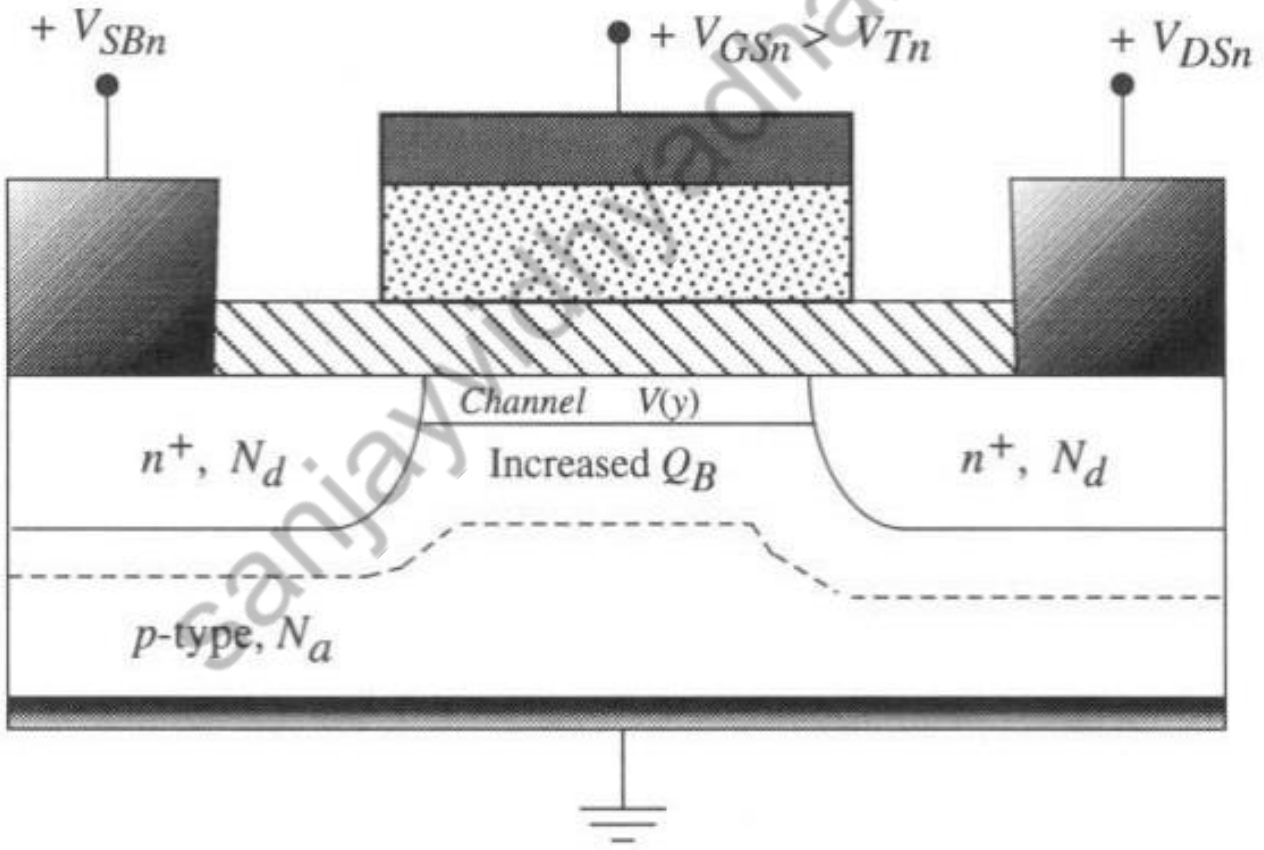
(Inversion of Function Taken care of by PMOS)

AND Implemented by Series Connection

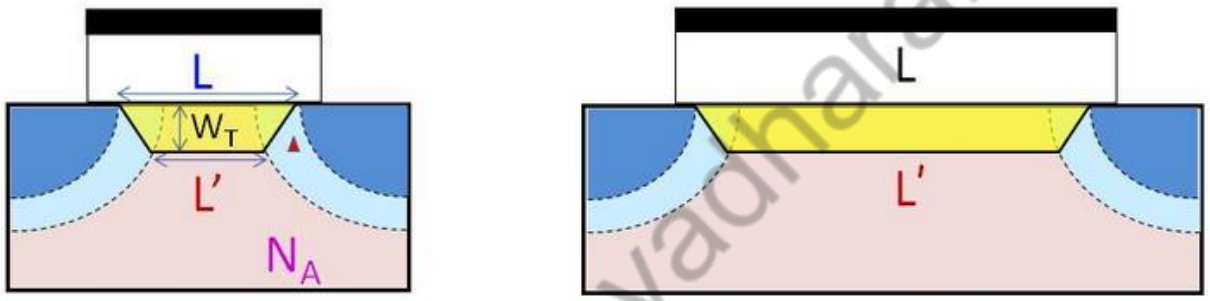
OR Implemented by Parallel Connection

Body-Effect

$$V_{T'n} = V_{FB} + 2|\phi_F| + \frac{1}{C_{ox}}\sqrt{2q\epsilon_{Si}N_a(2|\phi_F| + V_{SBn})} \pm \frac{qD_I}{C_{ox}}$$

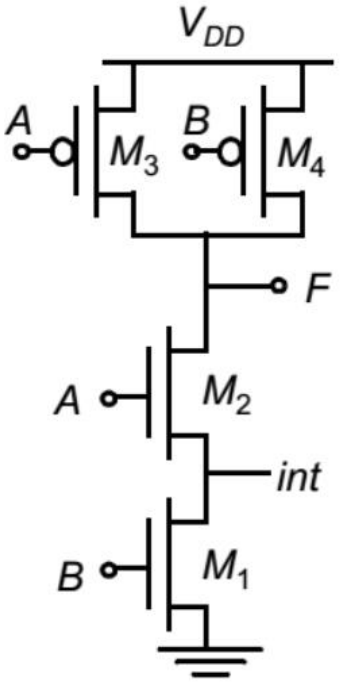


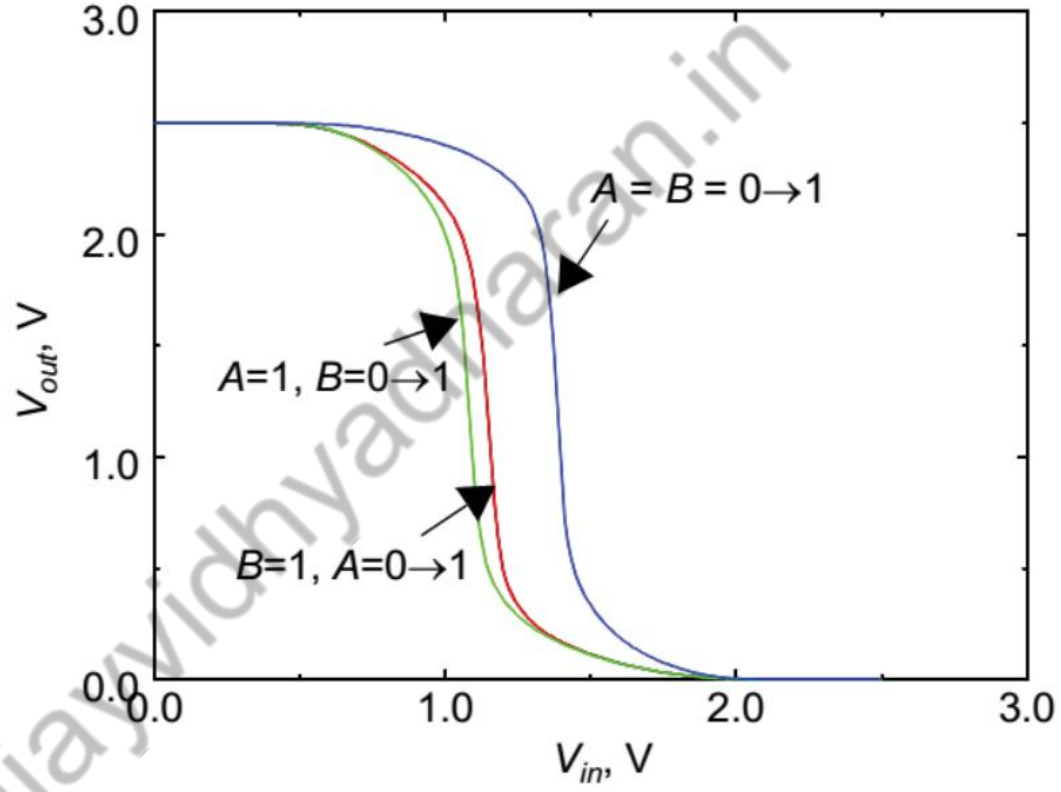
DIBL



The physical origin of DIBL is the increase of the depletion layer due to a high value of Vds that reduces the equivalent channel length and consequently decreases the threshold voltage

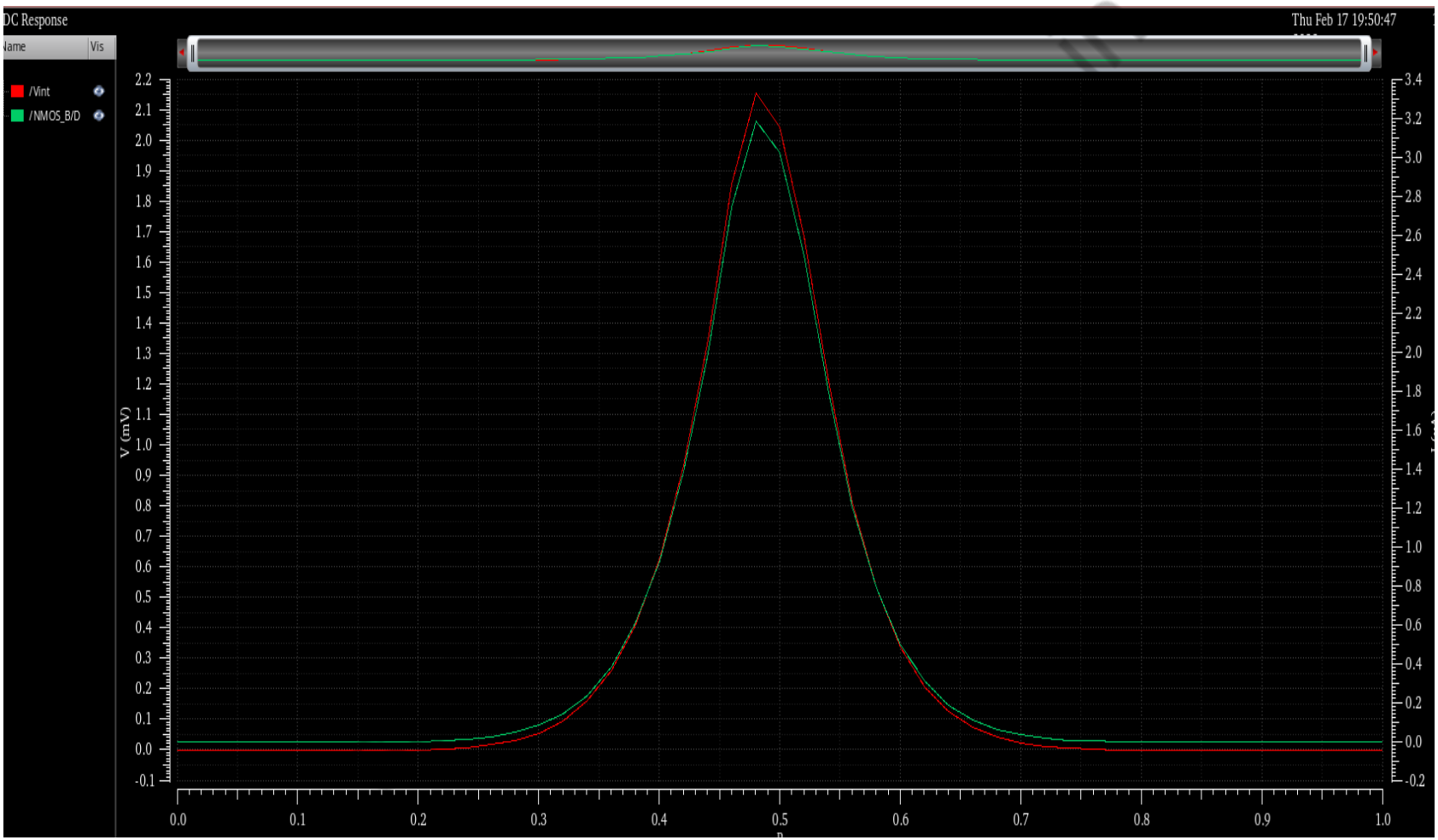
Static Two-Input NAND Gate



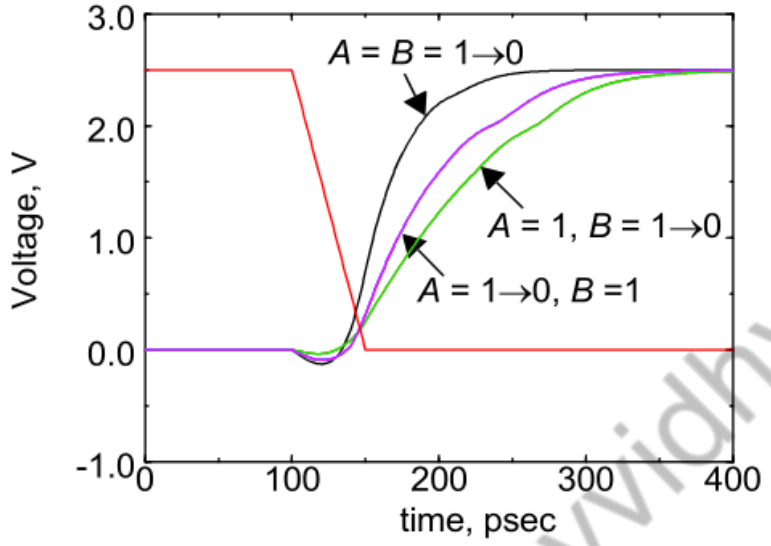


Noise margins are input/pattern dependent!!

Static Two-Input NAND Gate



Static Two-Input NAND Gate



Input Data Pattern	Delay (psec)
A = B= 0→1	69
A = 1, B= 0→1	62
A= 0→1, B = 1	50
A=B=1→0	35
A=1, B = 1→0	76
A= 1→0, B = 1	57

Delays are input/pattern dependent!!

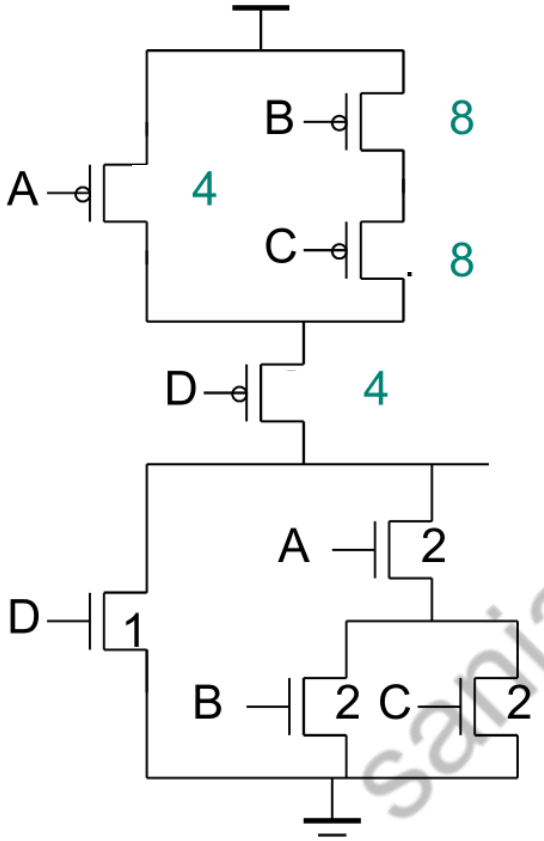
Transistor Sizing for a Complex Gate

Shortest Path First Sizing

$$R_N = \frac{12.5}{(W/L)_n}\ \text{k}\Omega$$

$$R_P = \frac{30}{(W/L)_p}\ \text{k}\Omega$$

OUT = !(D + A • (B + C))

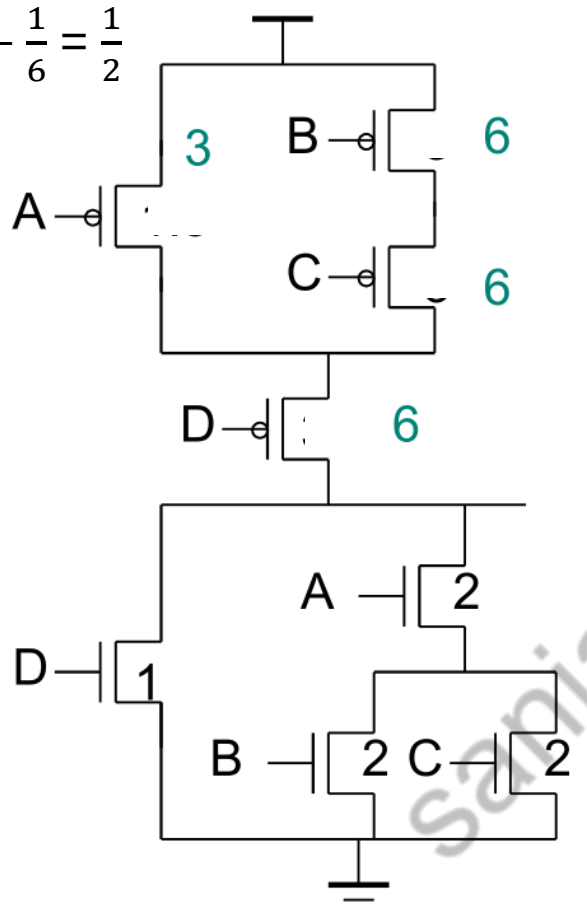


- Total Wp=24
- Shortest path resistance:
  - $Rp_{eff} = \beta(1/4 + 1/4)$
    $= 2 \times (1/2) = 1$
    (same as for an inverter)
- Worst case path resistance:
  - $Rp_{eff} = \beta(1/8 + 1/8 + 1/4)$
    $= 2 \times (1/2) = 1$
- Best case pull up resistance:
  - $Rp_{eff} = \beta\,[((1/8 + 1/8) \,||\, (1/4)) + 1/4]$
    $= \beta\,[1/8 + 1/4] = (3/8)\boldsymbol{\beta} = 0.75$

Transistor Sizing for a Complex Gate

Worst Path First Sizing

OUT = !(D + A • (B + C))



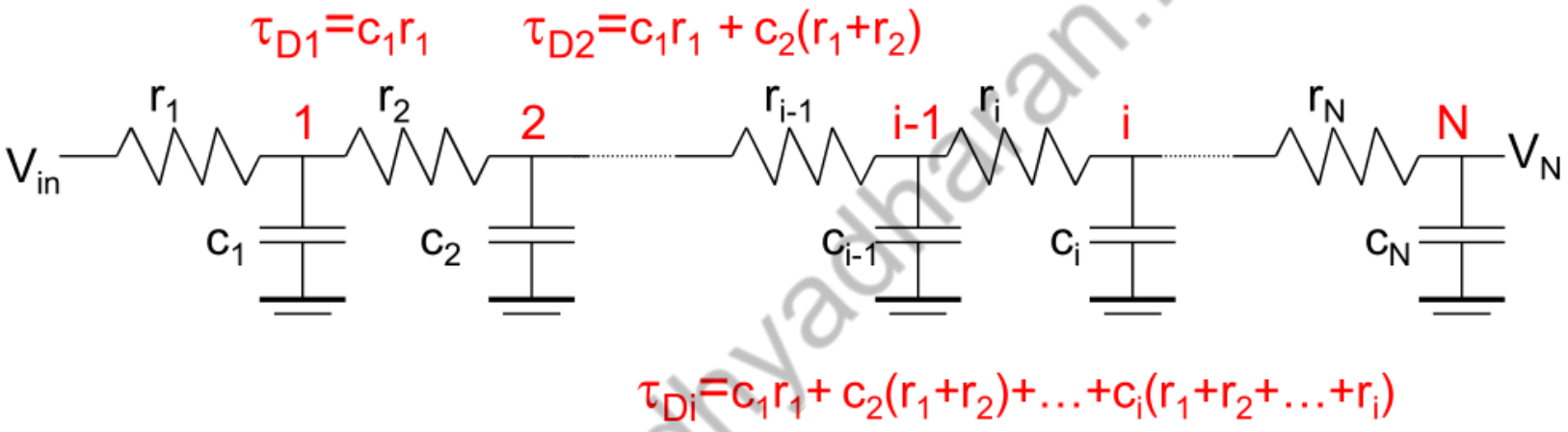
- Total Wp=21 (less area, intrinsic cap)
- Worst case path resistance:
  - $Rp_{eff} = \beta(1/6 + 1/6 + 1/6)$
    $= 2 \times (1/2) = 1$
    (same as for an inverter)
- Shortest path resistance:
  - $Rp_{eff} = \beta(1/3 + 1/6)$
    $= 2 \times (1/2) = 1$
- Best case pull up resistance:
  - $Rp_{eff} = \beta\,[((1/6 + 1/6) \,||\, (1/3)) + 1/6]$
    $= \beta\,[1/6 + 1/6] = (1/3)\boldsymbol{\beta} = 0.66$

(even better than shortest path first sizing!)

Creates larger disparity in delays as a function of inputs

Transistor Sizing for a Complex Gate

Chain Network Elmore Delay



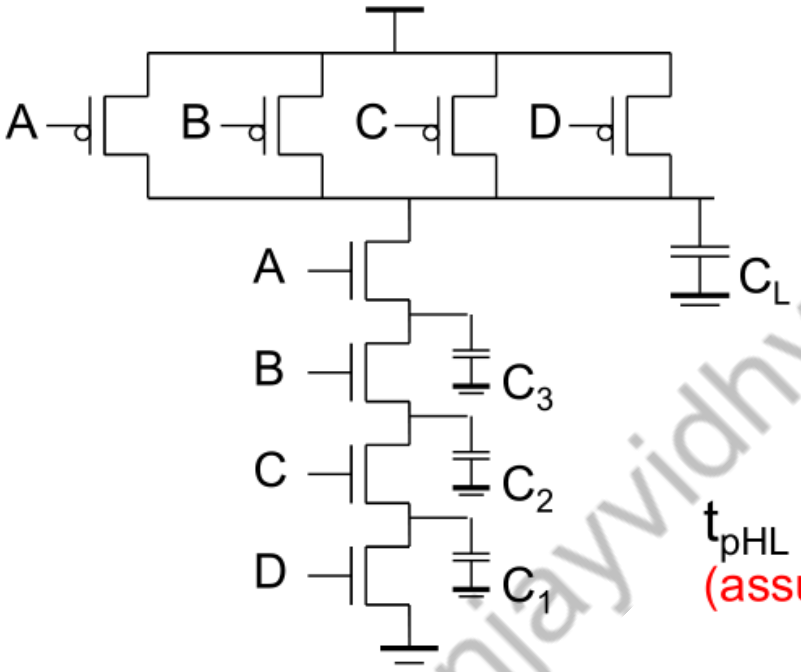
Elmore delay equation $\tau_{DN} = \sum c_i r_{ii} = \sum_{}^{N} c_i \sum_{}^{i} r_j$

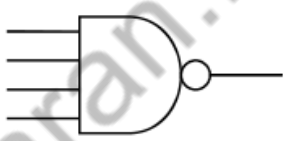
If all resistors are equal size,

$$\tau_{Di}=c_1r_{eq}+ 2c_2r_{eq}+ 3c_3r_{eq}+\ldots+ ic_ir_{eq}$$

Transistor Sizing for a Complex Gate

Fanin considerations





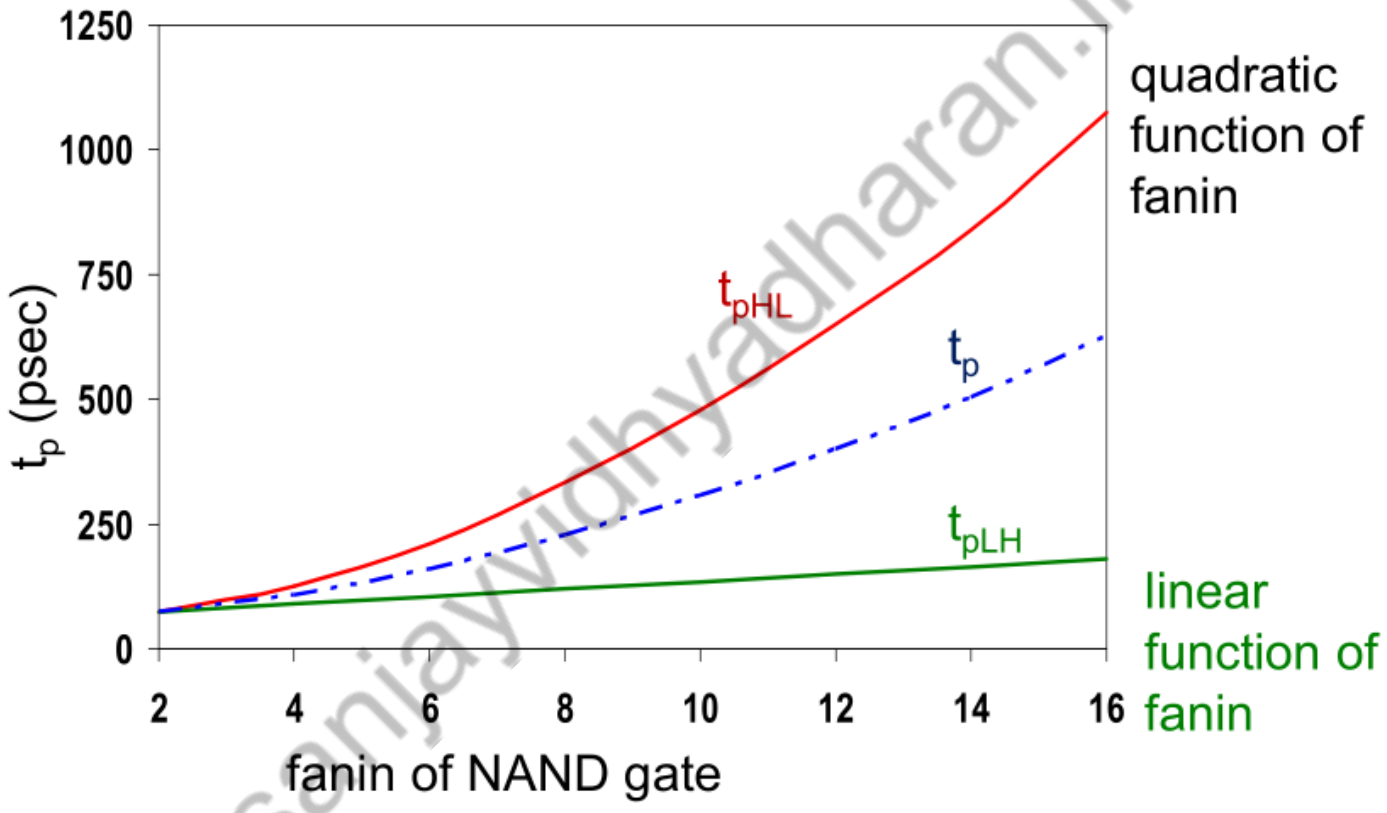
Distributed RC model
(Elmore delay)

$t_{pHL} = 0.69\ R_{eqn}(C_1+2C_2+3C_3+4C_L)$
(assuming all NMOS equally sized)

Propagation delay deteriorates rapidly as a function of fanin: quadratically in the worst case.

Transistor Sizing for a Complex Gate

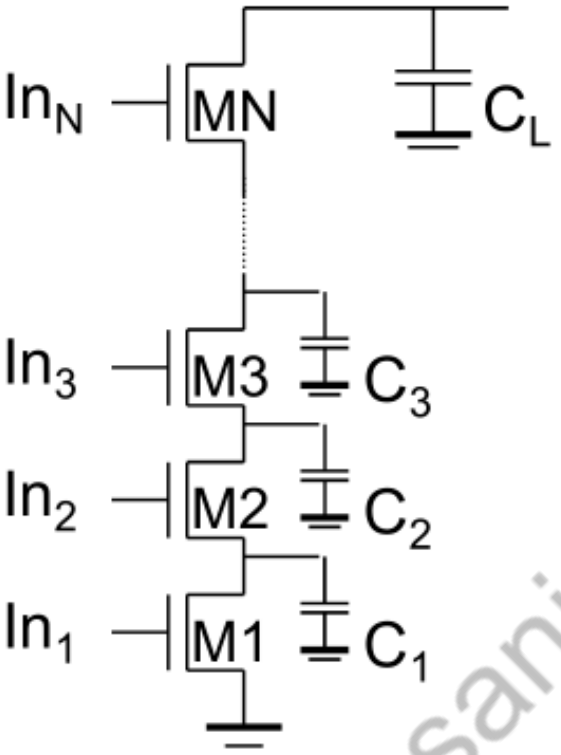
Propagation Delay as a function of fanin



Gates with a fan-in greater than 4 should be avoided.

Transistor Sizing for a Complex Gate

Design Technique 1 : Progressive sizing



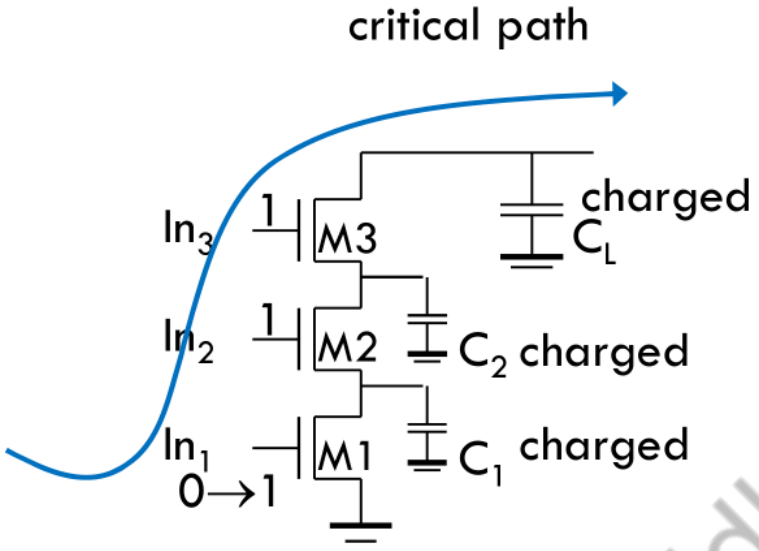
As long as fan-out capacitance dominates
M1(R1) appears N times in the delay equation,
the resistance of M2 (R2) appears N-1 times, etc.

The FET closest to the output should be the smallest
Can reduce delay by more than 20%;
decreasing gains as technology shrinks

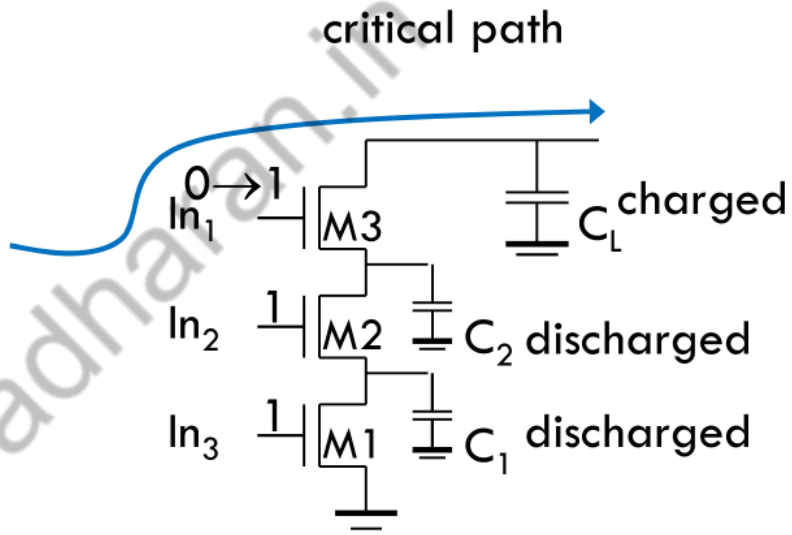
While progressive resizing of transistors is relatively easy in a schematic diagram, it is not as simple in a real layout.

Transistor Sizing for a Complex Gate

Design Technique 2 : Input re-ordering



delay determined by time to discharge C_L, C_1 and C_2

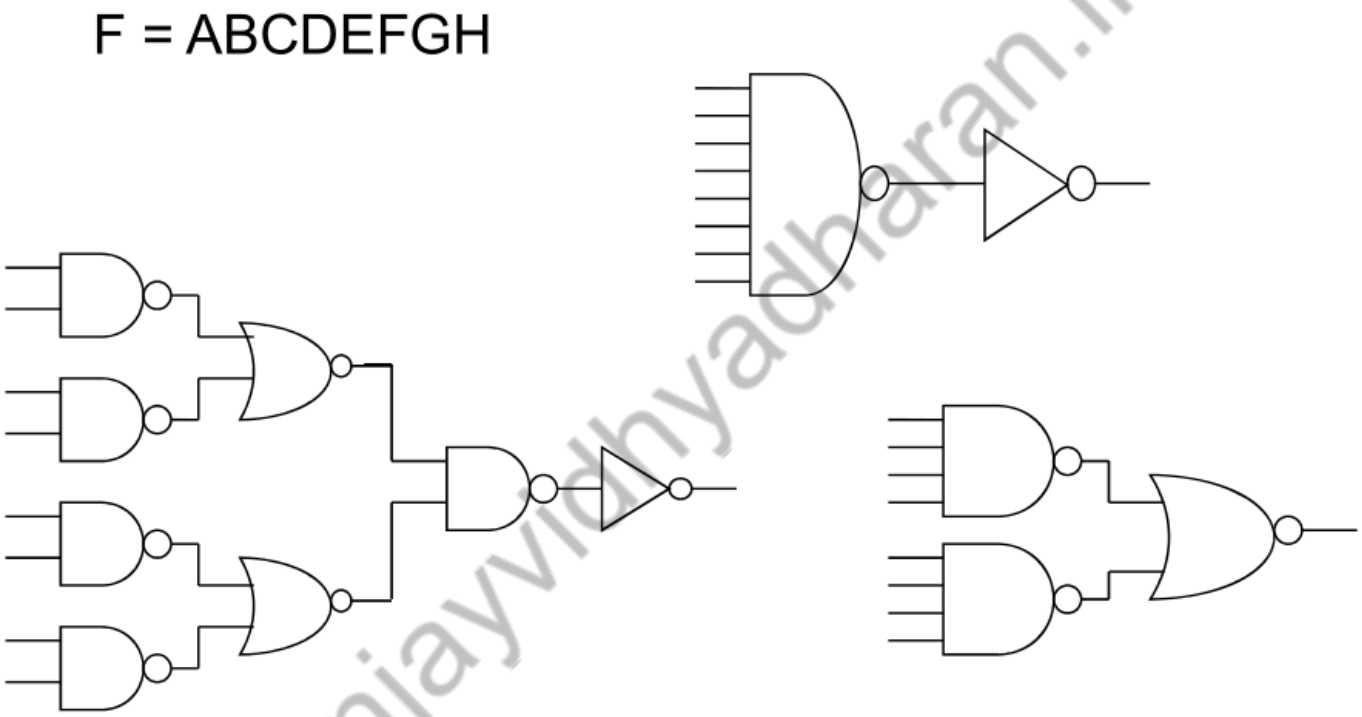


delay determined by time to discharge C_L

- An input signal to a gate is called critical if it is the last signal of all inputs to assume a stable value.
- The path through the logic which determines the ultimate speed of the structure is called the critical path.
- Putting the critical-path transistors closer to the output of the gate can result in a speed-up.

Transistor Sizing for a Complex Gate

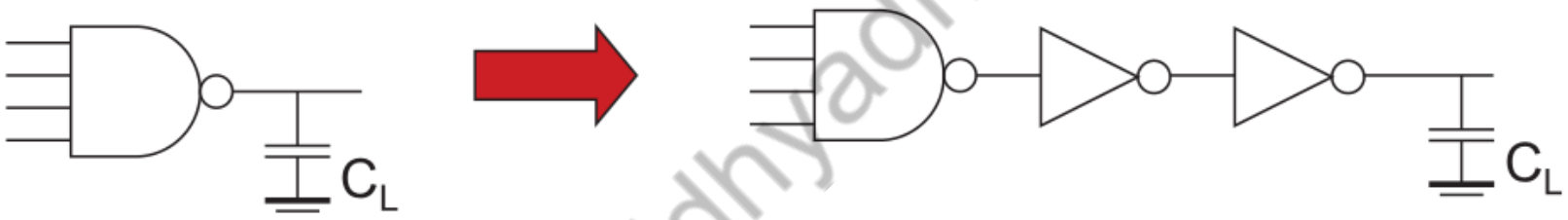
Design Technique 3 : Logic Restructuring



Manipulating the logic equations can reduce the fan-in requirements and hence reduce the gate delay

Transistor Sizing for a Complex Gate

Design Technique 4 : Isolating fan-in from fan-out using buffer insertion



Thank you