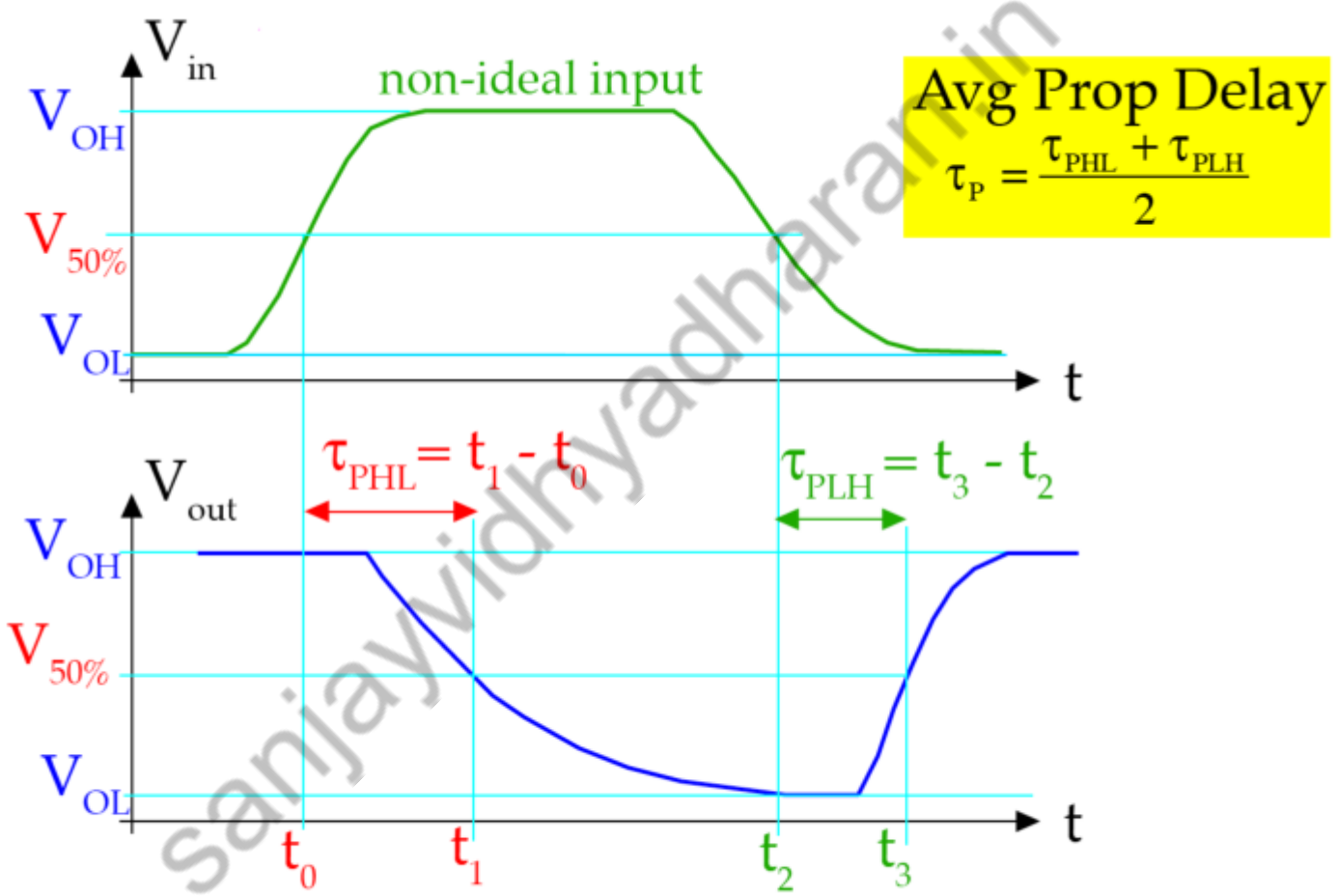
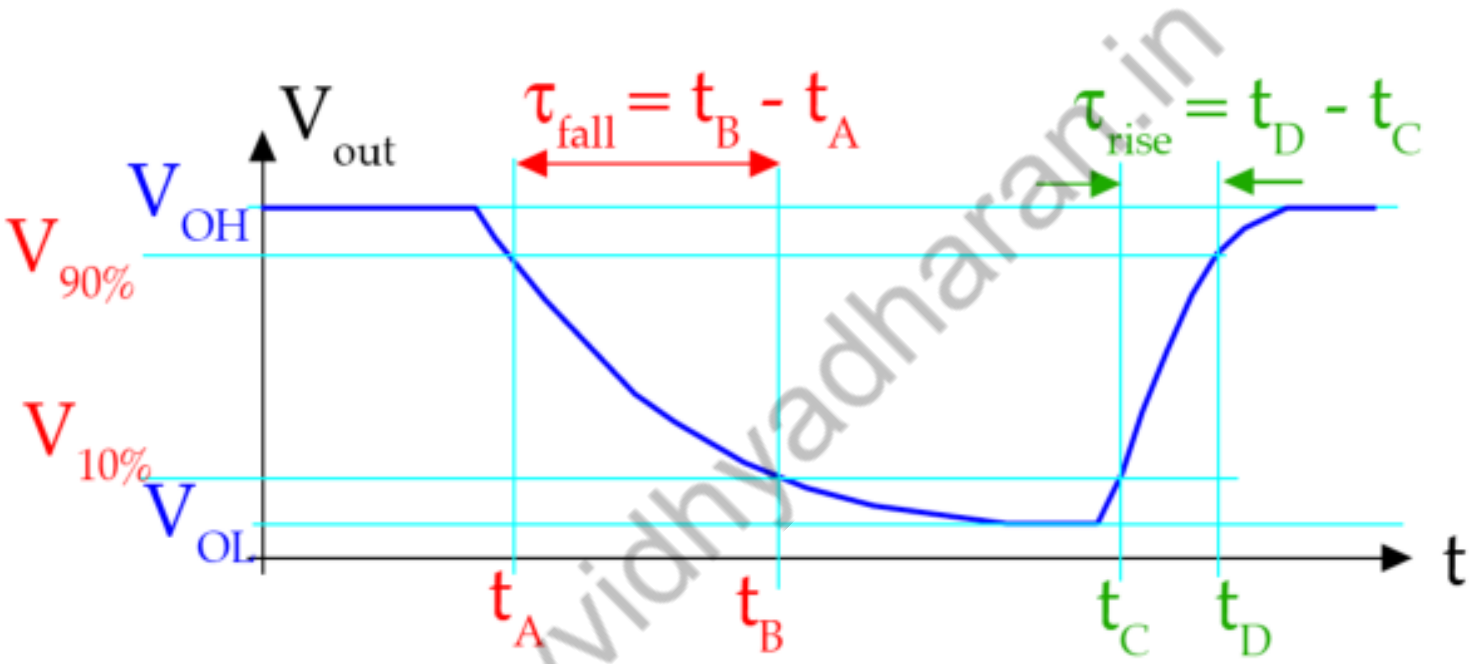
VLSI Design : 2021-22
Lecture 8
CMOS Inverter Transient Response

By Dr. Sanjay Vidhyadharan

CMOS Inverter: Transient Response



CMOS Inverter: Transient Response



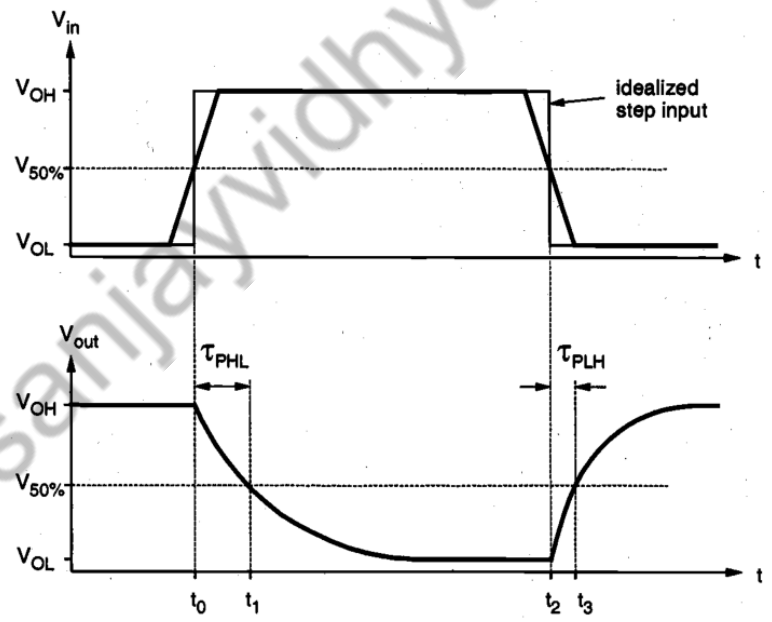
$$V_{10\%} = V_{OL} + 0.1\,[V_{OH} - V_{OL}]$$

$$V_{90\%} = V_{OL} + 0.9\,[V_{OH} - V_{OL}]$$

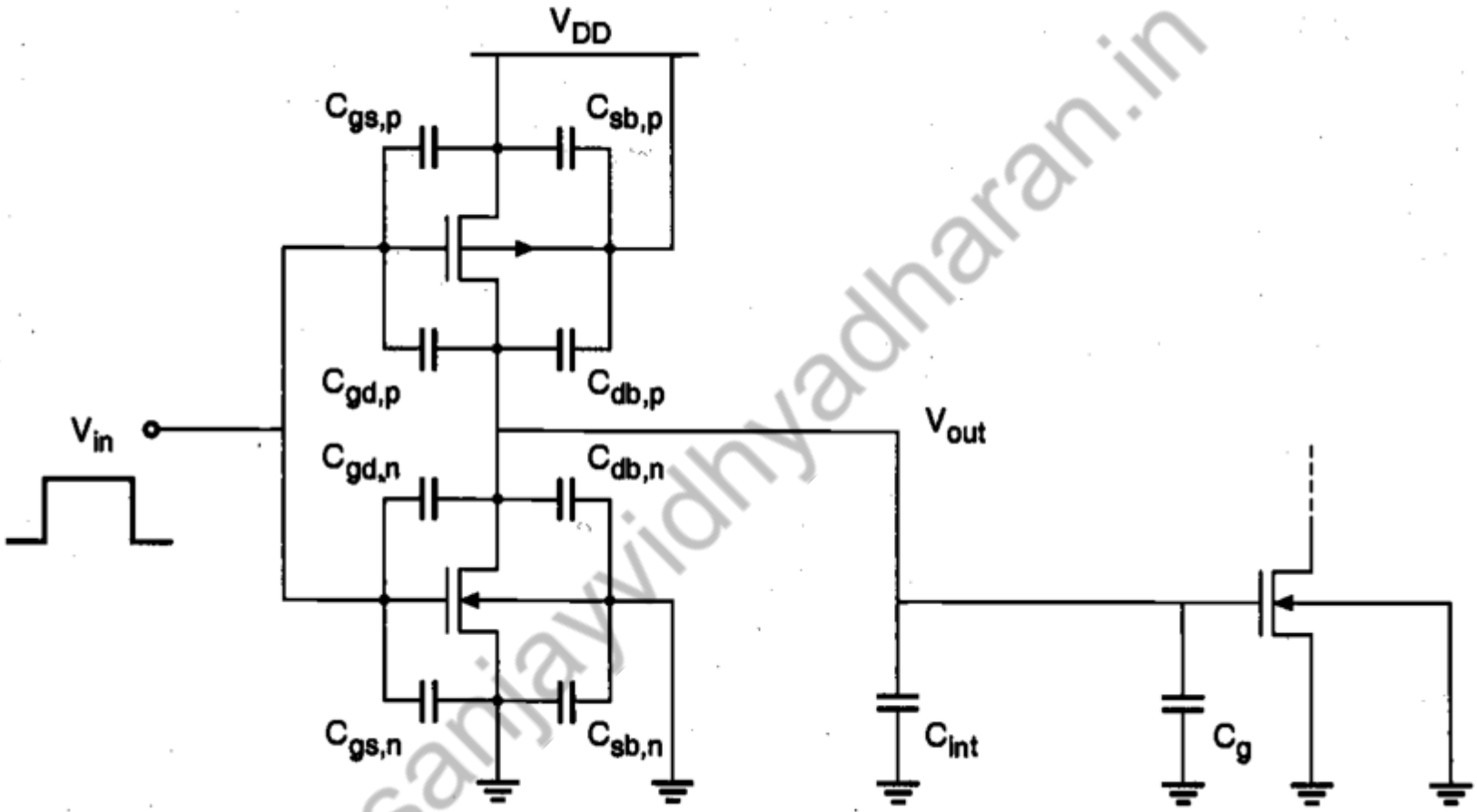
CMOS Inverter: Delay-Time Definitions

By definition, TP_{HL} is the time delay between the V50 %-transition of the rising input voltage and the V50%-transition of the falling output voltage. Similarly, TP_{LH} is defined as the time delay between the V50% -transition of the falling input voltage and the V50 %-transition of the rising output voltage.

To simplify the analysis and the derivation of delay expressions, the input voltage waveform is usually assumed to be an ideal step pulse with zero rise and fall times. Under this assumption,



CMOS Inverter: Transient Response



CMOS Inverter: Delay-Time Calculation

Three Methods

1. Average Current Model
2. Differential Equation Model
3. 1st Order RC delay Model

CMOS Inverter: Delay-Time Calculation

Average Current Model

$$c = \frac{q}{v} \gg i = \frac{dq}{dt} = c\frac{dv}{dt}$$

$$\tau_{PHL} = \frac{C_{load} \cdot \Delta V_{HL}}{I_{avg,HL}} = \frac{C_{load} \cdot (V_{OH} - V_{50\%})}{I_{avg,HL}}$$

$$\tau_{PLH} = \frac{C_{load} \cdot \Delta V_{LH}}{I_{avg,LH}} = \frac{C_{load} \cdot (V_{50\%} - V_{OL})}{I_{avg,LH}}$$

Note that the average current during high-to-low transition can be calculated by using the current values at the beginning and the end of the transition.

$$I_{avg,HL} = \frac{1}{2}\left[i_C(V_{in} = V_{OH}, V_{out} = V_{OH}) + i_C(V_{in} = V_{OH}, V_{out} = V_{50\%})\right]$$

$$I_D = \frac{k_n' W (V_{DD} - V_T)^2}{2L}$$

$$I_D = \frac{k_n' W (V_{ov} - \frac{V_{DS}}{2}) V_{DS}}{L}$$

$$I_D = \frac{k_n' W (V_{DD} - V_T - \frac{V_{DD}}{4}) \frac{V_{DD}}{2}}{L}$$

Similarly, the average capacitance current during low-to-high transition is

$$I_{avg,LH} = \frac{1}{2}\left[i_C(V_{in} = V_{OL}, V_{out} = V_{50\%}) + i_C(V_{in} = V_{OL}, V_{out} = V_{OL})\right]$$

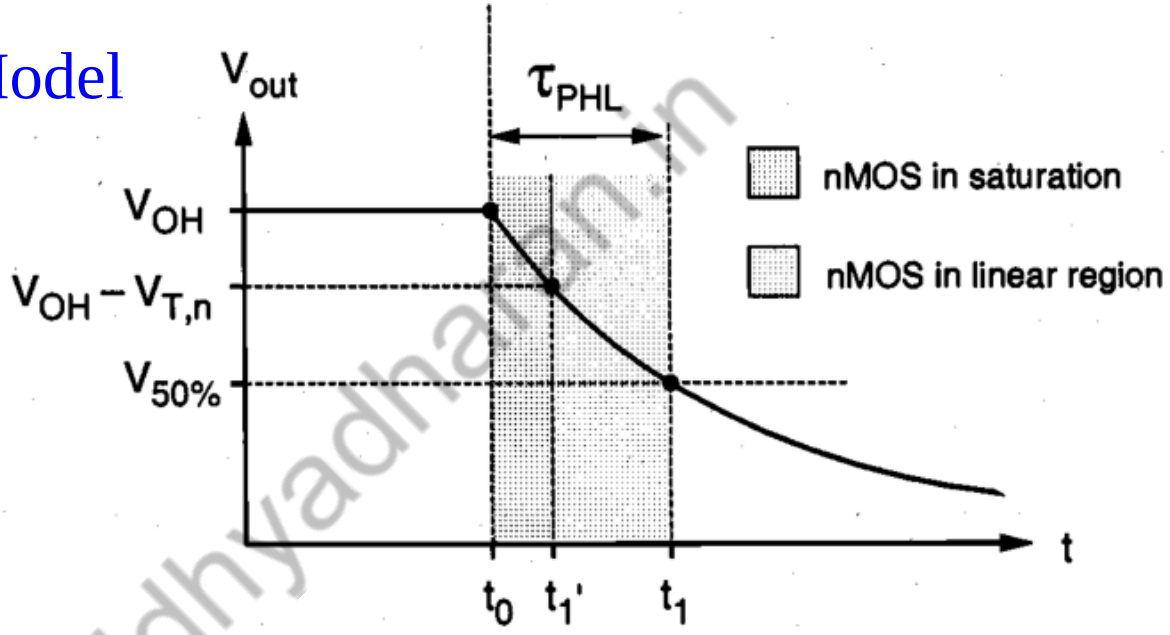
CMOS Inverter: Delay-Time Calculation

Differential Equation Model

$$C = \frac{Q}{V}$$

$$i = C\frac{dV}{dt}$$

$$dt = C\frac{dV}{i}$$



$$\int_{t=t_0}^{t=t_1'} dt = -C_{load} \int_{V_{out}=V_{OH}}^{V_{out}=V_{OH}-V_{T,n}} \left(\frac{1}{i_{D,n}}\right) dV_{out}$$

$$i_{D,n} = \frac{k_n}{2}\left(V_{in} - V_{T,n}\right)^2$$

$$= \frac{k_n}{2}\left(V_{OH} - V_{T,n}\right)^2,$$

$$t_1' - t_0 = \frac{2\,C_{load}\,V_{T,n}}{k_n\left(V_{OH} - V_{T,n}\right)^2}$$

CMOS Inverter: Delay-Time Calculation

Differential Equation Model

$$for \quad V_{out} \le V_{OH} - V_{T,n}$$

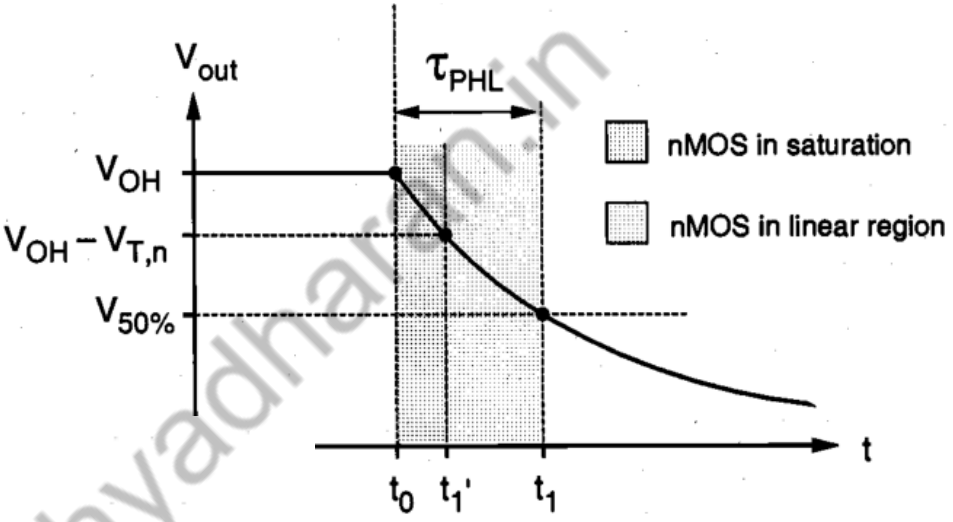
$$i_{D,n} = \frac{k_n}{2}\left[2\left(V_{in} - V_{T,n}\right)V_{out} - V_{out}^{\,2}\right]$$

$$= \frac{k_n}{2}\left[2\left(V_{OH} - V_{T,n}\right)V_{out} - V_{out}^{\,2}\right],$$

$$\int_{t=t_1'}^{t=t_1} dt = -C_{load} \int_{V_{out}=V_{OH}-V_{T,n}}^{V_{out}=V_{50\%}} \left(\frac{1}{i_{D,n}}\right) dV_{out}$$

$$= -2\,C_{load} \int_{V_{out}=V_{OH}-V_{T,n}}^{V_{out}=V_{50\%}} \left(\frac{1}{k_n\left[2\left(V_{OH} - V_{T,n}\right)V_{out} - V_{out}^2\right]}\right) dV_{out}$$

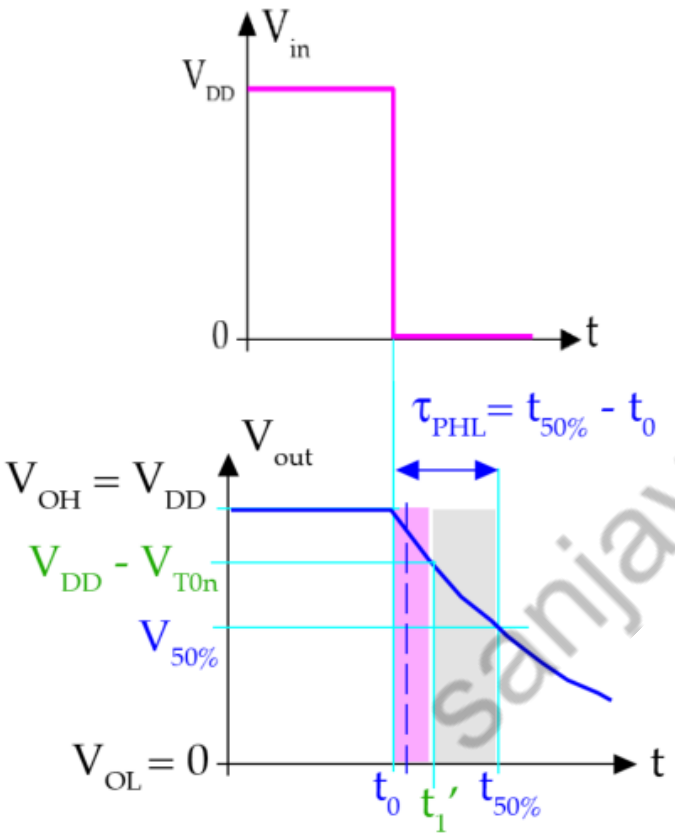
$$t_1 - t_1' = -\frac{2\,C_{load}}{k_n} \frac{1}{2\left(V_{OH} - V_{T,n}\right)} \ln\left(\frac{V_{out}}{2\left(V_{OH} - V_{T,n}\right) - V_{out}}\right)\Bigg|_{V_{out}=V_{OH}-V_{T,n}}^{V_{out}=V_{50\%}}$$



CMOS Inverter: Delay-Time Calculation

Differential Equation Model

Approximate by assuming in saturation:



$$\tau_{PHL} \approx C_{load} \int_{V_{DD}}^{V_{DD}/2} \left(\frac{-1}{i_{Dn,sat}} \right) dV_{out} = \int_{V_{DD}}^{V_{DD}/2} \left(\frac{-C_{load}}{\frac{k_n}{2}(V_{DD} - V_{T0n})^2} \right) dV_{out}$$

$$\tau_{PHL} \approx \frac{C_{load} V_{DD}}{k_n (V_{DD} - V_{T0n})^2} \propto R_n C_{load}$$

Δ is less than 10%

CMOS Inverter: Delay-Time Calculation

Differential Equation Model

Taking Velocity saturation into consideration

$$\tau_{PHL} \approx C_{load} \int_{V_{DD}}^{V_{DD}/2} \left(\frac{-1}{i_{Dn,vsat}} \right) dV_{out}$$

$$V_{dsat} \approx \frac{Lv_{sat}}{\mu_n}$$

$$= \int_{V_{DD}}^{V_{DD}/2} \left(\frac{-C_{load}}{v_{sat} C_{OX} W \left[V_{DD} - V_{T0n} - \frac{V_{dsat}}{2} \right]} \right) dV_{out}$$

$$\tau_{PHL} \approx \frac{C_{load} V_{DD}}{2 v_{sat} C_{OX} W \left(V_{DD} - V_{T0n} - \frac{V_{dsat}}{2} \right)} \propto R_n C_{load}$$

CMOS Inverter: Transient Response

1st Order RC delay Model

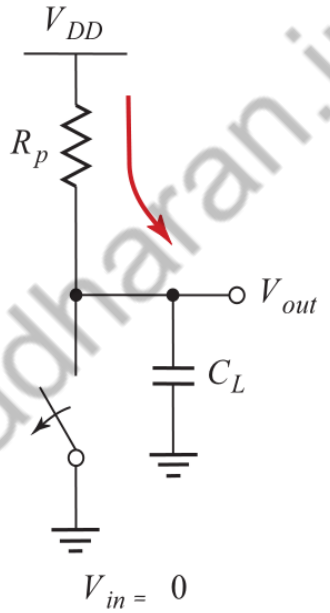
$$V_1(t) = V_{DD}(1 - e^{-t/R_pC_{load}})$$

$$V_{50\%} = \frac{V_{DD}}{2} = V_{DD}(1 - e^{-\tau_{PLH}/R_pC_{load}})$$

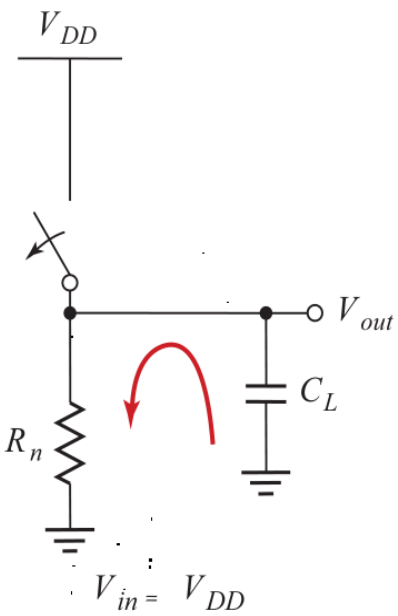
$$\frac{1}{2} = e^{-\tau_{PLH}/R_pC_{load}}$$

$$\ln\frac{1}{2} = -\frac{\tau_{PLH}}{R_pC_{load}}$$

$$\tau_{PLH} = \ln(2)R_pC_{load} \approx 0.69R_pC_{load}$$



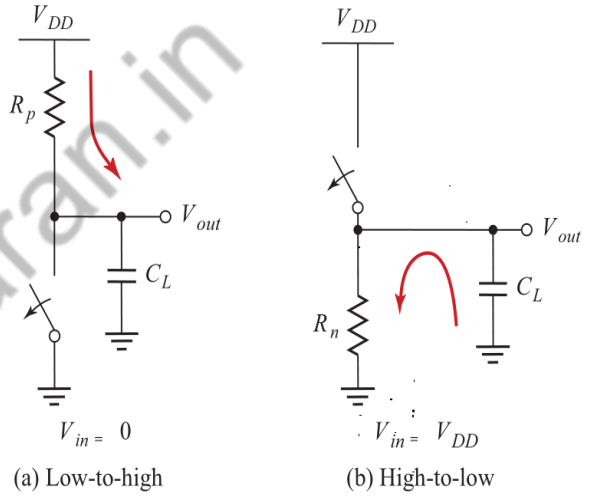
(a) Low-to-high



(b) High-to-low

CMOS Inverter: Transient Response

1st Order RC delay Model



(a) Low-to-high (b) High-to-low

Empirical values have been found for R_N and R_P,

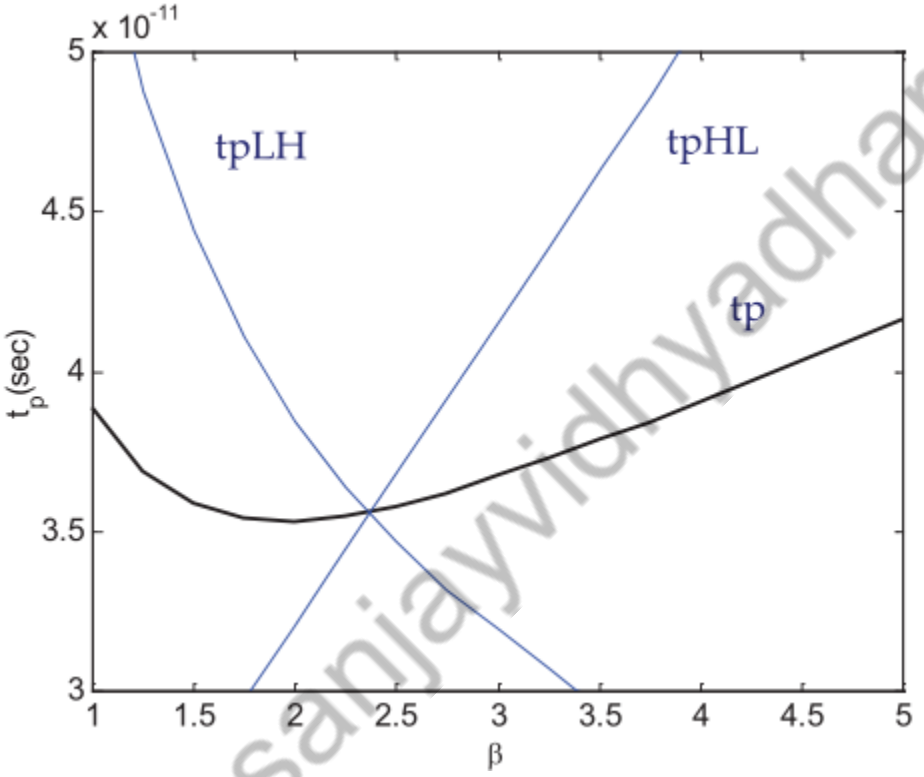
$$R_N = \frac{12.5}{(W/L)_n} \text{ k}\Omega$$

$$R_P = \frac{30}{(W/L)_p} \text{ k}\Omega$$

Furthermore, it has been found that these values apply for a number of CMOS fabrication processes including 0.25 μm, 0.18 μm, and 0.13 μm (see Hodges et al., 2004).

Sizing of CMOS Inverter

Increase PMOS size -> improve tp_{LH} but degrades tp_{HL} !!



However delays are identical @ β = 2.4

Sizing of CMOS Inverter

$$t_p = 0.69 R_{eq}(C_{int} + C_{ext})$$
$$= 0.69 R_{eq} C_{int}(1 + C_{ext}/C_{int}) = t_{p0}(1 + C_{ext}/C_{int})$$

$t_{p0} = 0.69\ R_{eq}C_{int}$ represents the delay of the inverter only loaded by its own intrinsic capacitance ($C_{ext} = 0$), and is called the *intrinsic or unloaded delay*.

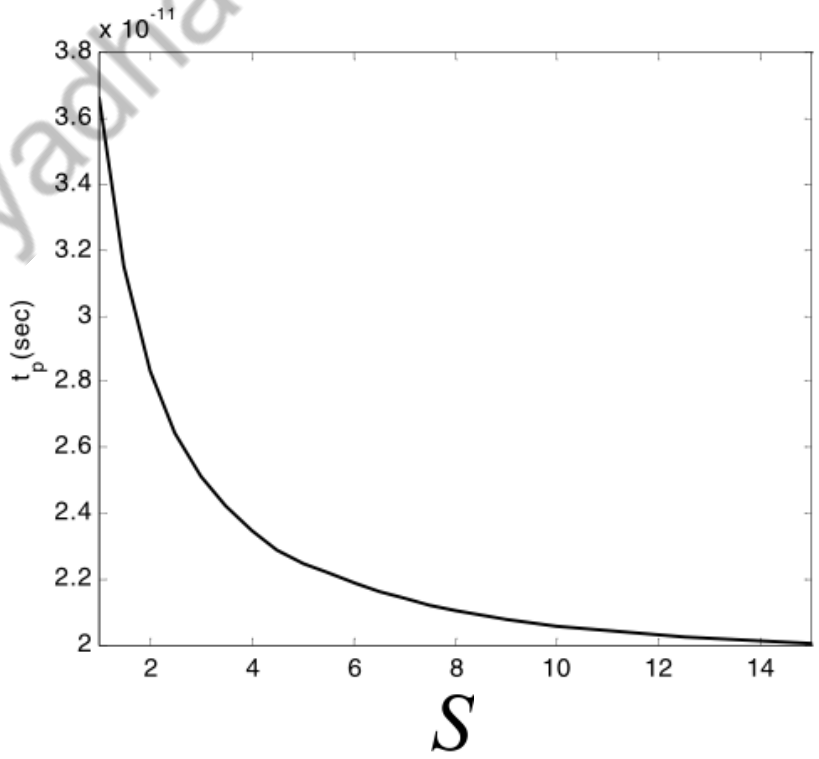
- The intrinsic delay of the inverter tp0 is independent of the sizing of the gate, and is purely determined by technology and inverter layout.
- When no load is present, an increase in the drive of the gate is totally offset by the increased capacitance.

Sizing of CMOS Inverter

$$t_p = 0.69 R_{eq}(C_{int} + C_{ext})$$
$$= 0.69 R_{eq} C_{int}(1 + C_{ext}/C_{int}) = t_{p0}(1 + C_{ext}/C_{int})$$

$$C_{int} = S\, C_{ext}$$

- Making S infinitely large yields the maximum obtainable performance gain, eliminating the impact of any external load, and reducing the delay to the intrinsic one.
- Yet, any sizing factor S that is sufficiently larger than (Cext /Cint) produces similar results at a substantial gain in silicon area.



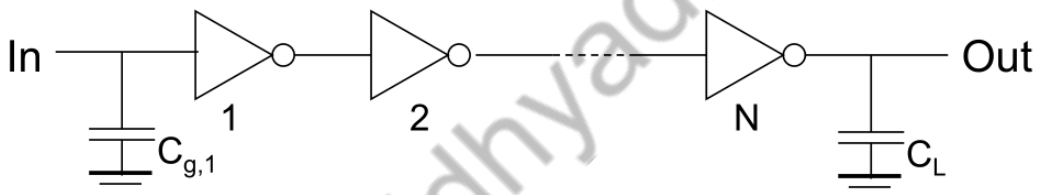
Sizing of CMOS Chain of Inverters

$$C_{int} = \gamma C_g$$

γ is a proportionality factor, which is only a function of technology and is close to 1 for most sub-micron processes.

$$t_p = t_{p0}\left(1 + \frac{C_{ext}}{\gamma C_g}\right) = t_{p0}(1 + f/\gamma)$$

$f = C_{ext}/C_g$



the delay of the j-th inverter stage is

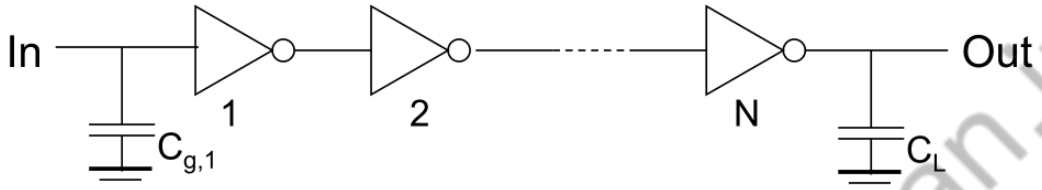
$$t_{p,j} = t_{p0}\,(1 + C_{g,j+1}/(\gamma C_{g,j})) = t_{p0}(1 + f_j/\gamma)$$

and $t_p = t_{p1} + t_{p2} + \ldots + t_{pN}$

so $t_p = \Sigma t_{p,j} = t_{p0} \Sigma\,(1 + C_{g,j+1}/(\gamma C_{g,j}))$

- If C_L is given
  - How should the inverters be sized?
  - How many stages are needed to minimize the delay?

Sizing of CMOS Chain of Inverters



The optimum size of each inverter is the geometric mean of its neighbours – meaning that if each inverter is sized up by the same factor f wrt the preceding gate, it will have the same effective fan-out and the same delay

$$f = \sqrt[N]{C_L/C_{g,1}} = \sqrt[N]{F}$$

where the overall effective fan-out of the circuit is

$$F = C_L/C_{g,1}$$

and the minimum delay through the inverter chain is

$$t_p = N\, t_{p0}\, (1 + (\sqrt[N]{F}) / \gamma)$$

- The relationship between t_p and F is linear for one inverter, square root for two, etc.

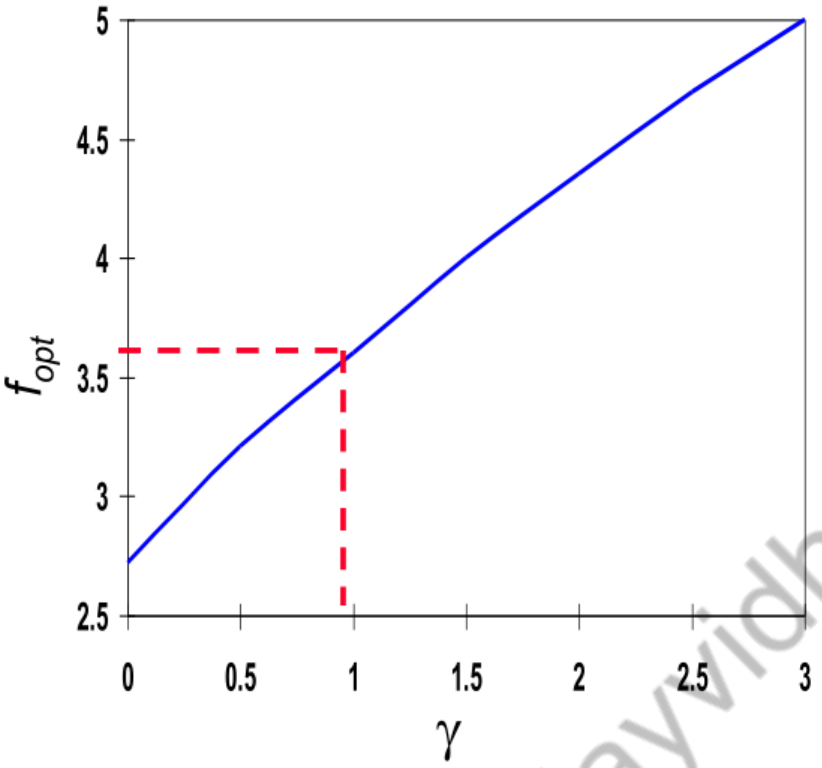
Sizing of CMOS Chain of Inverters

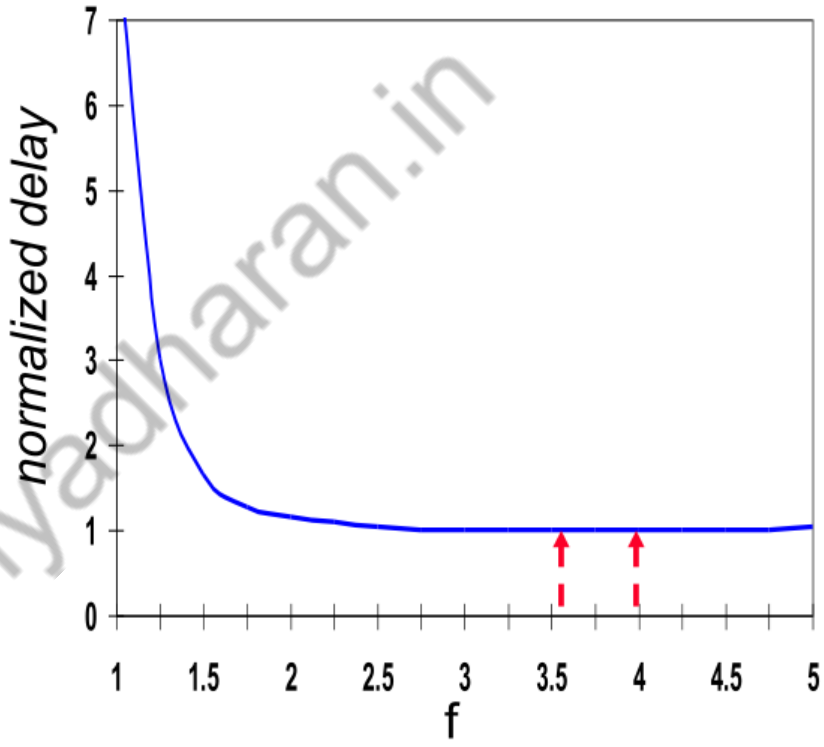
- What is the optimal value for N given F (= f^N) ?
  - if the number of stages is too large, the intrinsic delay of the stages becomes dominate
  - if the number of stages is too small, the effective fan-out of each stage becomes dominate
- The *optimum* N is found by differentiating the minimum delay expression divided by the number of stages and setting the result to 0, giving

$$\gamma + \sqrt[N]{F} - (\sqrt[N]{F} \ln(F))/N = 0 \quad \text{and} \quad f = e^{(1 + \gamma/f)}$$

- For $\gamma = 0$ (ignoring self-loading) $N = \ln(F)$
  and the effective-fan out (tapering factor) is $f = e = 2.718$
- For $\gamma = 1$ (the typical case) $N = \ln(F) - 1$
  and the effective fan-out (tapering factor) is $f = 3.6$

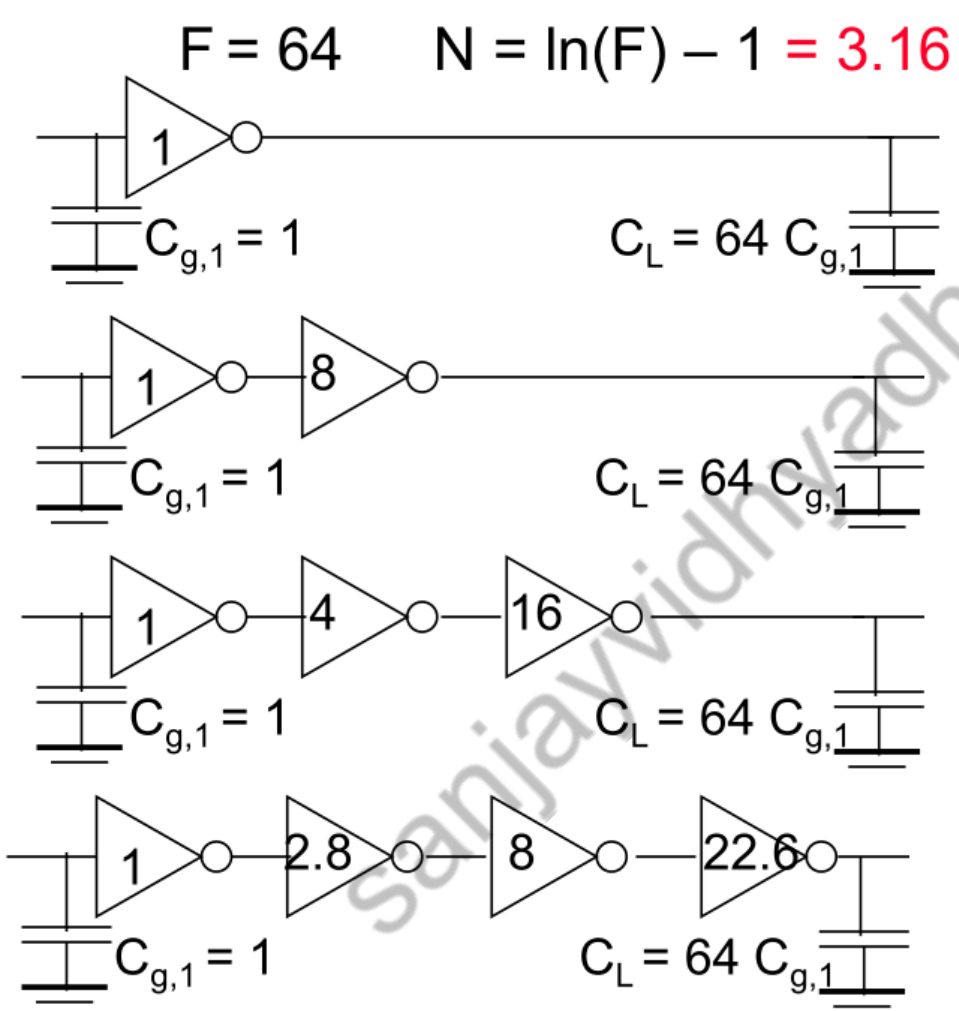
Sizing of CMOS Chain of Inverters





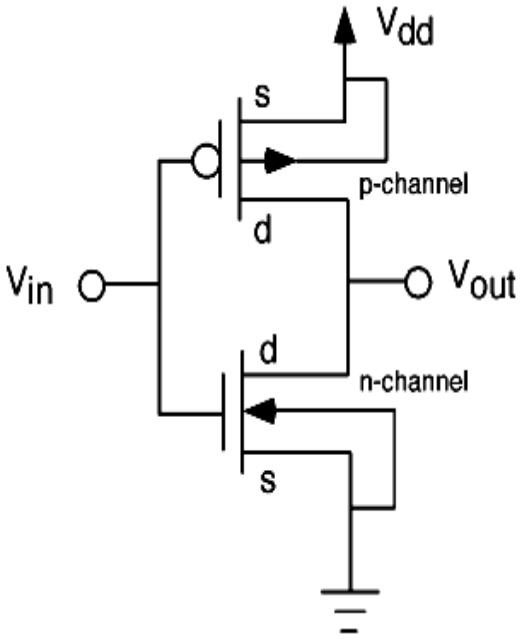
- Choosing f larger than optimum has little effect on delay and reduces the number of stages (and area).
  - So it is common practice to use f = 4 (for γ = 1) and reduce N
  - Too many stages has a substantial negative impact on delay

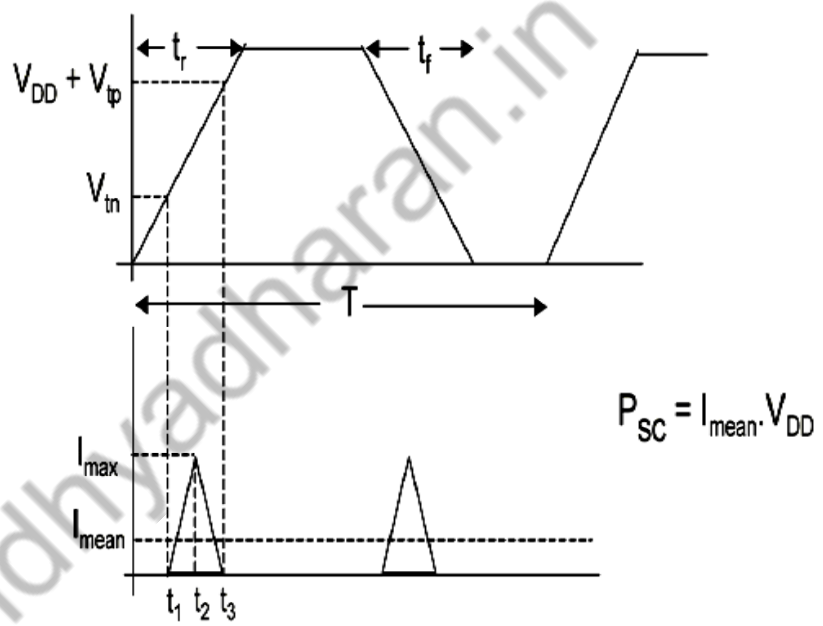
Sizing of CMOS Chain of Inverters



N	f	t_p
1	64	65
2	8	18
3	4	15
4	2.8	15.3

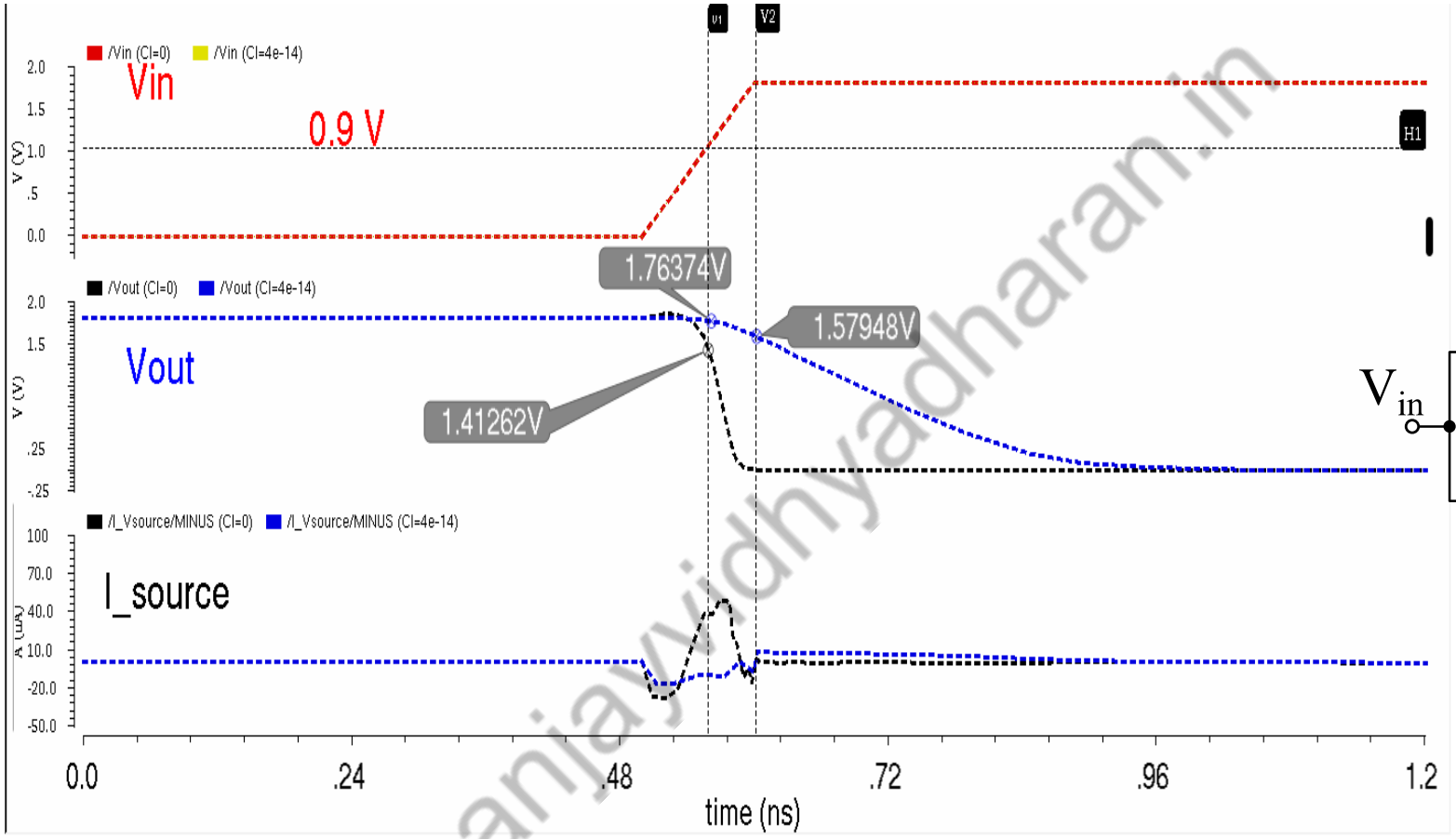
Short Circuit Loss

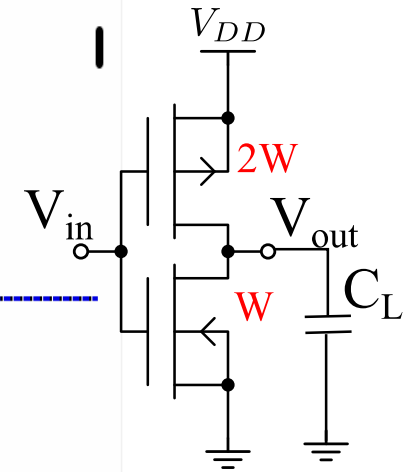




- Use devices with V_{th} close to $\frac{V_{DD}}{2}$ & steep switching characteristics
- Short Circuit loss reduces with C_{load}

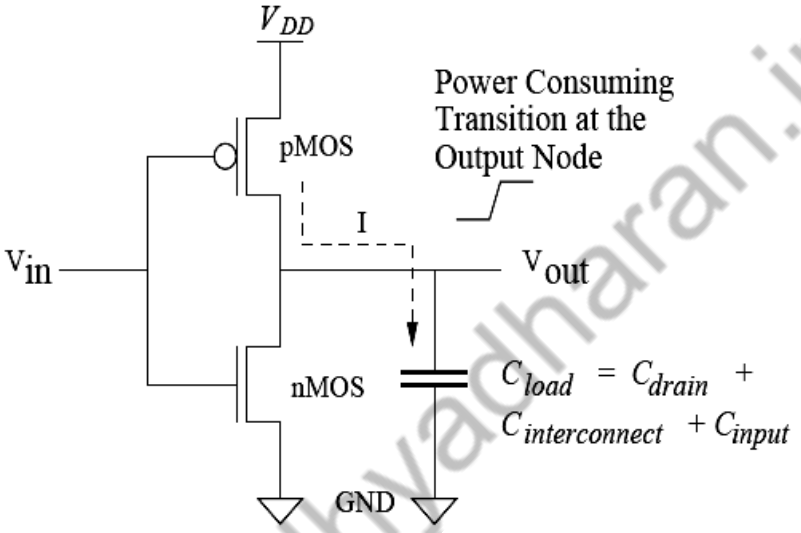
Short Circuit Loss





- Short Circuit loss reduces with C_{load}

Switching Loss



Energy stored in C_{Load} $(C_L) = \int_0^{V_{DD}} V_C \, C_L dV_c = \frac{1}{2}.V_{DD}^2 * C_L$

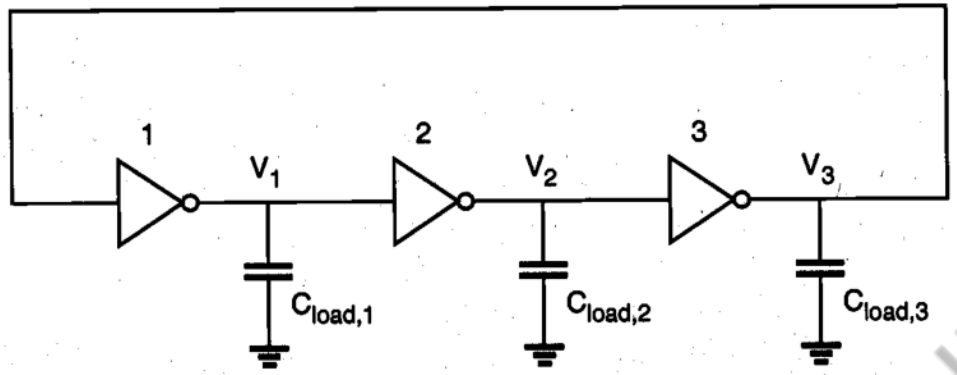
Energy consumed from power supply= $V_{DD} \int_0^T i(t)dt = V_{DD}.Q_{CL} = V_{DD}^2.C_L$

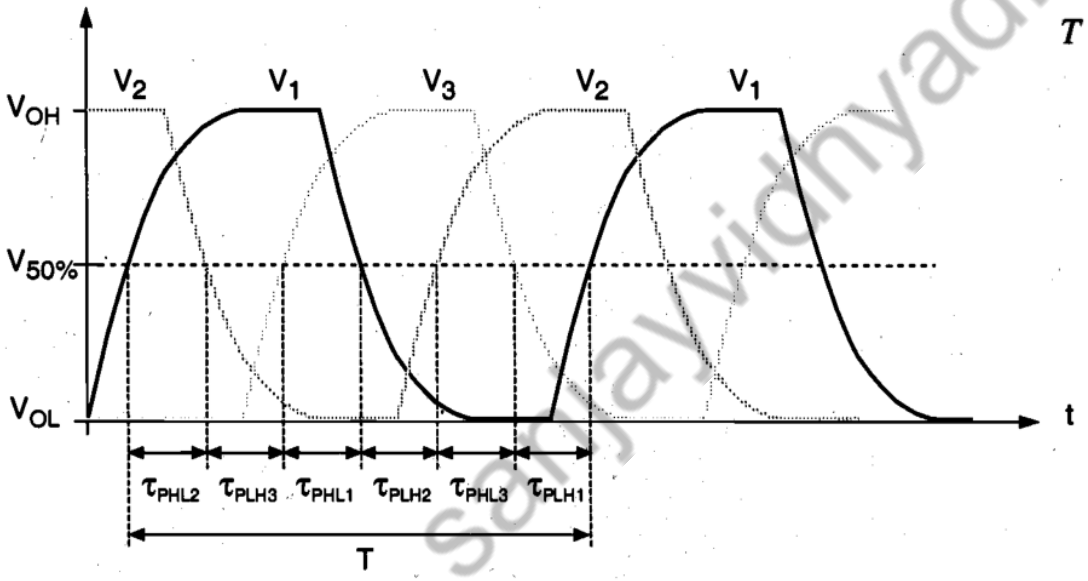
Energy dissipated in pMOSFET during charging = $\frac{1}{2}.V_{DD}^2.C_L$

Energy dissipated in nMOSFET during discharging = $\frac{1}{2}.V_{DD}^2.C_L$

Power Consumption = Frequency. $V_{DD}^2.C_L$

Ring Oscillator Circuit





$$T = \tau_{PHL1} + \tau_{PLH1} + \tau_{PHL2} + \tau_{PLH2} + \tau_{PHL3} + \tau_{PLH3}$$
$$= 2\tau_P + 2\tau_P + 2\tau_P$$
$$= 3 \cdot 2\tau_P = 6\tau_P$$

$$f = \frac{1}{T} = \frac{1}{2 \cdot n \cdot \tau_P}$$

- The ring oscillator circuit can be used as a very simple pulse generator
- Utilized to characterize a particular design and/or a new fabrication process.

Thank you