VLSI Design : 2021-22
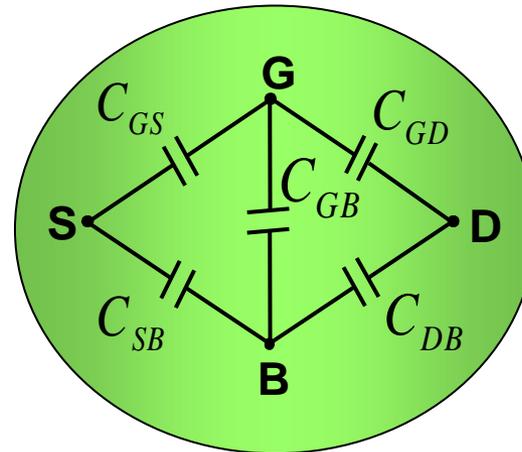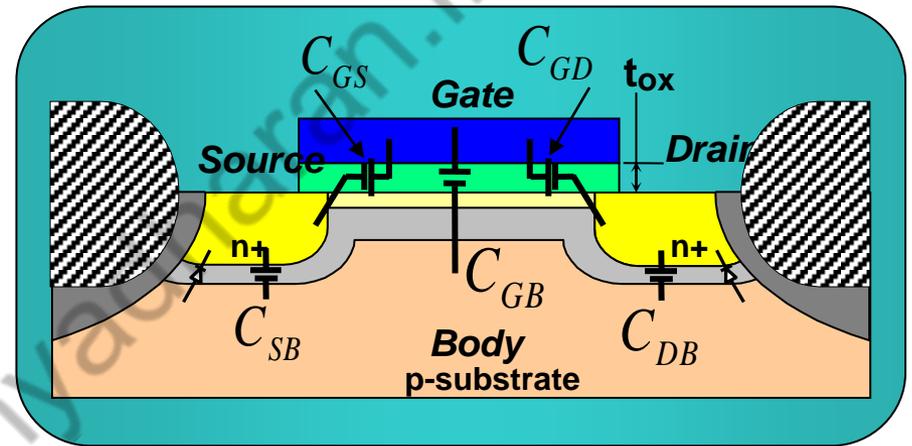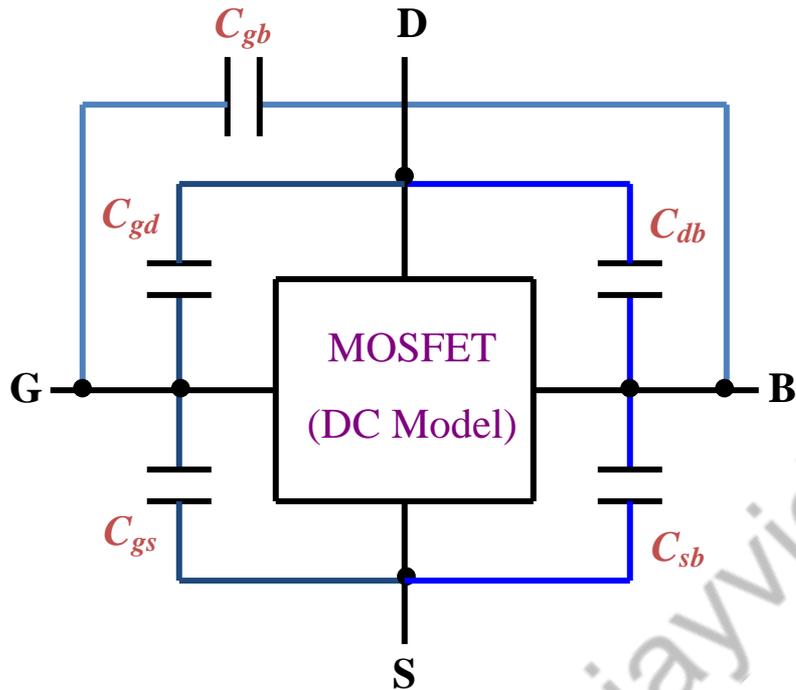# Lecture 7
MOS Capacitance

By Dr. Sanjay Vidhyadharan

MOSFET Junction Capacitances

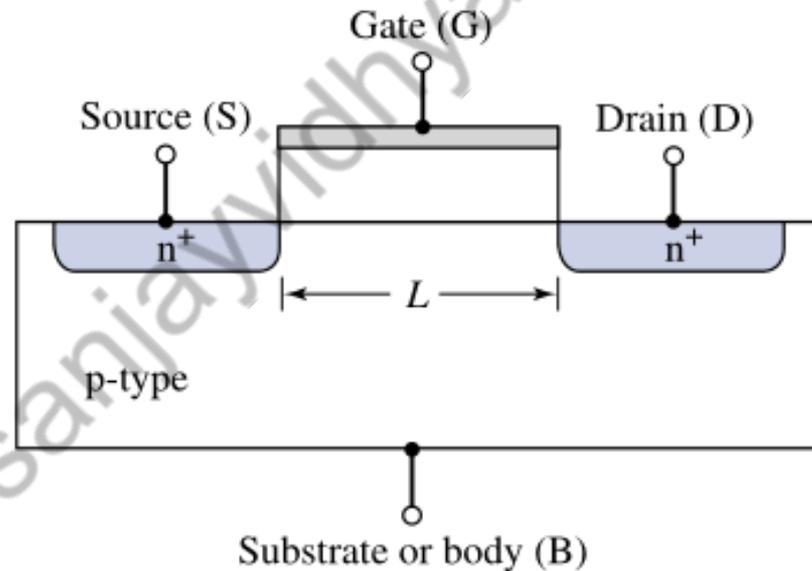# MOSFET Gate Capacitances

Cutoff

– No channel formation => $C_{gs} = C_{gd} = 0$. The gate capacitance to the substrate
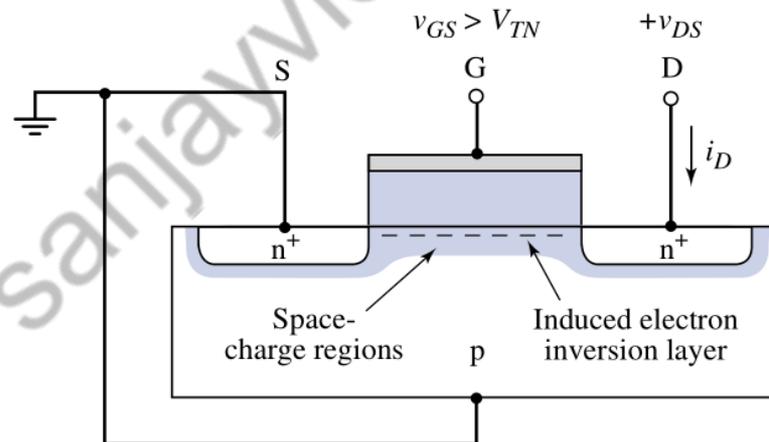
$$C_{gb} = C_{ox}\, W\, L$$

MOSFET Gate Capacitances

Linear

The channel has formed and the capacitance is from the gate to the source and drain, **not** to the substrate. Thus $C_{gb}=0$ and

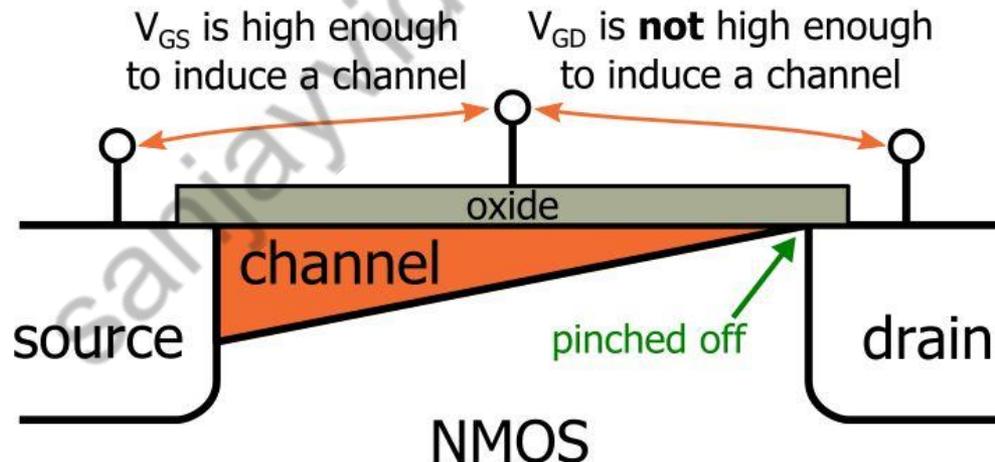$$C_{gs} \approx C_{gd} \approx (C_{ox}\ W\ L)/2$$

$v_{GS} > V_{TN}$ $+v_{DS}$

S   G   D

i_D

n$^+$ n$^+$

Space-charge regions   Induced electron inversion layer

p

MOSFET Gate Capacitances

Saturation
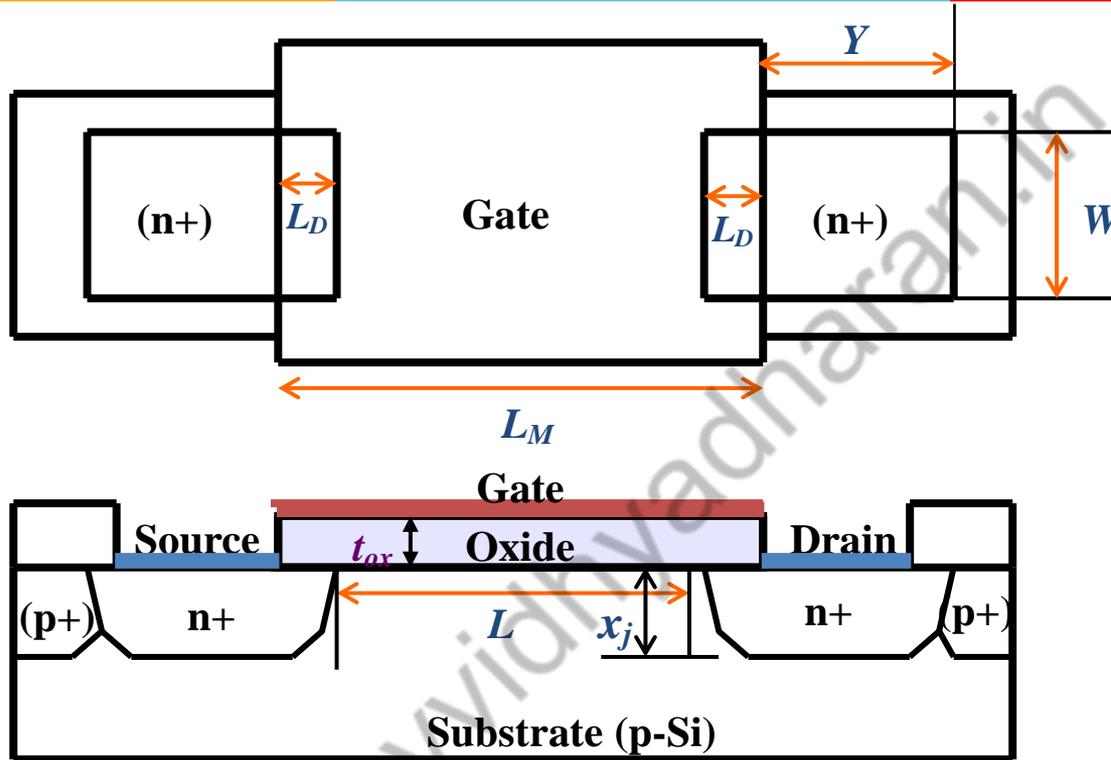
In saturation, the channel does not extend to the drain. Thus, $C_{gd}=0$ and

$$C_{gs} \approx (C_{ox} \, W \, L) * 2/3$$

V_{GS} is high enough to induce a channel V_{GD} is **not** high enough to induce a channel

oxide

channel

source   pinched off   drain

NMOS

MOSFET Overlap Capacitances

- L_M: mask length of the gate
- L: actual channel length
- L_D: gate-drain overlap
- Y: typical diffusion length
- W: length of the source and drain diffusion region

MOSFET Overlap Capacitances

Overlap Capacitances

– Two special components of C_{gs} and C_{gd} caused by the lateral diffusion under the gate and thin oxide

$$C_{GS(overlap)} = C_{ox}WL_D$$

$$C_{GD(overlap)} = C_{ox}WL_D$$

L_D: lateral diffusion length

W : the width of channel

$C_{ox} = \varepsilon_{ox}/t_{ox}$: capacitance per unit area

– Theses overlap capacitances are *bias independent* and are added components of C_{gs} and C_{gd}.
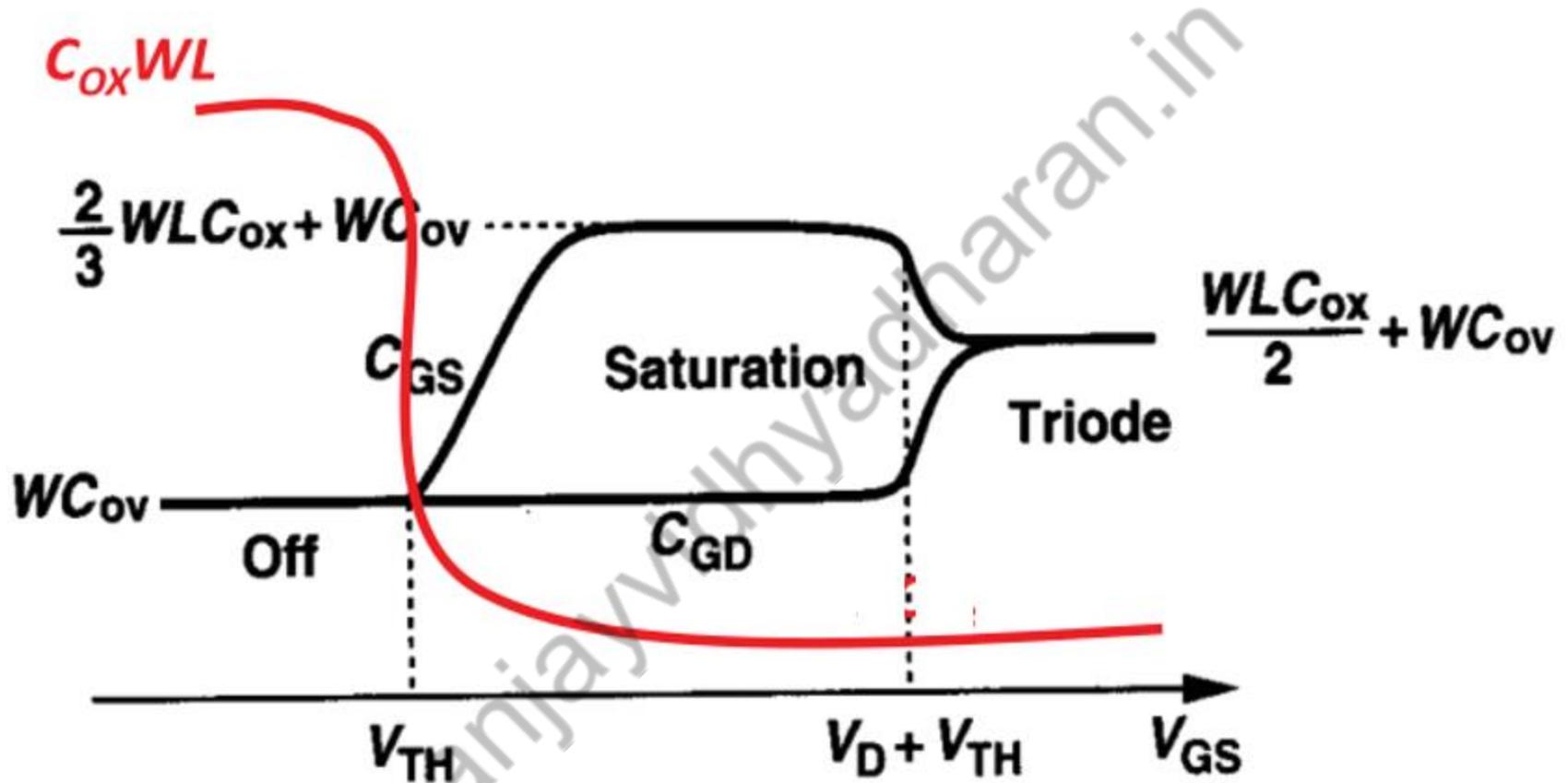
MOSFET Gate Capacitances

Note that the capacitance seen looking into the gate is C_g:

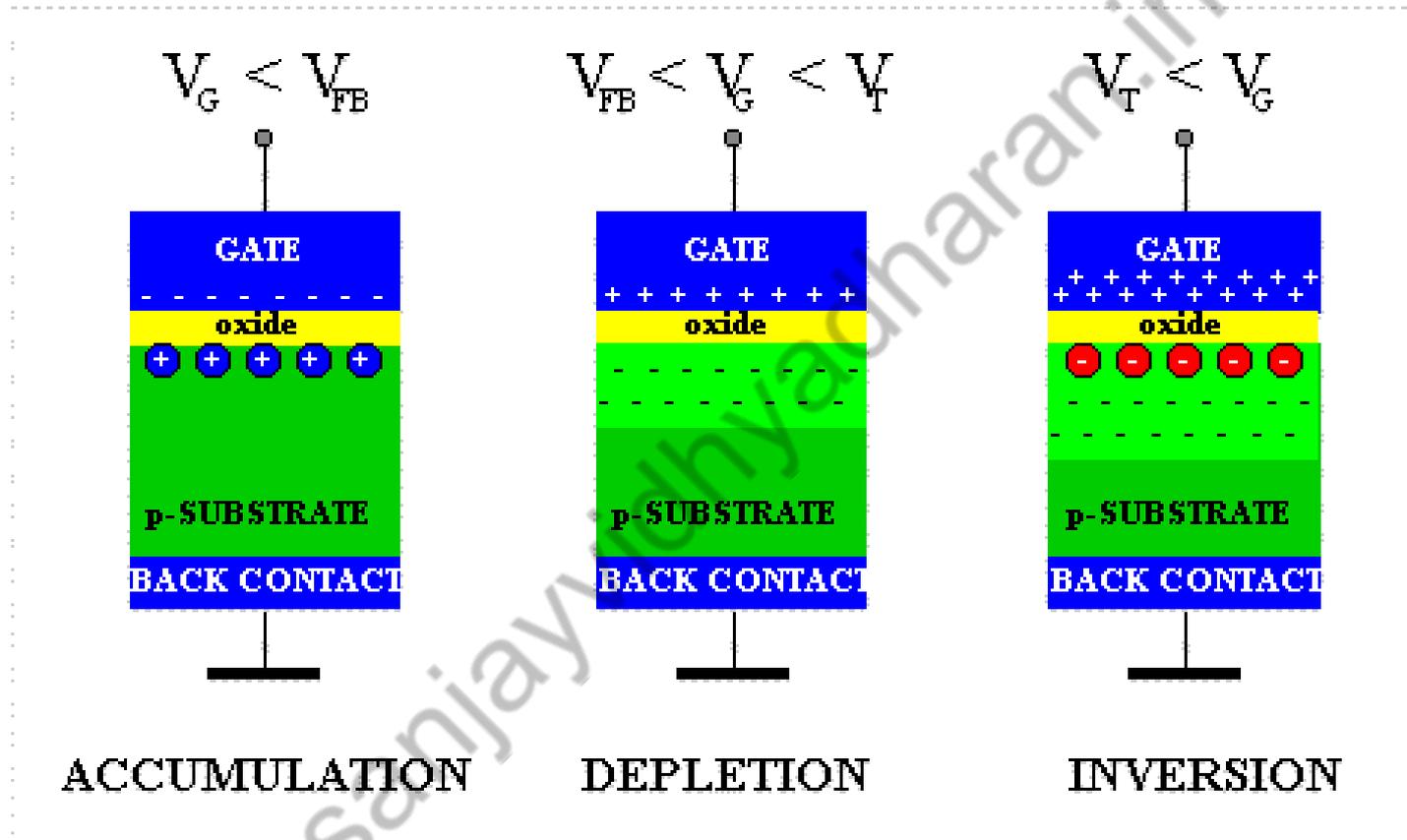– For manual calculations, we approximate C_g as its maximum value.

Capacitance	Cut-off	Linear	Saturation
C_{gb}(total)	$C_{ox}WL$	0	0
C_{gd}(total)	$C_{ox}WL_D$	$C_{ox}WL/2 + C_{ox}WL_D$	$C_{ox}WL_D$
C_{gs}(total)	$C_{ox}WL_D$	$C_{ox}WL/2 + C_{ox}WL_D$	$2C_{ox}WL/3 + C_{ox}WL_D$

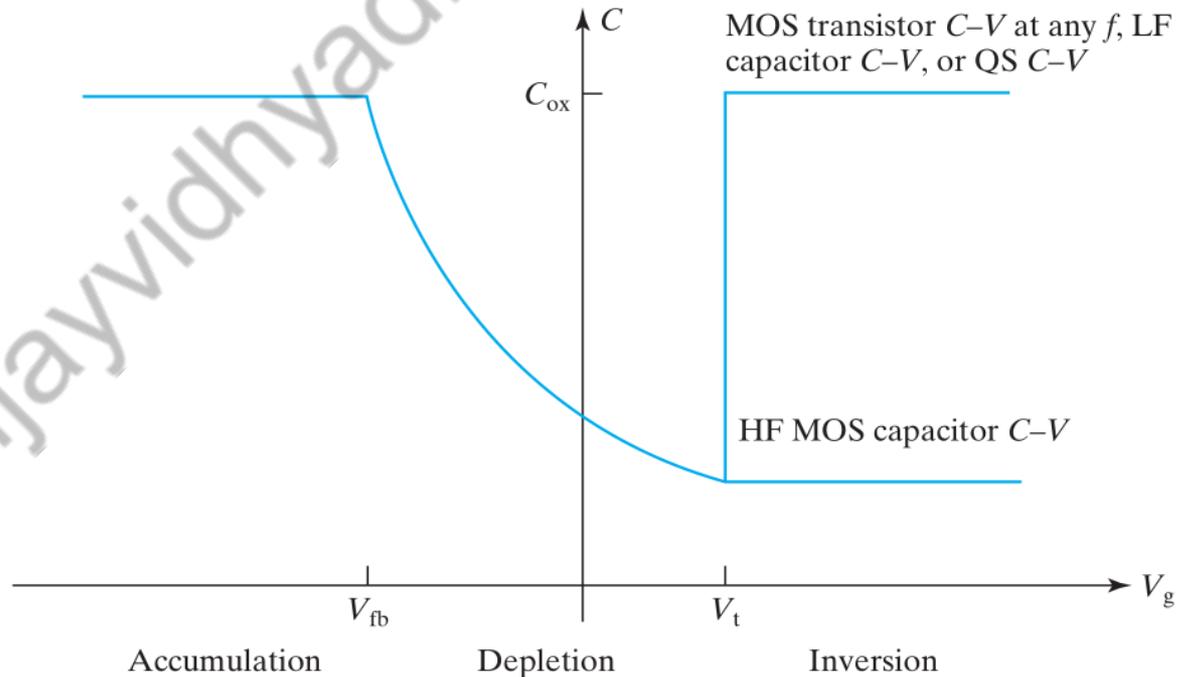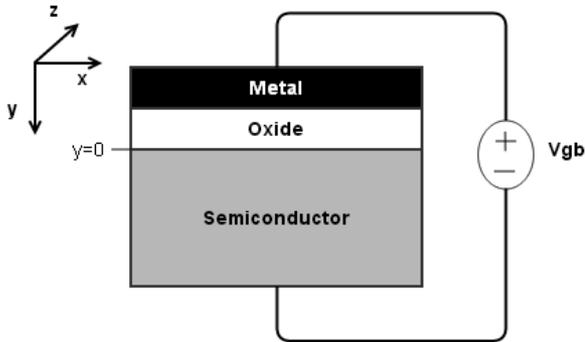– This component of input capacitance is directly proportional to L and W

MOSFET Gate Capacitances

MOS Capacitor

$$V_G < V_{FB}$$

GATE

oxide

p-SUBSTRATE

BACK CONTACT

ACCUMULATION

$$V_{FB} < V_G < V_T$$

GATE

oxide

p-SUBSTRATE

BACK CONTACT

DEPLETION

$$V_T < V_G$$

GATE

oxide

p-SUBSTRATE

BACK CONTACT

INVERSION

MOS Capacitor

MOS Capacitor based LNA

Thank you