Advanced VLSI Design: 2021-22
Lecture 4 - Part 2
Pipelined Registers and Static Timing Analysis

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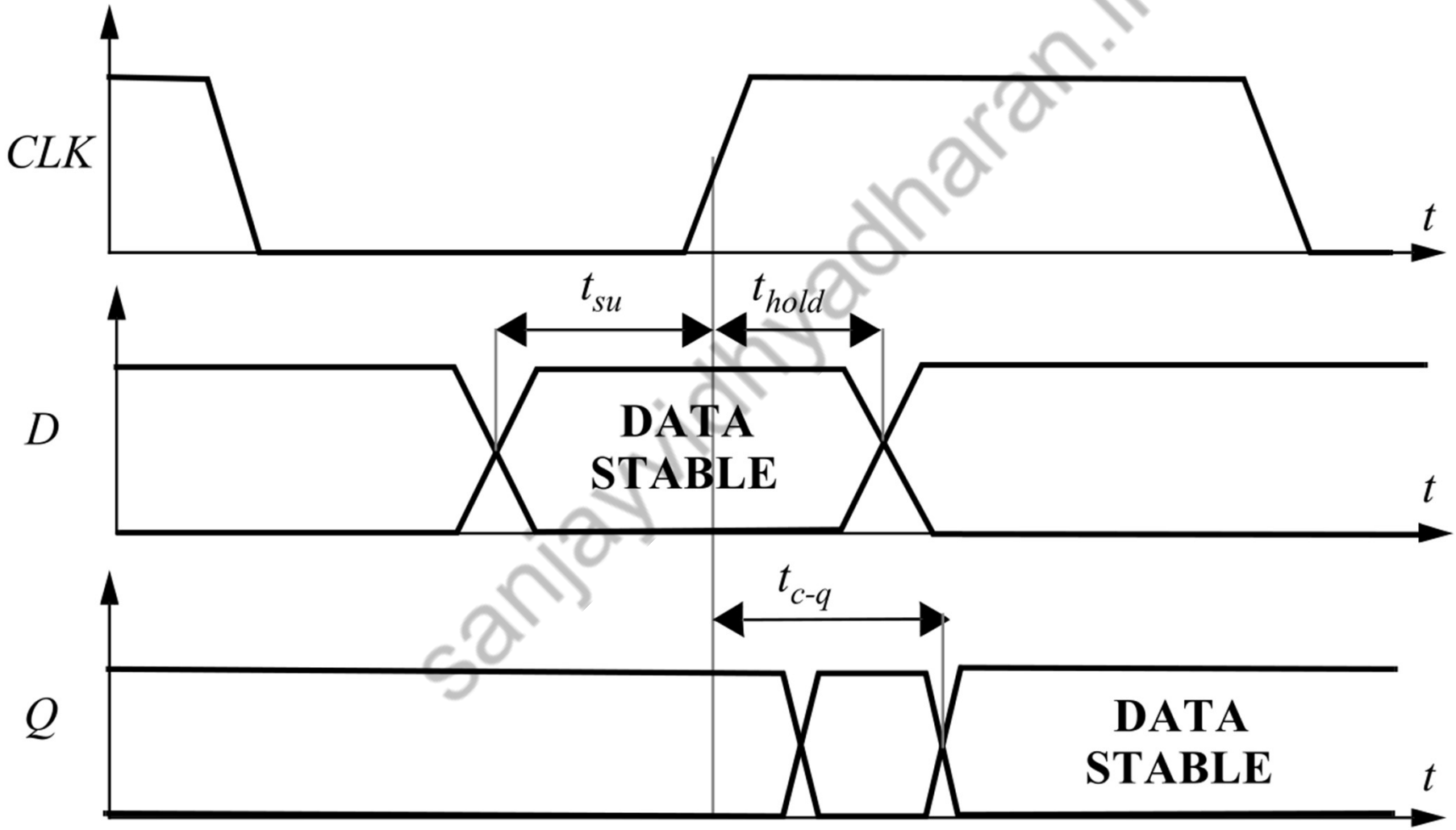
Timing Constraints of a Flip-flop

- Setup Time
- Hold Time



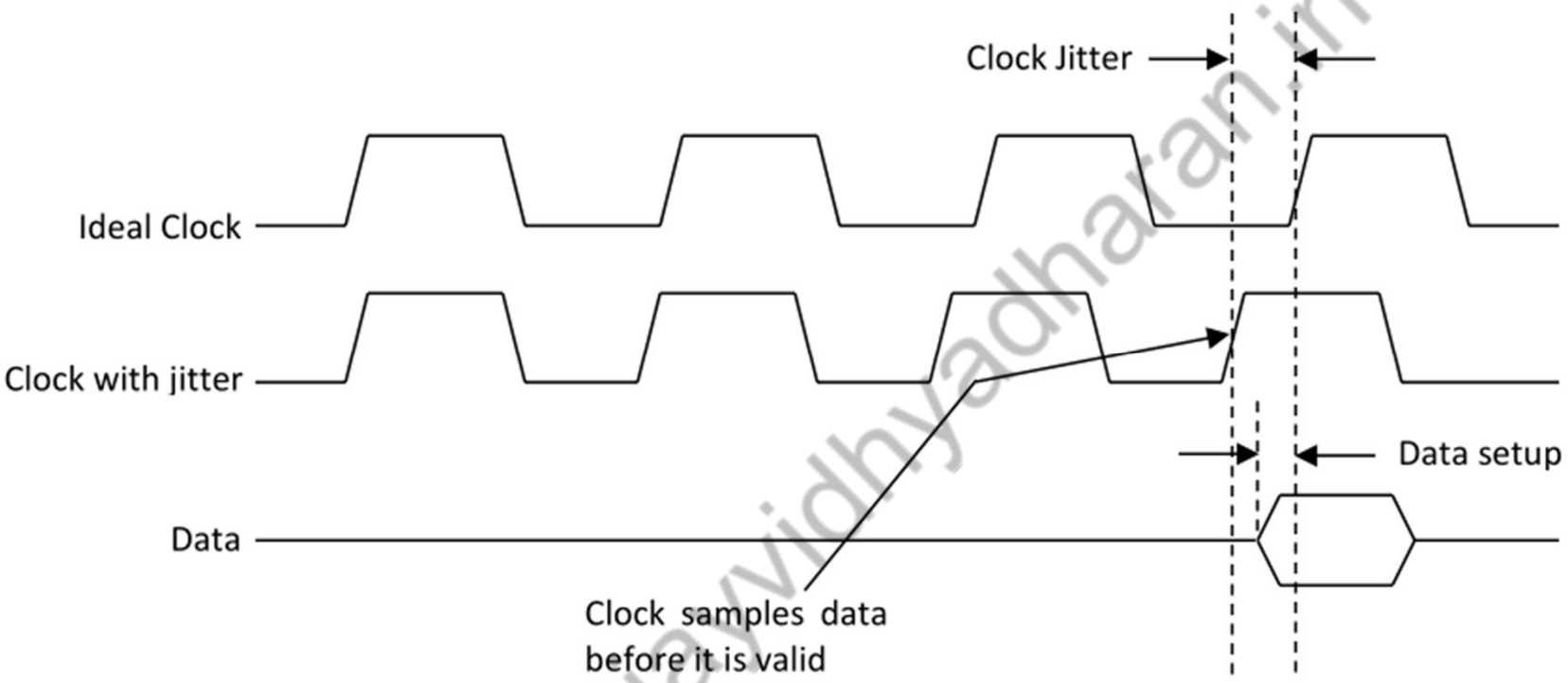
Clock Skew and Jitter

Clock skew (sometimes called timing **skew**) is a phenomenon in synchronous digital circuit systems (such as computer systems) in which the same sourced **clock** signal arrives at different components at different times.

Clock Jitter: Sometimes some external sources like noise, voltage variations may cause to disrupt the natural periodicity or frequency of the clock. This deviation from the natural location of the clock is termed to be clock jitter.

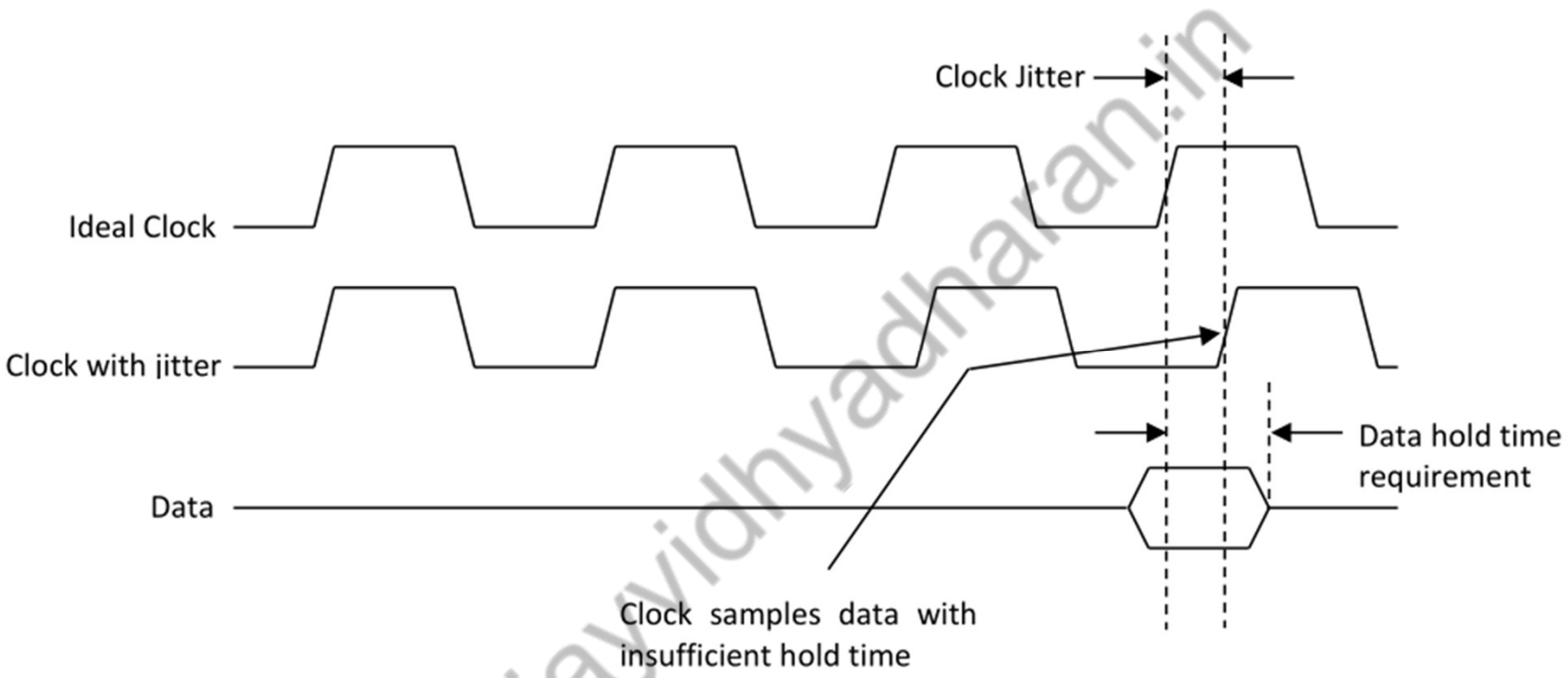
Clock Uncertainty = Clock Jitter + Clock Skew

Timing Constraints of a Flip-flop



Data setup violation caused by clock jitter

Timing Constraints of a Flip-flop



Data hold time violation caused by clock jitter

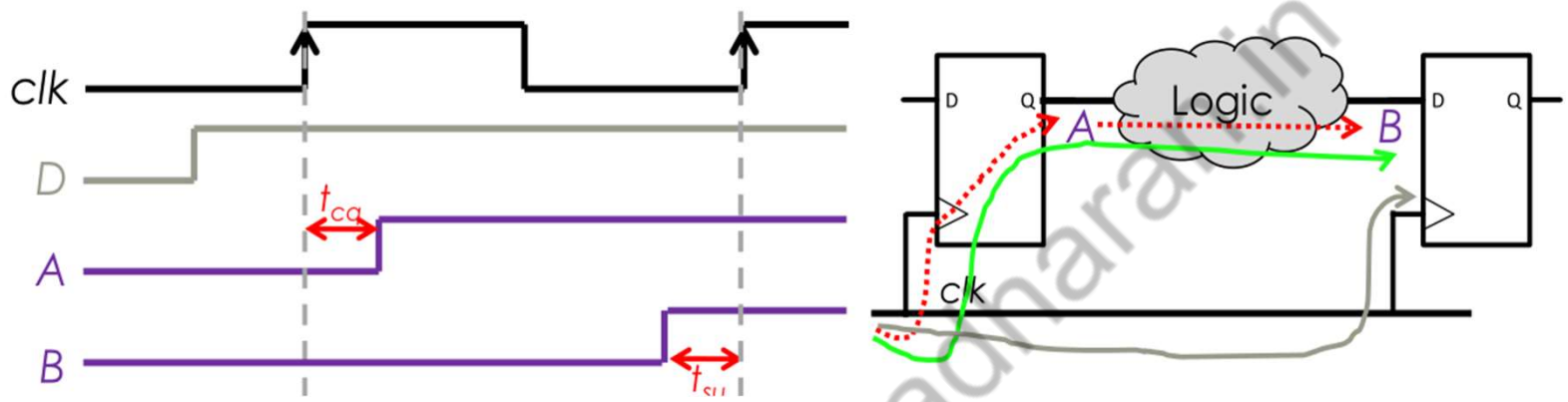
Static Time Analysis

There are two main problems that can arise in synchronous logic:

- Max Delay: The data doesn't have enough time to pass from one register to the next before the next clock edge.
- Min Delay: The data path is so short that it passes through several registers during the same clock cycle.
- Max delay violations are a result of a slow data path, including the registers, $\mathbf{t_{su}}$ therefore it is often called the "Setup" path.
- Min delay violations are a result of a short data path, causing the data to change before the $\mathbf{t_{hold}}$ has passed, therefore it is often called the "Hold" path.

Static Time Analysis

Setup (Max) Constraint



- After the clock rises, it takes t_{cq} for the data to propagate to point A.
- Then the data goes through the delay of the logic to get to point B.
- The data has to arrive at point B, t_{su} before the next clock.

$$T > t_{CQ} + t_{\text{logic}} + t_{SU}$$

$$T + \delta_{\text{skew}} > t_{CQ} + t_{\text{logic}} + t_{SU} + \delta_{\text{margin}}$$

Setup Slack = Data Required Time – Data Arrival Time

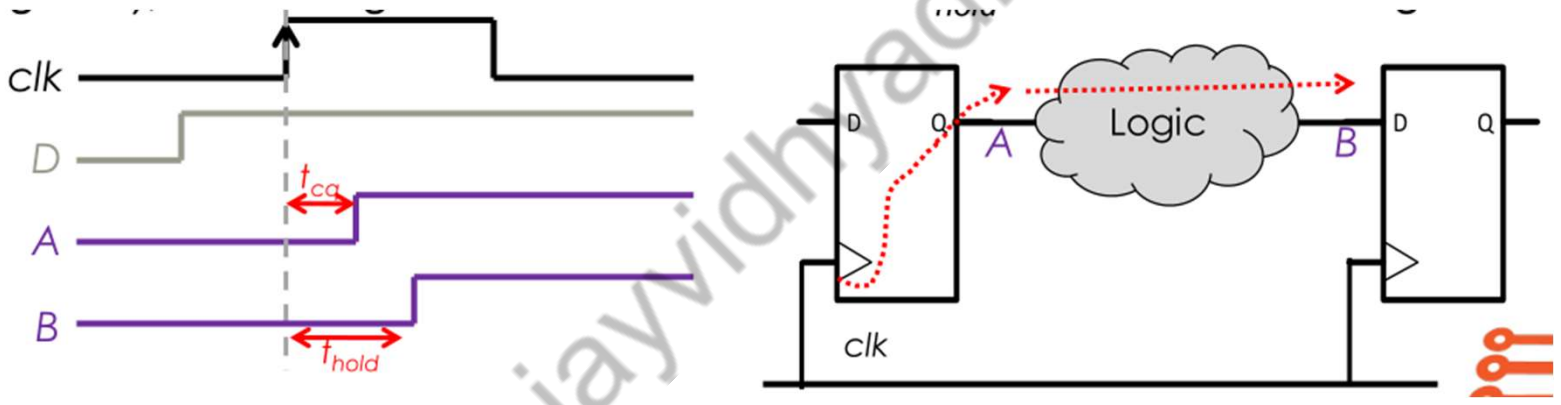
- Positive Slack : No Timing Violation
- Negative Slack : Timing Violation

Static Time Analysis

Hold (Min) Constraint

Hold problems occur due to the logic changing before t_{hold} has passed.
This is not a function of cycle time – it is relative to a single clock edge!

- The clock rises and the data at A changes after t_{cq} . The data at B changes t_{pd} (logic) later.
- Since the data at B had to stay stable for t_{hold} after the clock (for the second register), the change at B has to be at least t_{hold} after the clock edge.



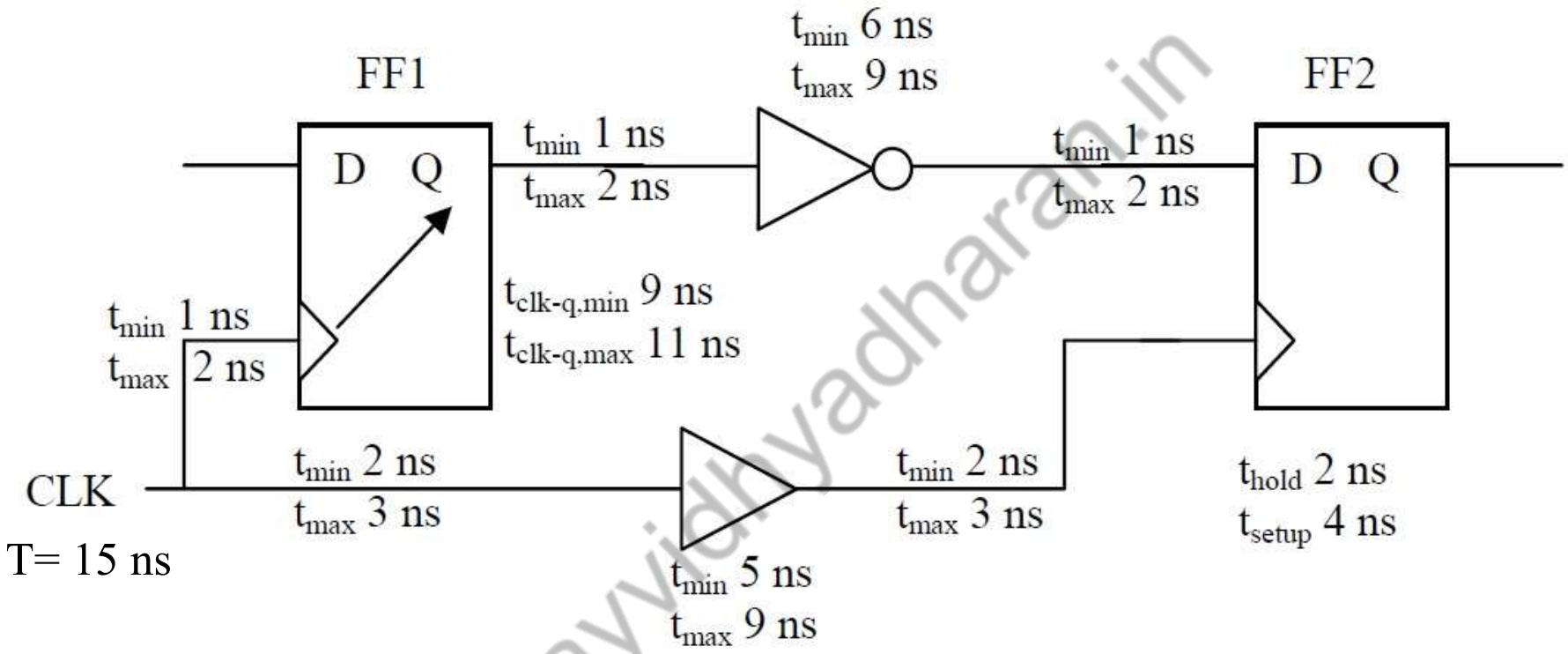
$$t_{CQ} + t_{\text{logic}} > t_{hold}$$

$$t_{CQ} + t_{\text{logic}} - \delta_{\text{margin}} > t_{hold} + \delta_{\text{skew}}$$

Hold Slack = Data Arrival Time– Data Required Time

- Positive Slack : No Timing Violation
- Negative Slack : Timing Violation

Static Time Analysis



Setup slack = Min. Clock Path Delay - Max. Data Arrival Time

= (15 ns + 2ns + 5 ns + 2 ns - 4 ns) - (2 ns + 11 ns +2 ns + 9 ns + 2 ns)

= 20 ns – 26 ns = -6 ns : Setup Time Violation.

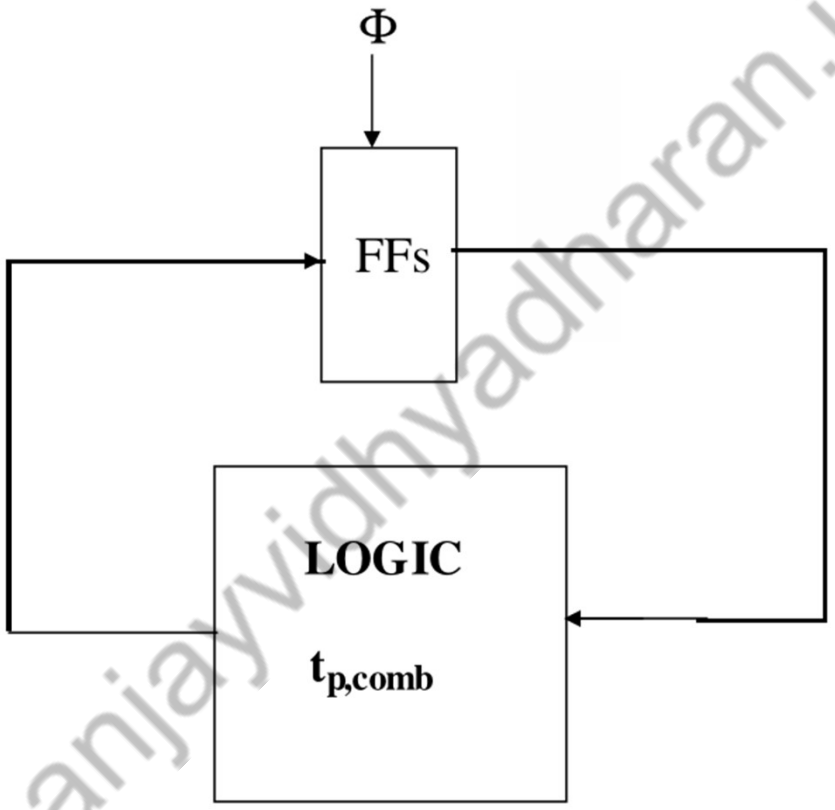
Hold time slack = Min. Data Arrival Time - Max. Clock Path Delay

= (1 ns + 9 ns + 1 ns + 6 ns + 1 ns) - (3 ns + 9ns + 3 ns + 2 ns) -

= 18 ns – 17 ns = + 1ns : No Hold Time Violation.

Timing Constraints of a Sequential Circuit

Maximum Clock Frequency



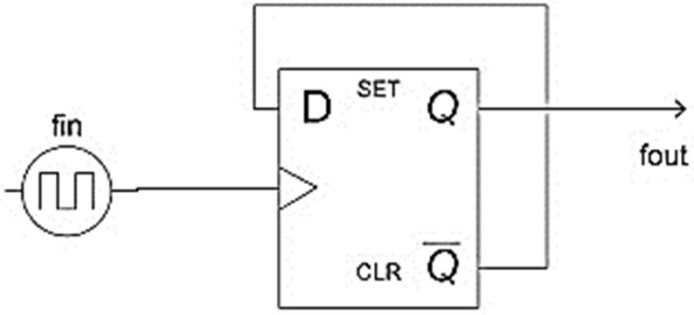
$$t_{pFF} + t_{pComb} + t_{setup} < T$$

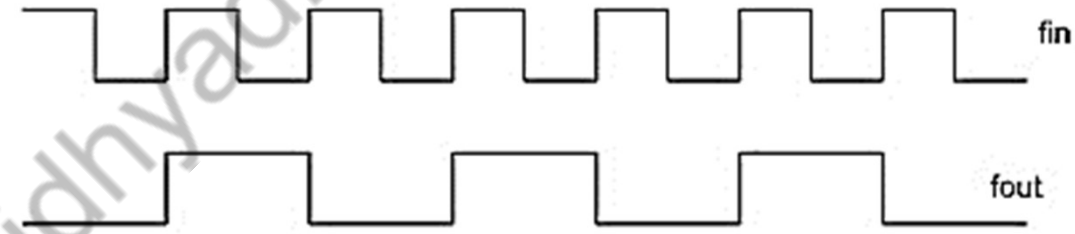
Static Time Analysis

Given the data setup time of the flop is 6ns, the hold time of the flop is 2ns, and the clock to Q delay is given as 10ns.

a. Calculate the minimum clock period required to handle the circuit by drawing a digital logic circuit for function clock frequency divided by 2.

b. Also determine the status of hold time violation and give a proper reason.





$T_{minimum} >= T_{setup\_time} + T_{clock\_Q} + dly$

$T_{minimum} >= 6ns + 10ns + 0$

$T_{minimum} >= 16ns$

$f_{maximum} = 1/16ns = 62.5MHz$ is the maximum possible frequency of operation

$T_{hold\_time} <= T_{clock\_Q} + delay$

$2ns <= 10ns + 0$

$2ns <= 10ns$ No Hold Time Violation

Thank you