Advanced VLSI Design: 2021-22
Lecture 4 : Part-1
Pipelined Registers and Static Timing Analysis

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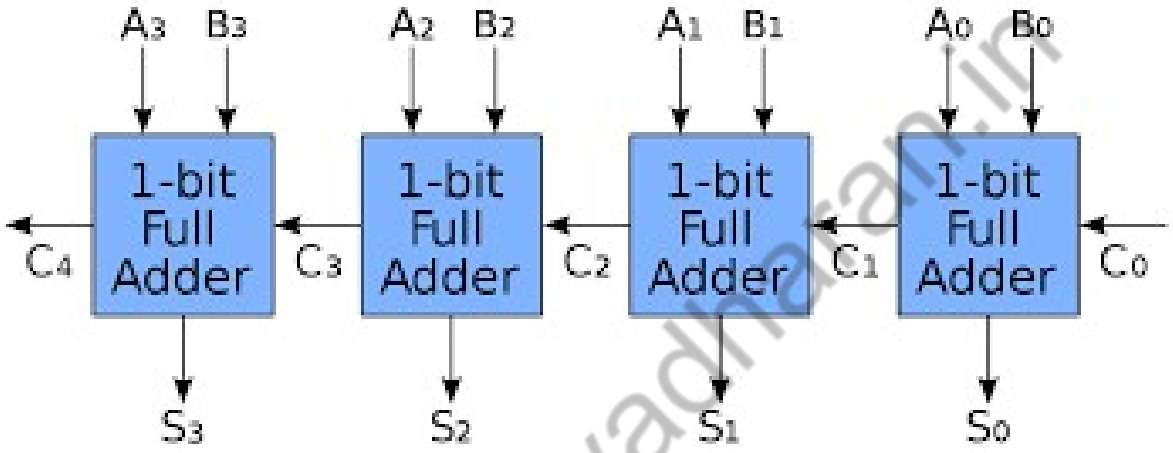
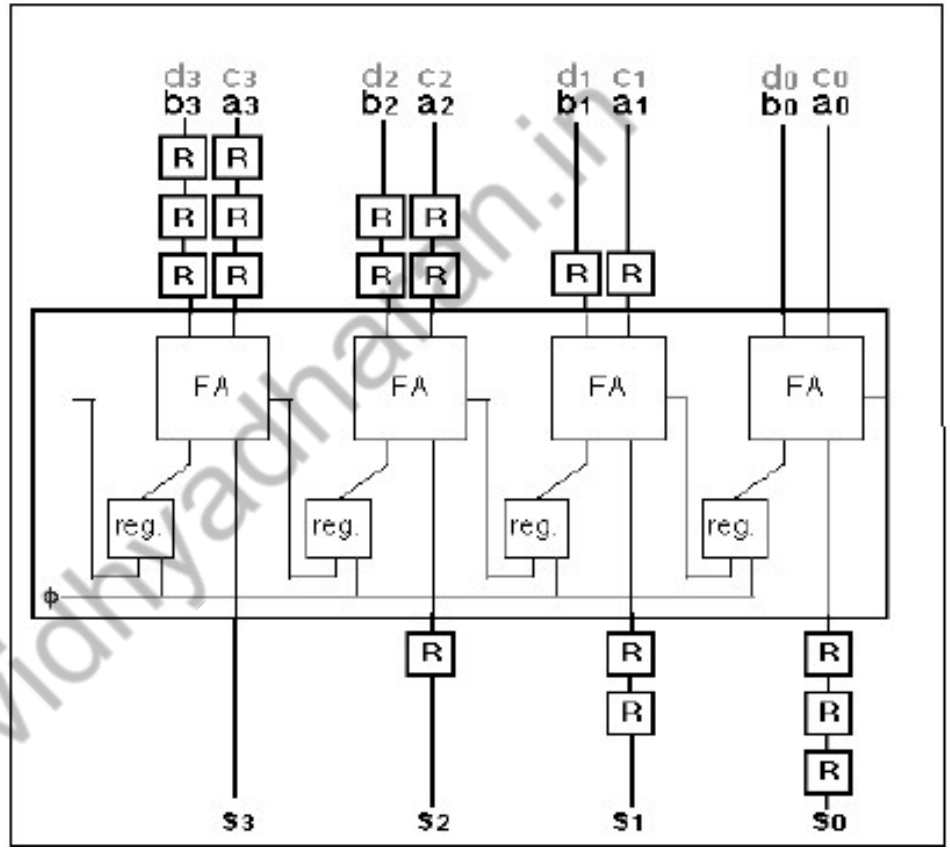
4-Bit Adder



Performance Figure	Value
Function Delay	$3 * \tau_{pd\_adder(Carry)} + \tau_{pd\_adder(Sum)}$
Power	$4 * P_{adder}$
Throughput	$@ (3 * \tau_{pd\_adder(Carry)} + \tau_{pd\_adder(Sum)})$
Gate complexity	$4 * G_{adder}$

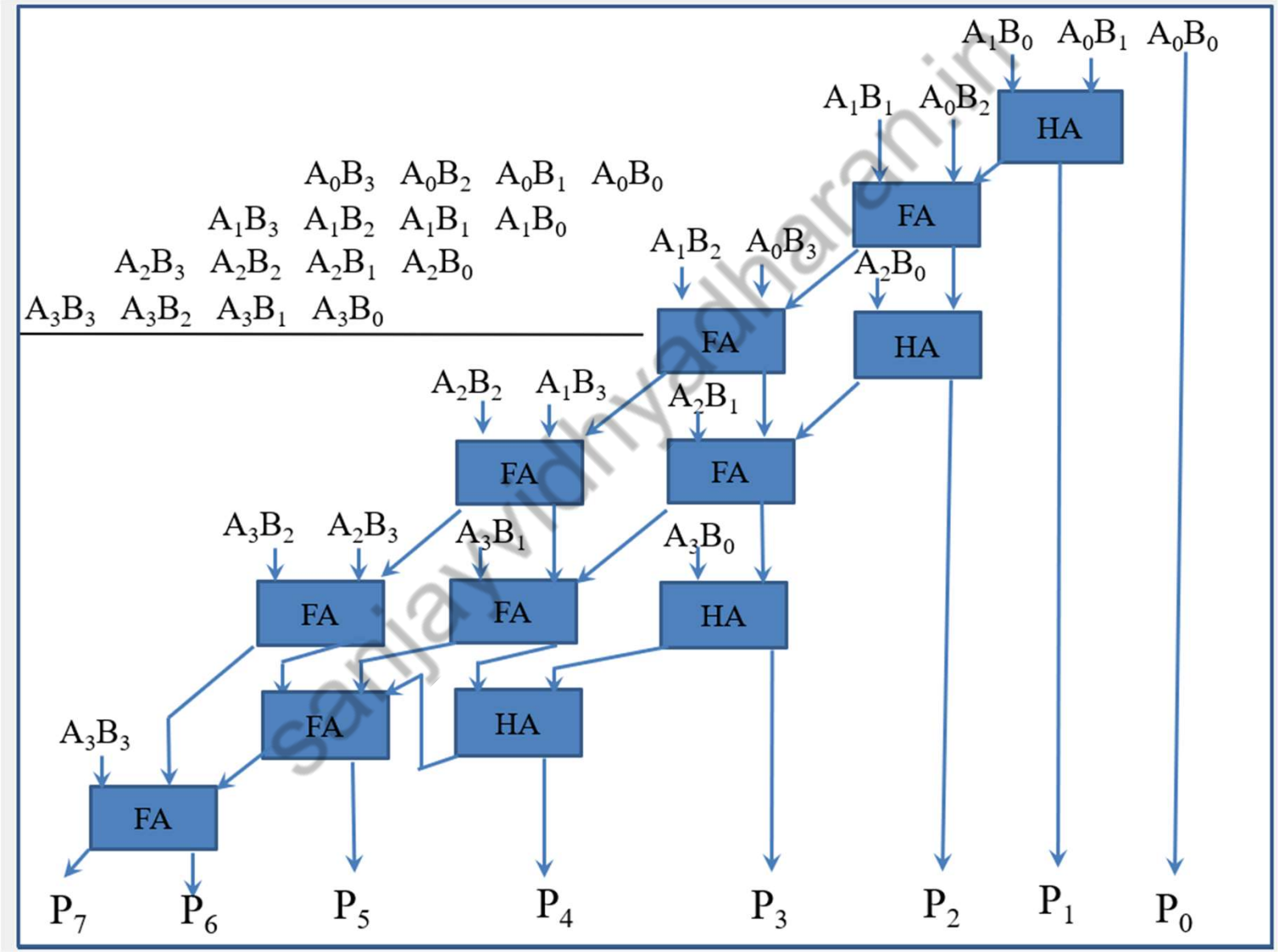
Pipelined 4-Bit Adder

Principle of Operation:

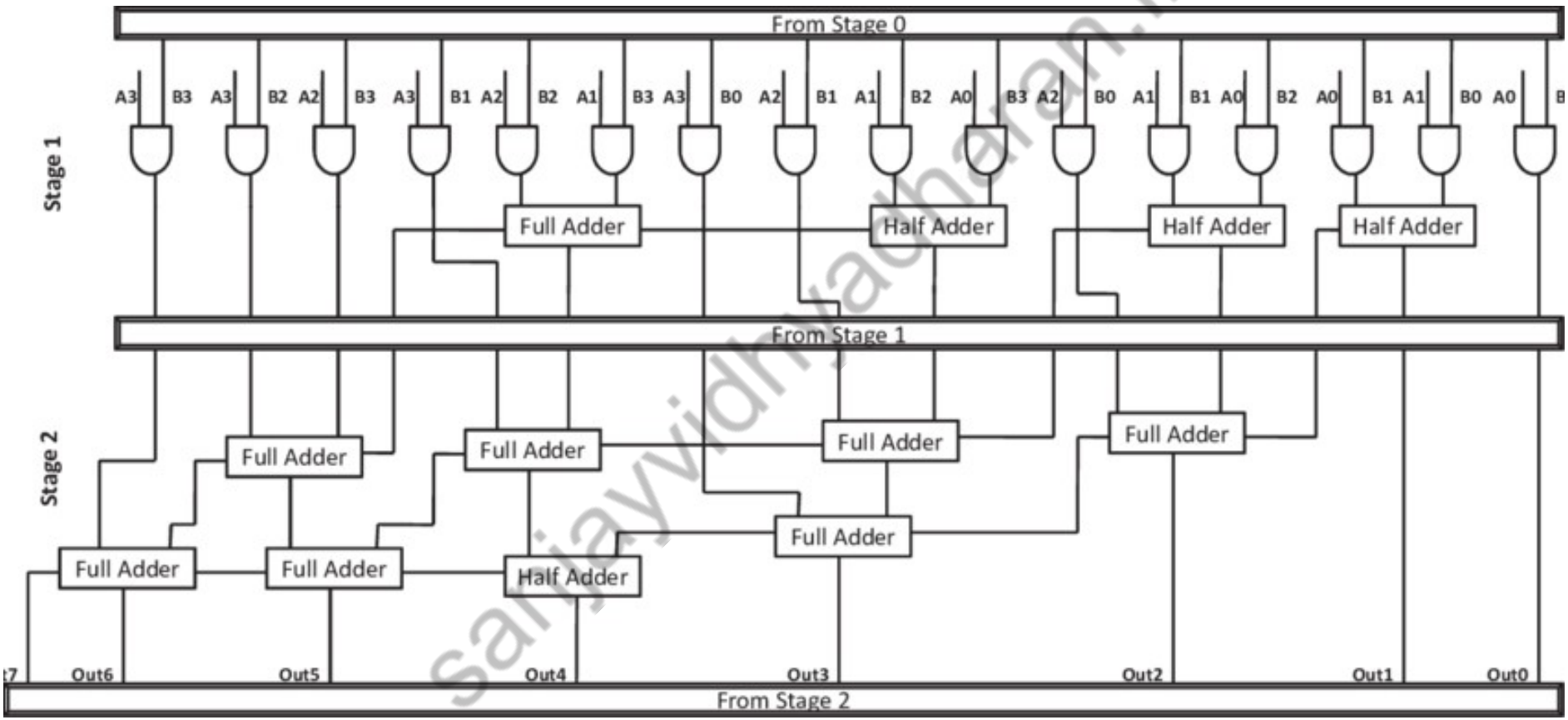


Performance Figure	Value
Function Delay	$4*T_{clock}$ ($T_{clock} > T_{pd\_adder} + T_{setup} + T_{clk-Q}$)
Power	$4 * P_{adder} + 22 * P_{Regsiter}$
Throughput	@ T_{Clock}
Gate complexity	$4 * G_{adder} + 22 * G_{Register}$

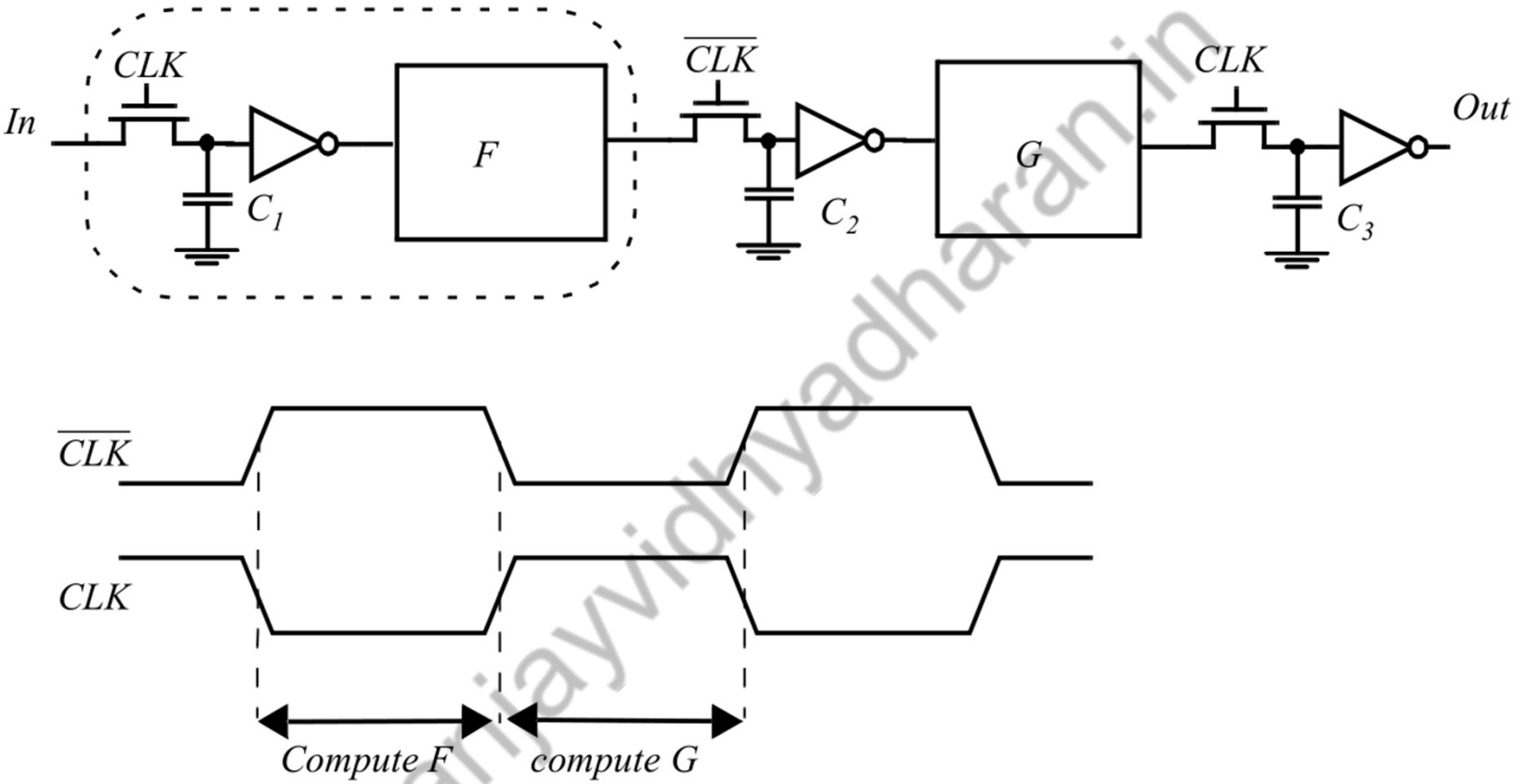
4-Bit Multiplier



4-Bit Pipelined Multiplier

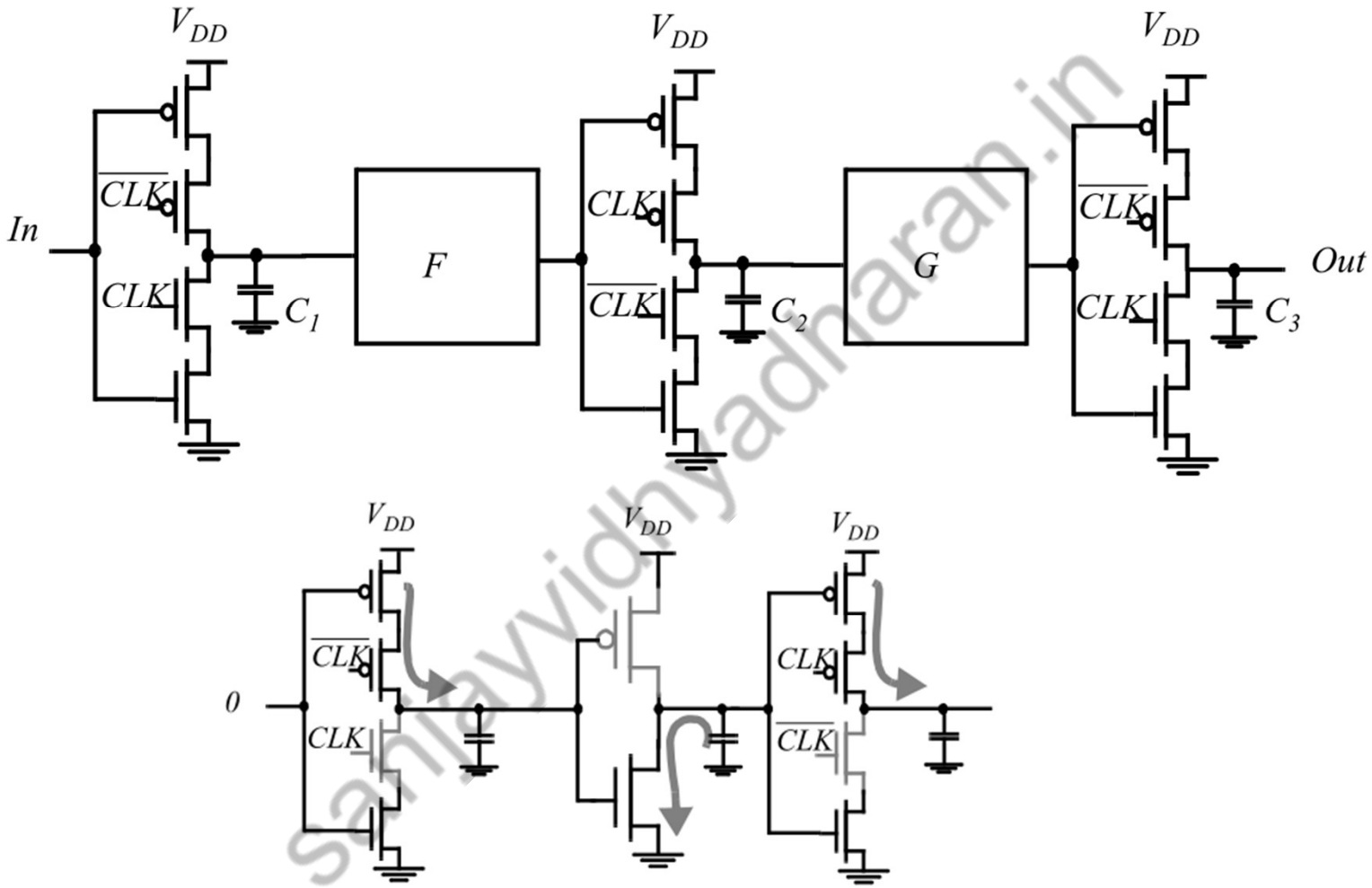


Pipelining with Latches



A non-overlapping clock essential for correct operation. Else there will be race around

Pipelined Logic using C²MOS

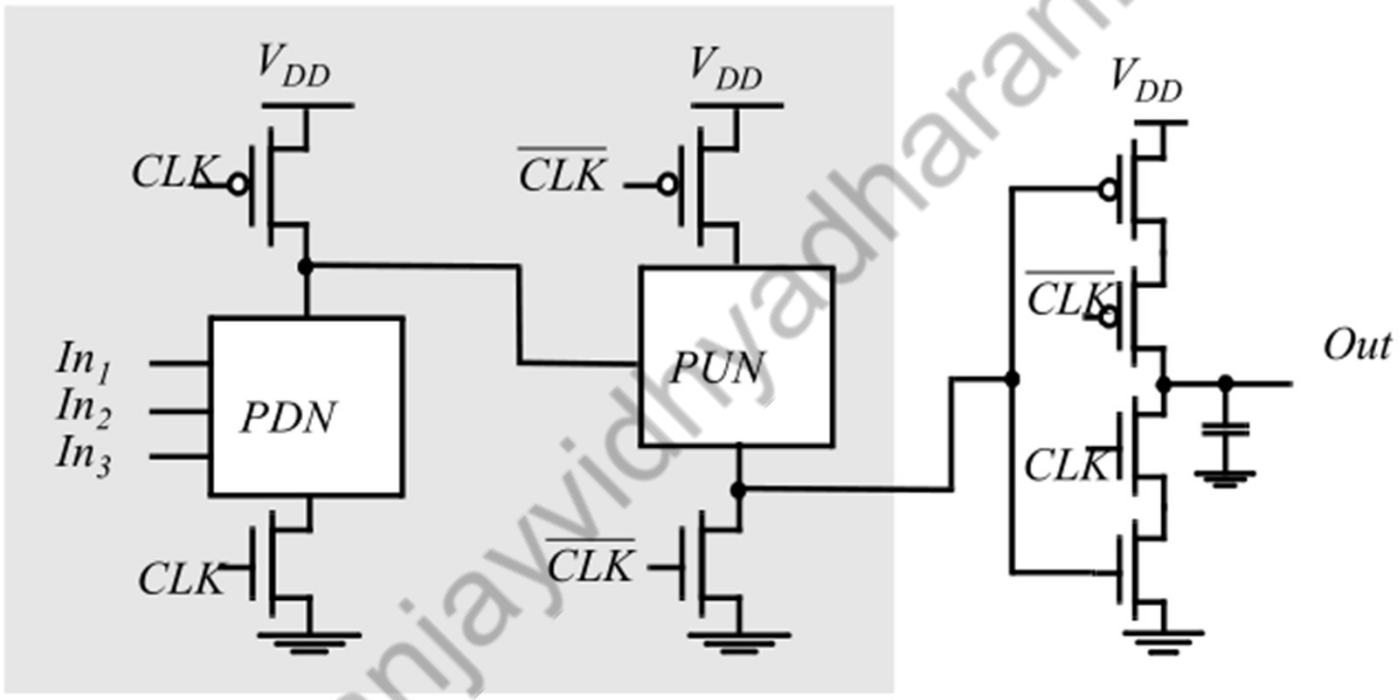


Potential race condition during (0-0) overlap in C²MOS-based design

Similar considerations are valid for the (1-1) overlap.

NORA CMOS

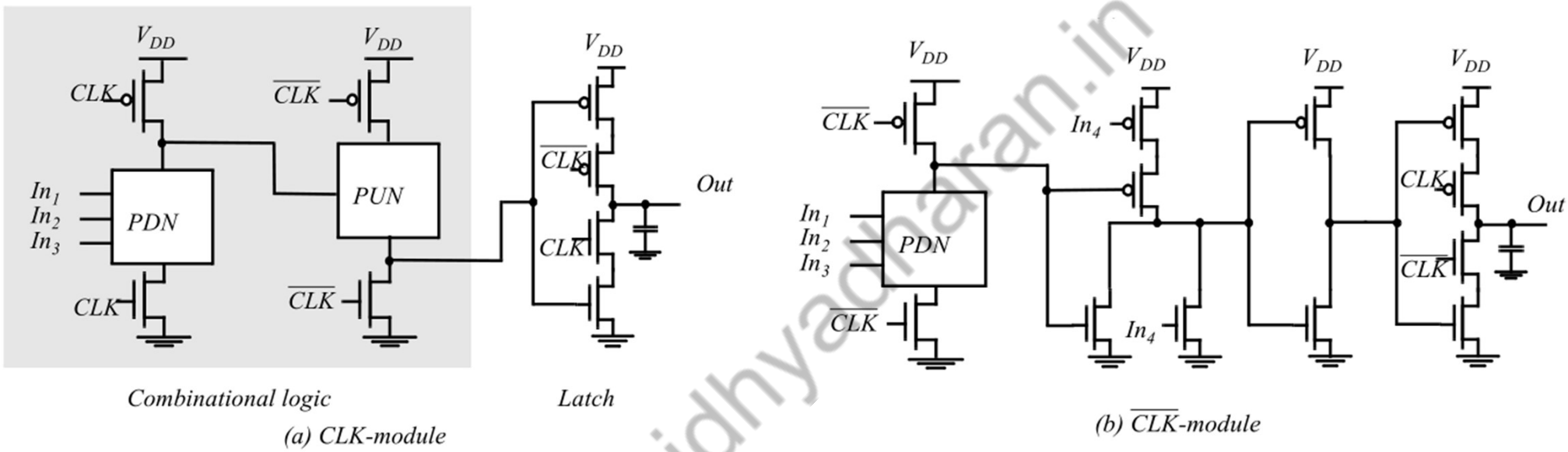
It combines C^2MOS pipeline registers and NORA dynamic logic functional blocks.



(a) CLK-module

NORA CMOS

It combines C^2MOS pipeline registers and NORA dynamic logic functional blocks.



	Φ-block		$\overline{\Phi}$-block	
	Logic	Latch	Logic	Latch
Φ = 0	Precharge	Hold	Evaluate	Evaluate
Φ = 1	Evaluate	Evaluate	Precharge	Hold

NORA offers designers a wide range of design choices. Dynamic and static logic can be mixed freely. A NORA datapath consists of a chain of alternating CLK and CLK modules. While one class of modules is precharging with its output latch in hold mode, preserving the pre-vious output value, the other class is evaluating. Data is passed in a pipelined fashion from module to module.