VLSI SYSTEMS AND ARCHITECTURE

2021-22

Lecture 1

Introduction to VLSI Architecture

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VLSI System Design

VLSI Design Starts with System Specifications

The System specifications include

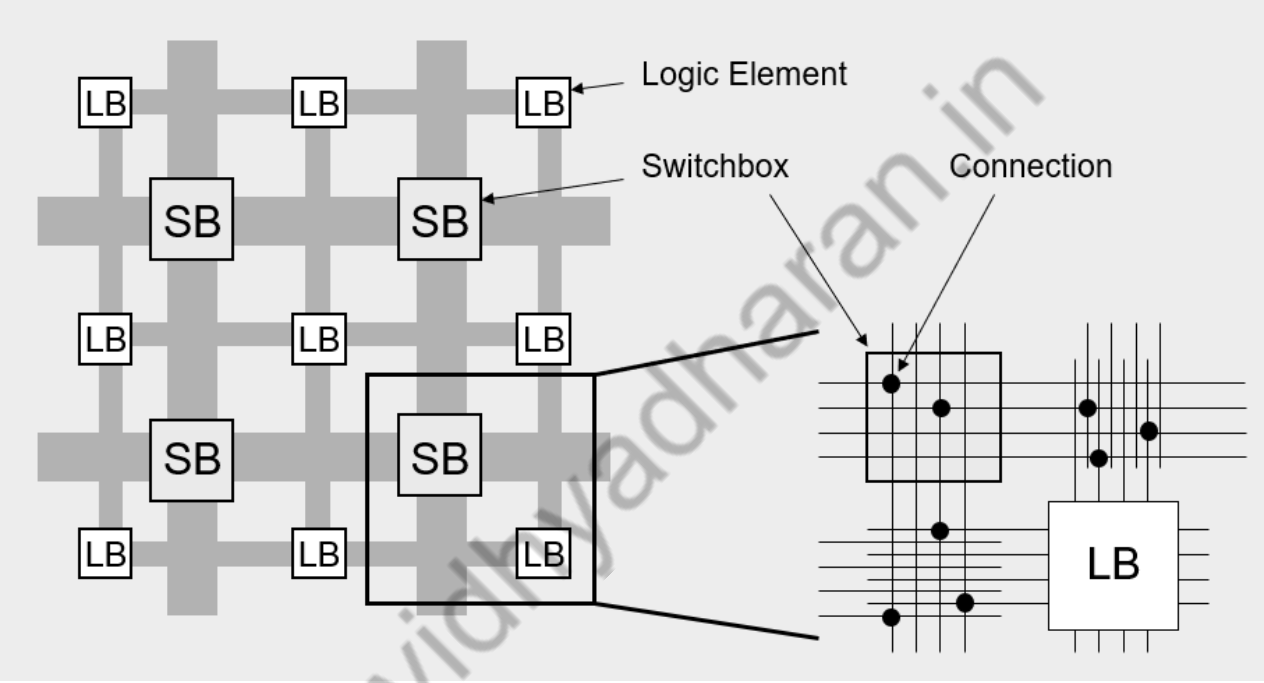
- Technical Requirements,
- Market requirements and
- Economic Considerations

Technical Requirements include

- Size of the IC,
- The maximum amount of power that can be consumed and
- The performance and the functionality

VLSI Design Styles

1. FPGA

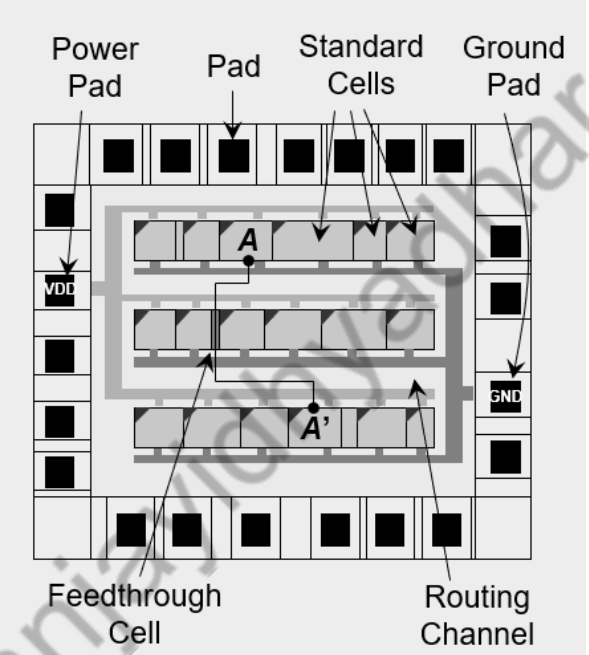


- CLBs have also been introduced to map complex functions
- Behavioral description of functionality, using a hardware description language (e.g. VHDL)
- FPGA-based design is the very short turn-around time, Fast Prototyping
- No physical manufacturing step is necessary
- Cost effective for small-volume production
- Slower, Bulkier, Complex, Higher Power Requirements, Expensive for Large-volume

VLSI Design Styles

2. Standard Cell or Semi-Custom Design

It uses pre-designed logic cell(and gates, OR gate, multiplexers) known as standard cells.

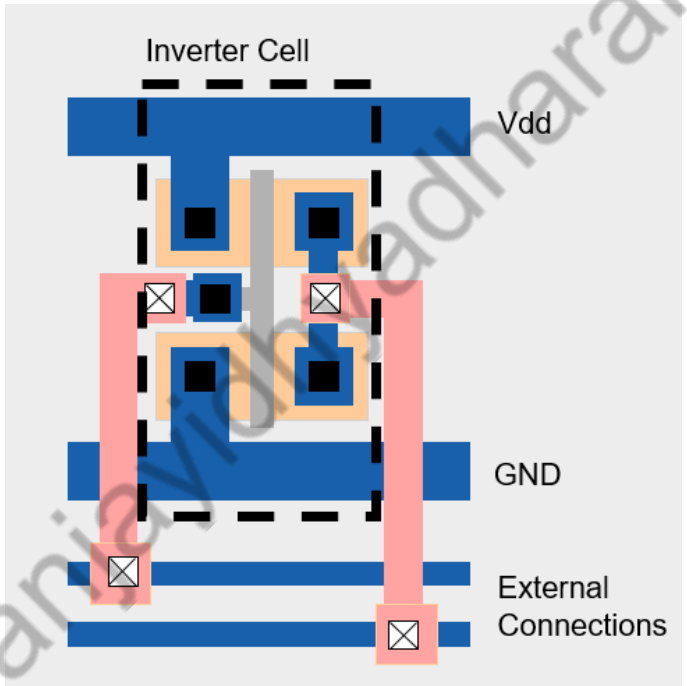


- Technical Specifications are Optimised using EDA tools before fabrication
- Medium Prototyping time.
- Expensive for Small-volume Production

VLSI Design Styles

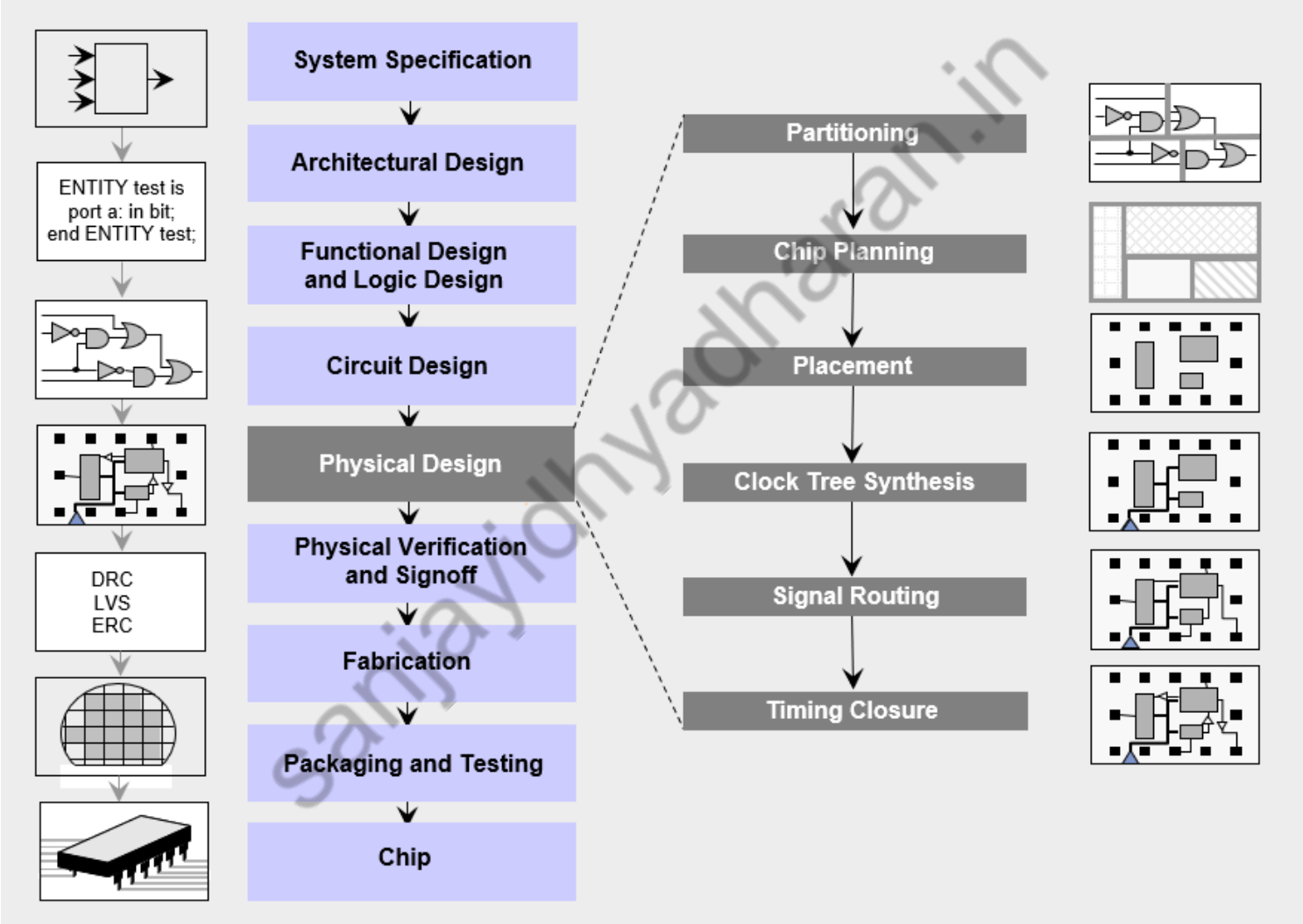
3. Full-Custom Design

Full custom design requires all the components to be designed and verified right from the transistor level. This methodology is used for mass production

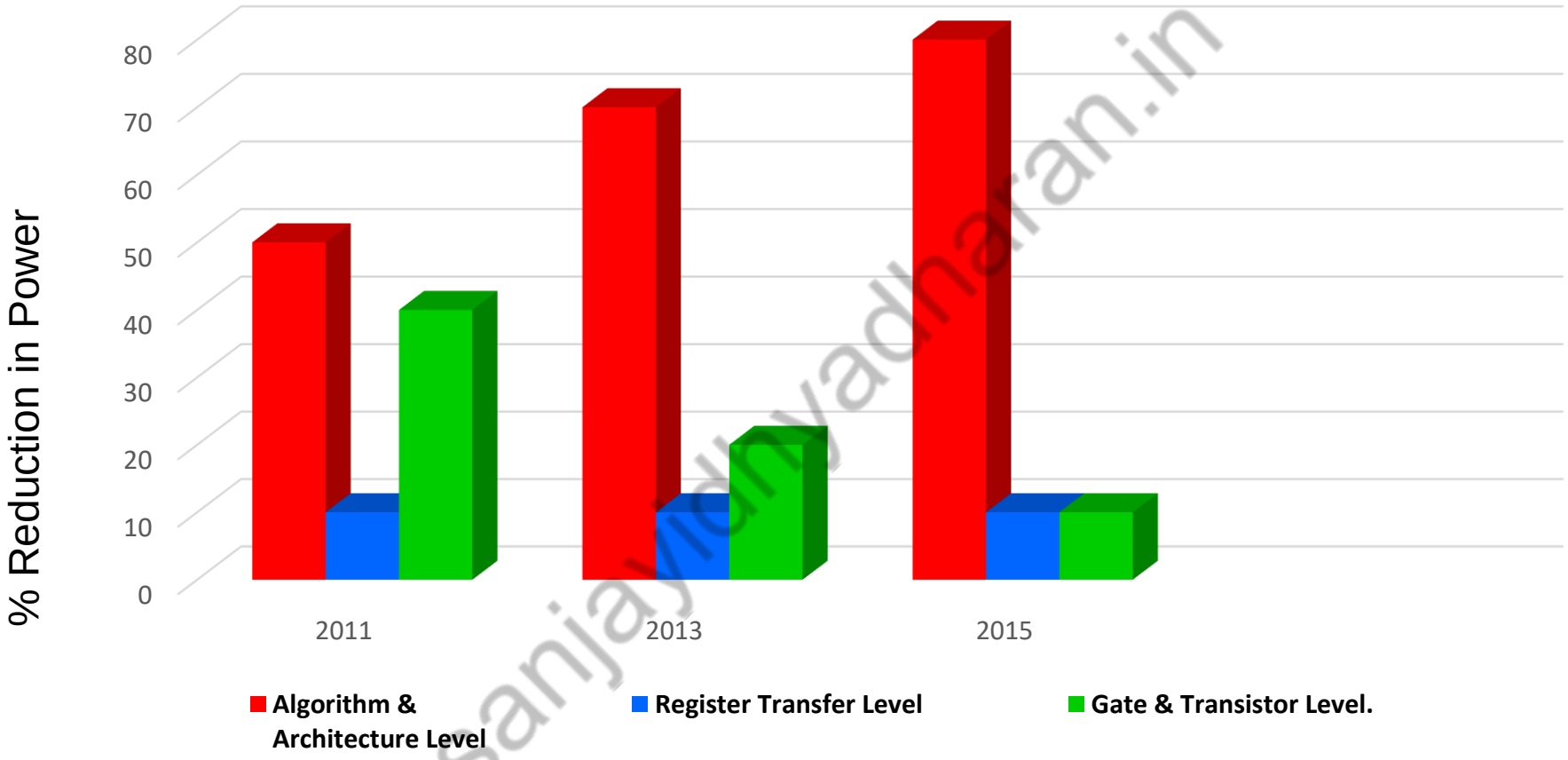


- Technical Specifications are Best Optimised the most using EDA tools before fabrication
- High Prototyping time.
- Expensive for Small-volume Production

VLSI Design Flow



VLSI Architecture



[4] V. Natarajan, A. Nagarajan, N. Pandian, and V. Savithri, "Low Power Design Methodology," 02 2018.
isbn = 978-953-51-3863-1, doi = 10.5772/intechopen.73729
[Online]. Available: https://www.intechopen.com/books/very-large-scale-integration/low-power-design-methodology

VLSI Architecture Example 1

Ex: Behavioral Model of an Adder

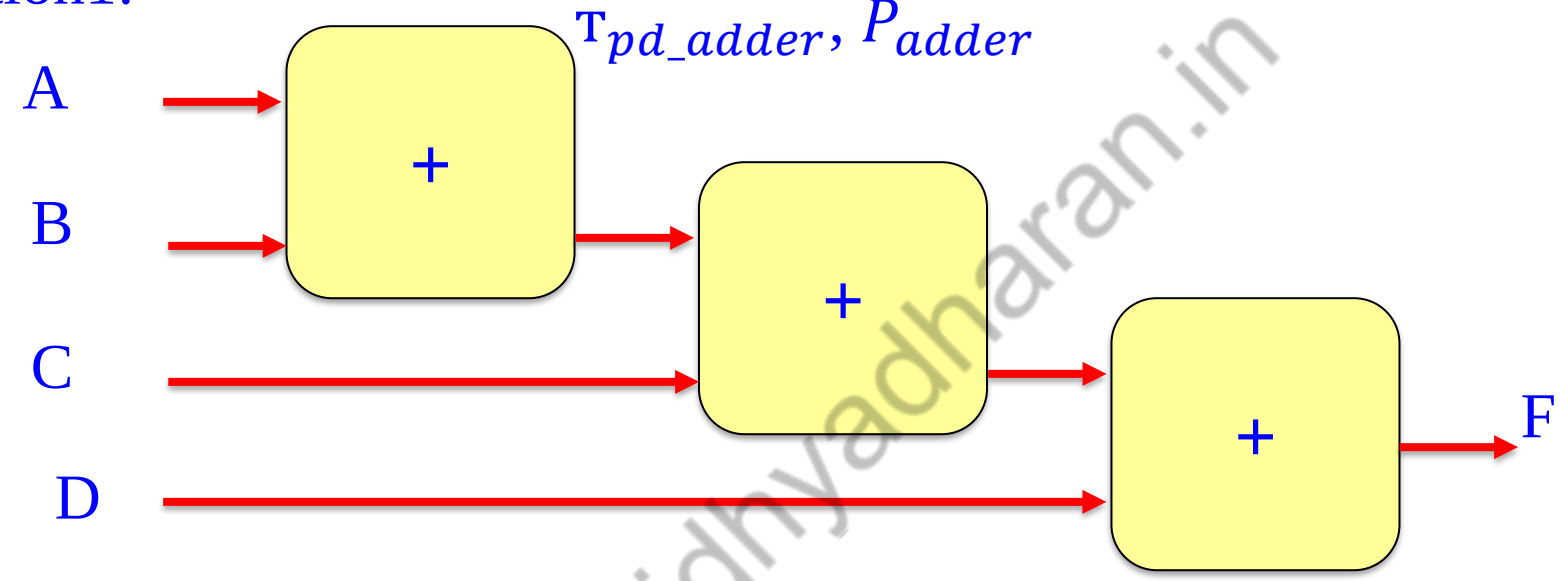
$$Z = A + B + C + D$$

Architectural choices

to realize digital hardware solution for a given behavioral description - creation of suitable architectural plan

VLSI Architecture Example 1

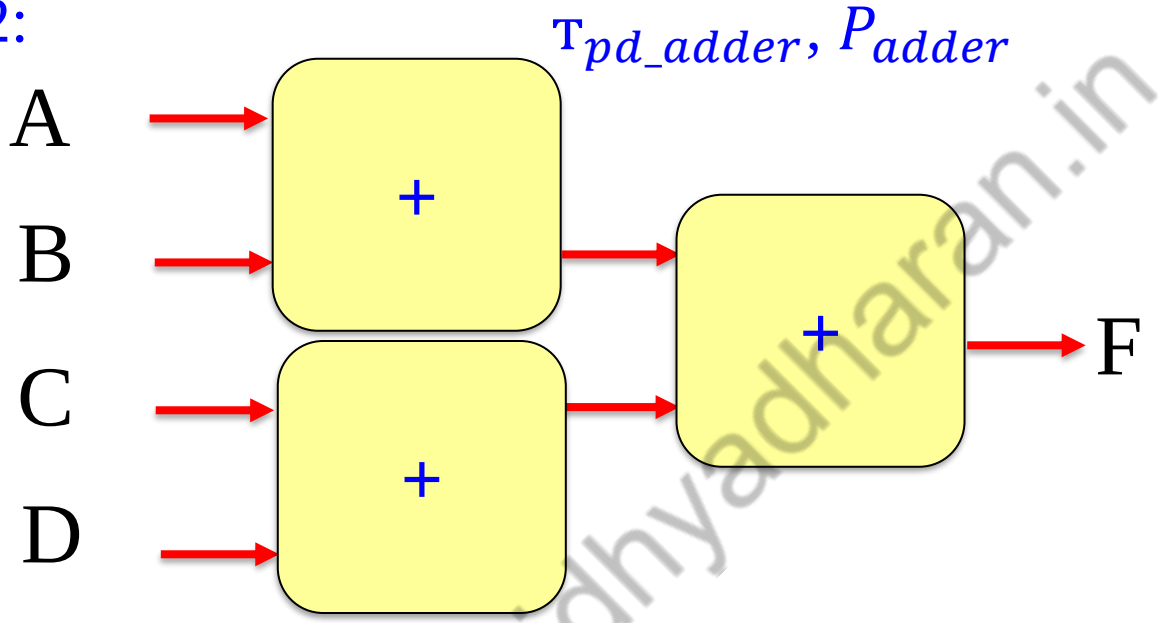
Option1:



Performance Figure	Value
Function Delay	3 * τ_{pd_adder}
Power	3 * P_{adder}
Throughput	@ 3 *τ_{pd_adder}
Gate complexity	3 * G_{adder}
Functional Flexibility	Nil
Function Expandability	Nil

VLSI Architecture Example 1

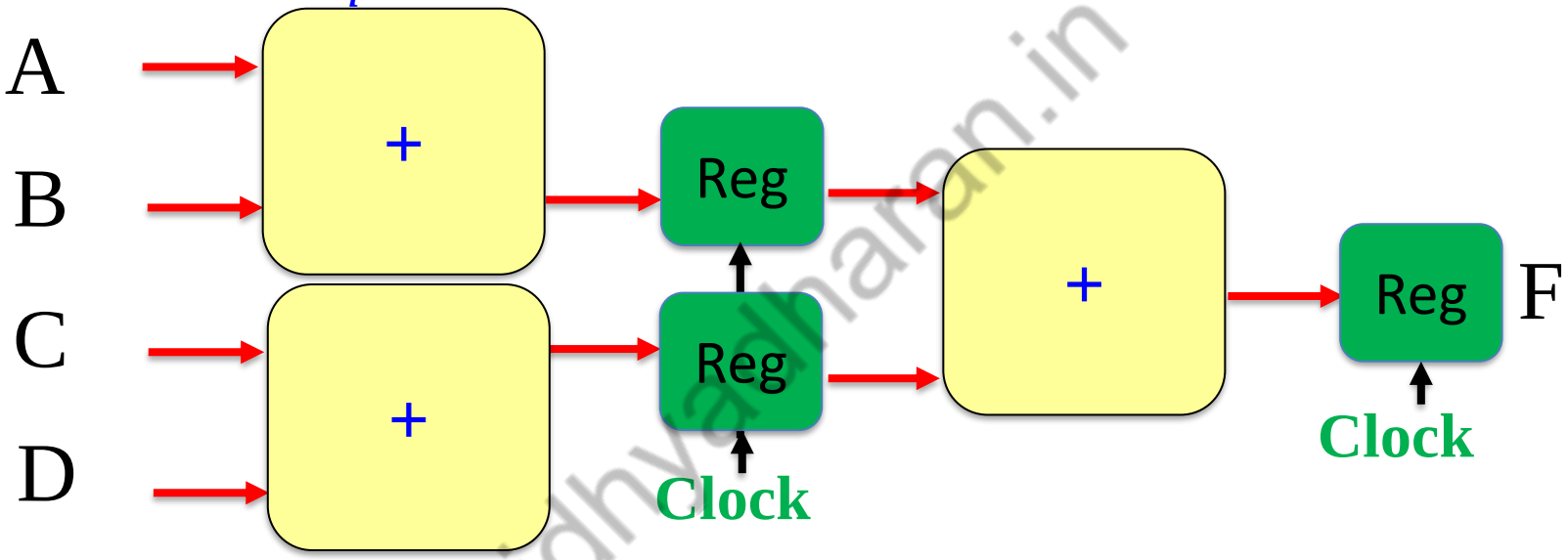
Option 2:



Performance Figure	Value
Function Delay	2 *τ_{pd_adder}
Power	3 * P_{adder}
Throughput	@ 2 *τ_{pd_adder}
Gate complexity	3 * G_{adder}
Functional Flexibility	Nil
Function Expandability	Nil

VLSI Architecture Example 1

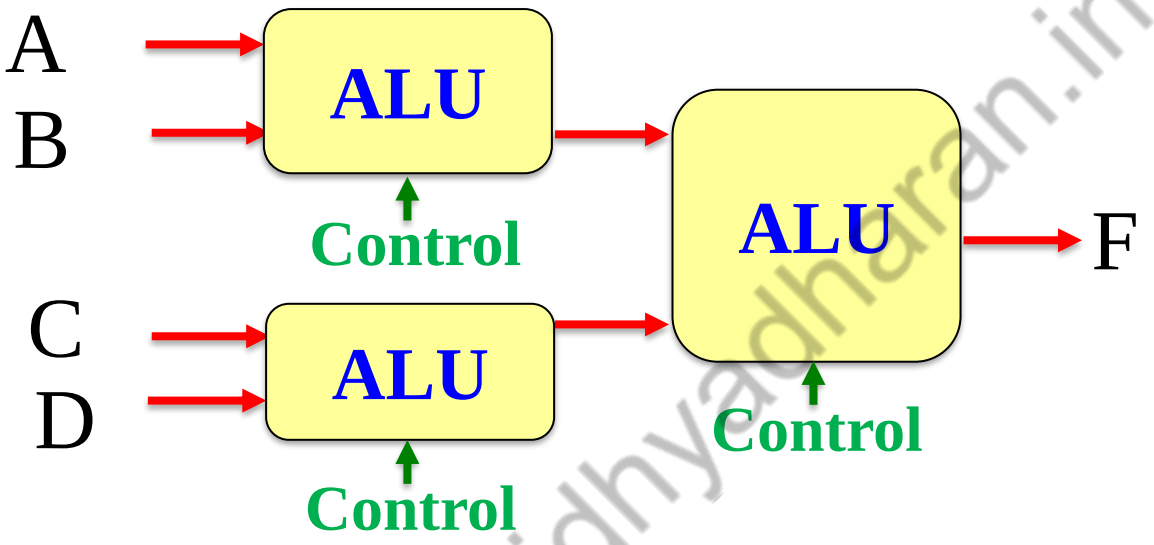
Option 3: τ_{pd}, P_{adder}



Performance Figure	Value
Function Delay	$2*T_{Clock}$
Power	$3 * P_{adder} + 3 * P_{Regsiter}$
Throughput	@ T_{Clock} ($\tau_{clk-Q} + \tau_{pd\_adder} + \tau_{setup}$)
Gate complexity	$3 * G_{adder} + 2 * G_{Register}$
Functional Flexibility	Nil
Function Expandability	Nil

VLSI Architecture Example 1

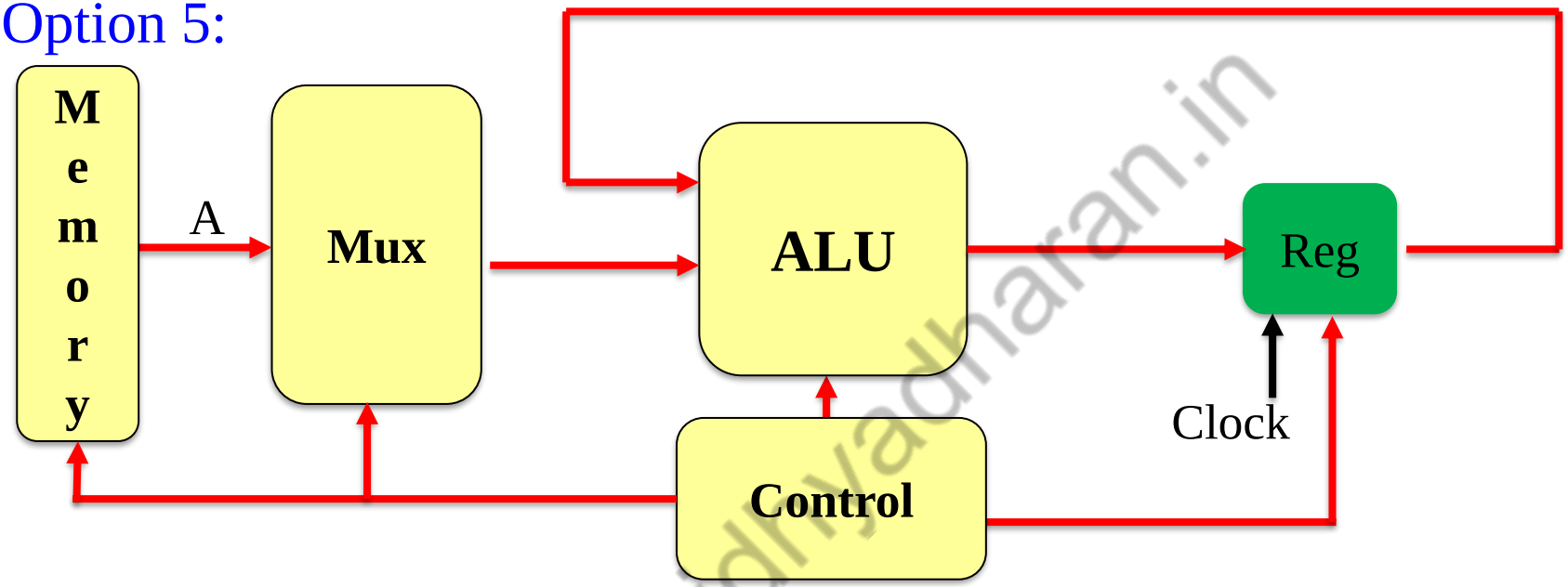
Option 4: τ_{pd}, P_{adder}



Performance Figure	Value
Function Delay	$2 * \tau_{ALU}$
Power	$3 * P_{ALU}$
Throughput	@ $2*T_{ALU}$
Gate complexity	$3 * G_{ALU}$
Functional Flexibility	Yes
Function Expandability	Nil

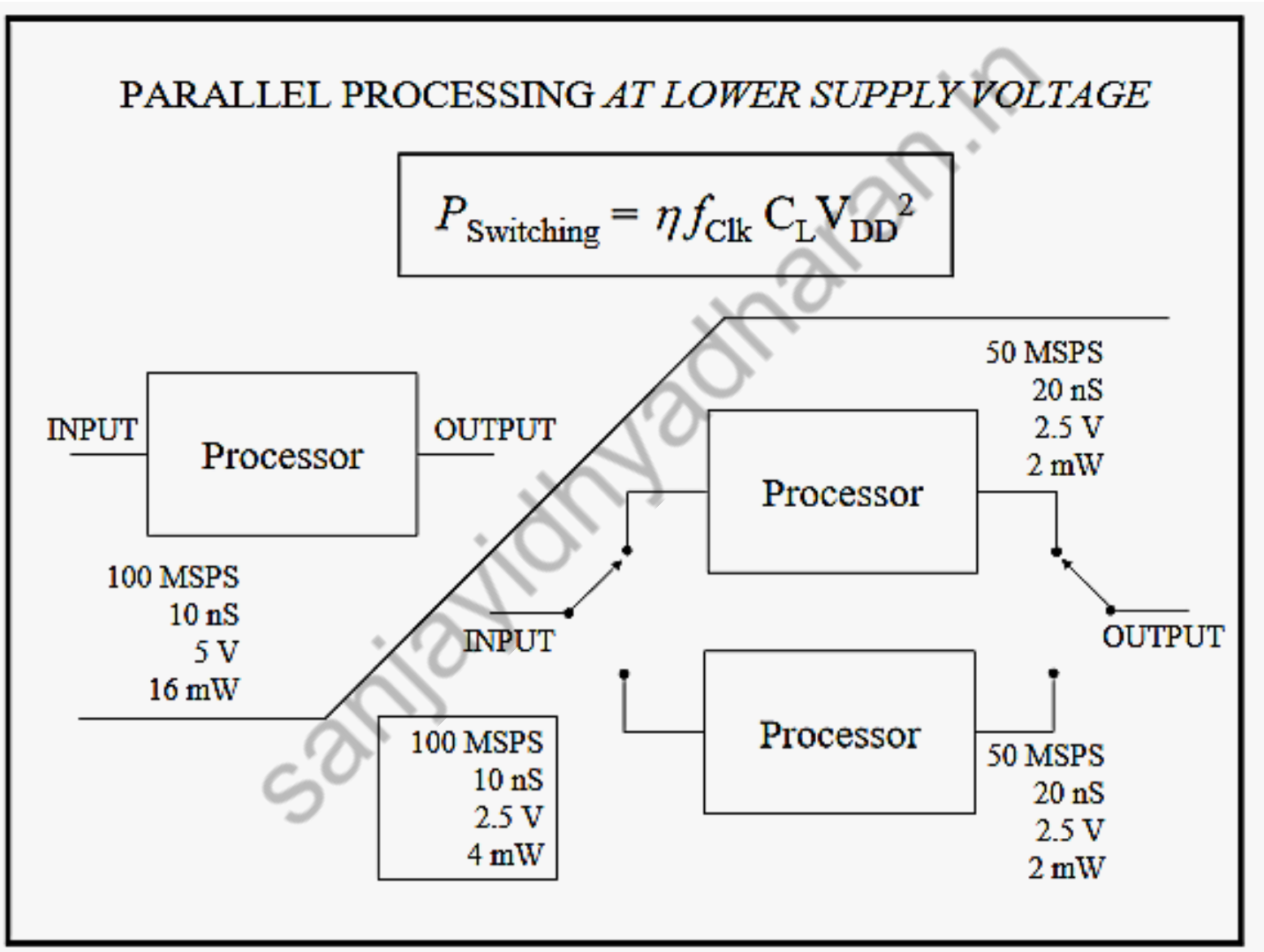
VLSI Architecture Example 1

Option 5:

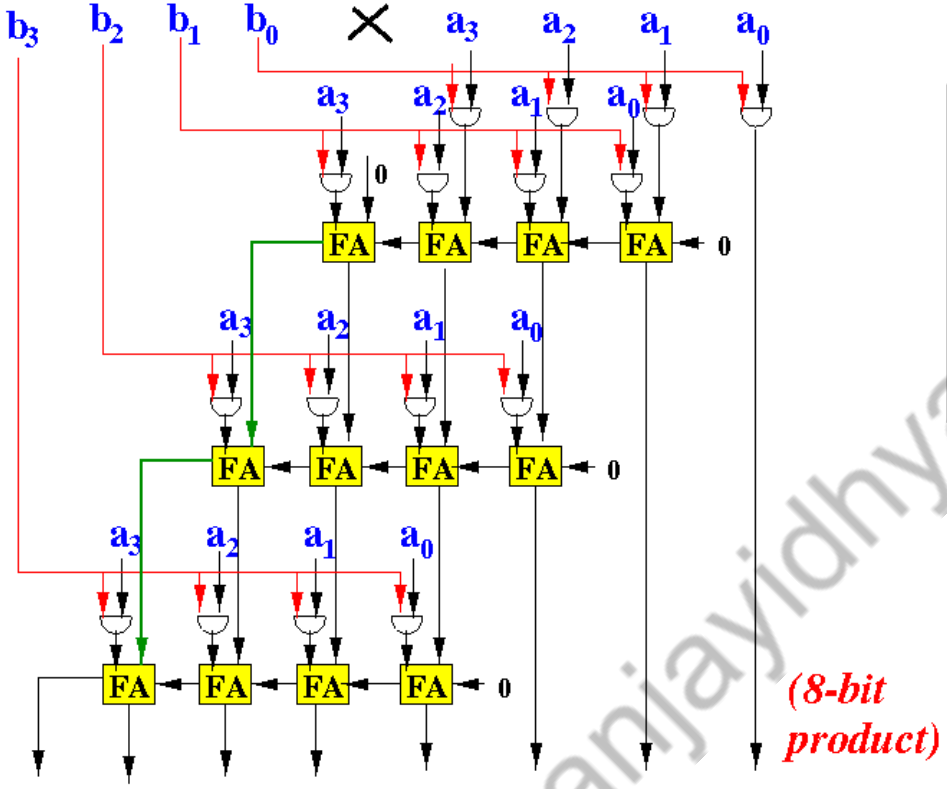


Performance Figure	Value
Function Delay	$\tau_{MUX} + T_{ALU} + \tau_{clk-Q}$
Power	$P_{MUX} + P_{ALU} + P_{Regsiter}$
Throughput	@ 4 * T_{CLK}
Gate complexity	$G_{MUX} + G_{ALU} + G_{Regsiter}$
Functional Flexibility	Yes
Function Expandability	Yes

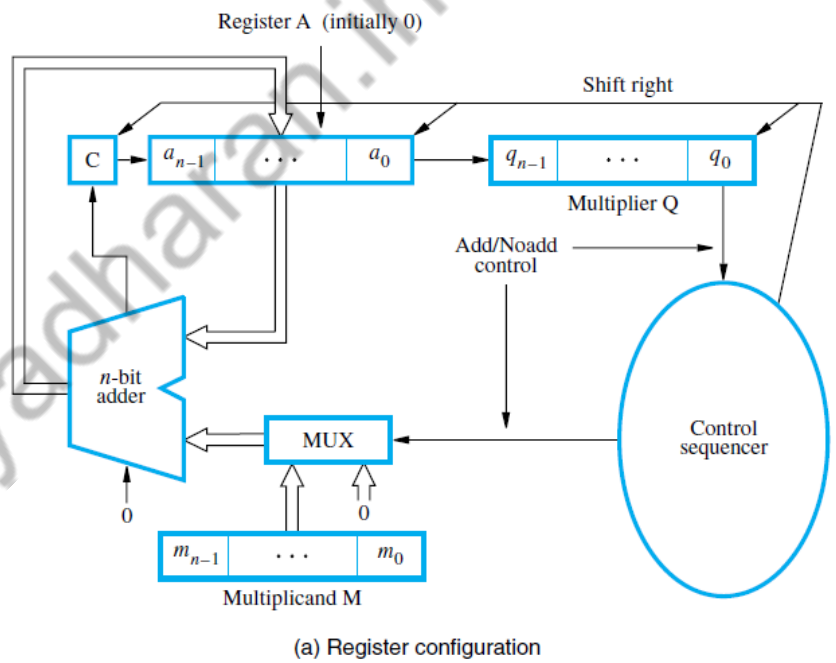
VLSI Architecture Example 2



VLSI Architecture Example 3



4-bit Parallel Multiplier



Booth's Algorithm Multiplier

Course Objectives

- To familiarize with various architectural techniques used in implementing complex logic functions as VLSI chips and to achieve various design objectives such as to meet high performance; low cost, high throughput, low-power or a combination thereof

- The course covers the architectural techniques and design methods used for designing programmable processors (CISC, RISC Processors).

Course Evaluation Components

No	Name	Type	Duration	Weight
EC-1	Quiz-I	Online		5%
	Assignment -1	Verilog based Arithmetic block design		15%
	Assignment-II	Sample Processor Design:		10%
EC-2	Mid-Semester Test	Closed Book	2 hours	30%
EC-3	Comprehensive Exam	Open Book	3 hours	40%

Thank you