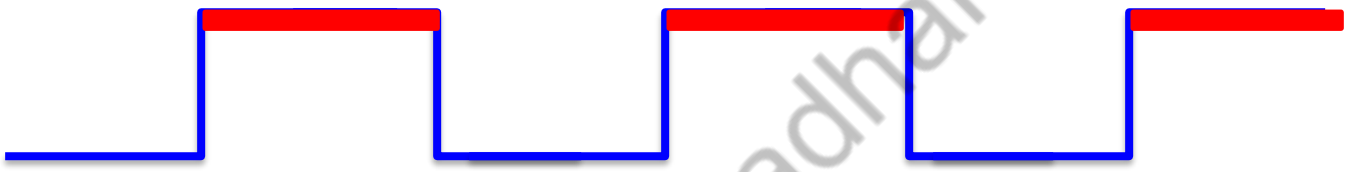
Digital Design : 2021-22
Lecture 18 : Sequential Logic – Flipflops

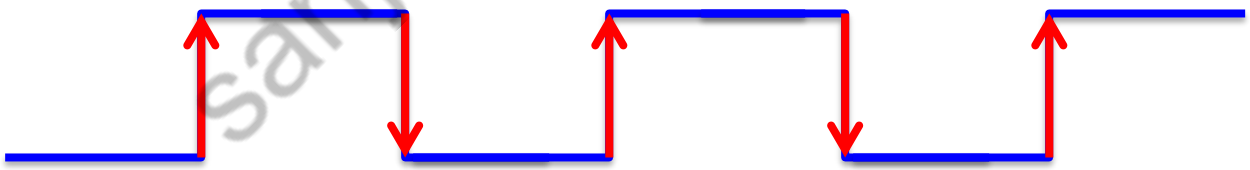
By Dr. Sanjay Vidhyadharan

Latch vs. Flip-flop

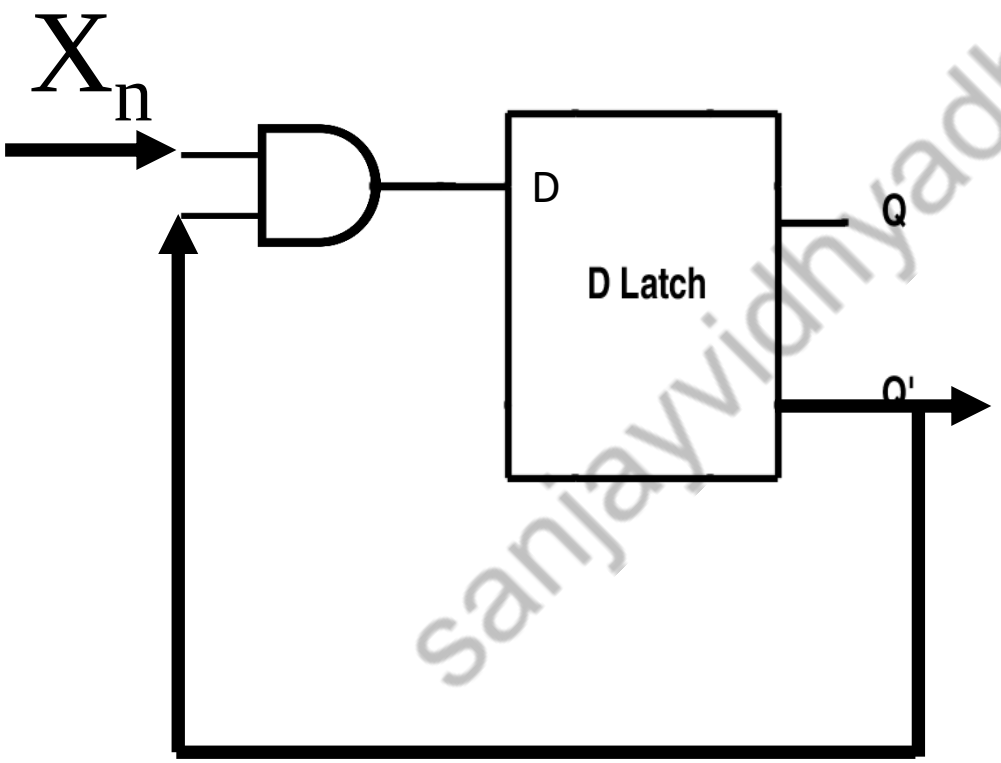
Latch – Responds to change in level of clock pulse



The key to the proper operation of a flip-flop is to trigger it only during signal transition.



Race around in Latches



$$Y_n = X_n \cdot X'_{n-1}$$

Flip-flops

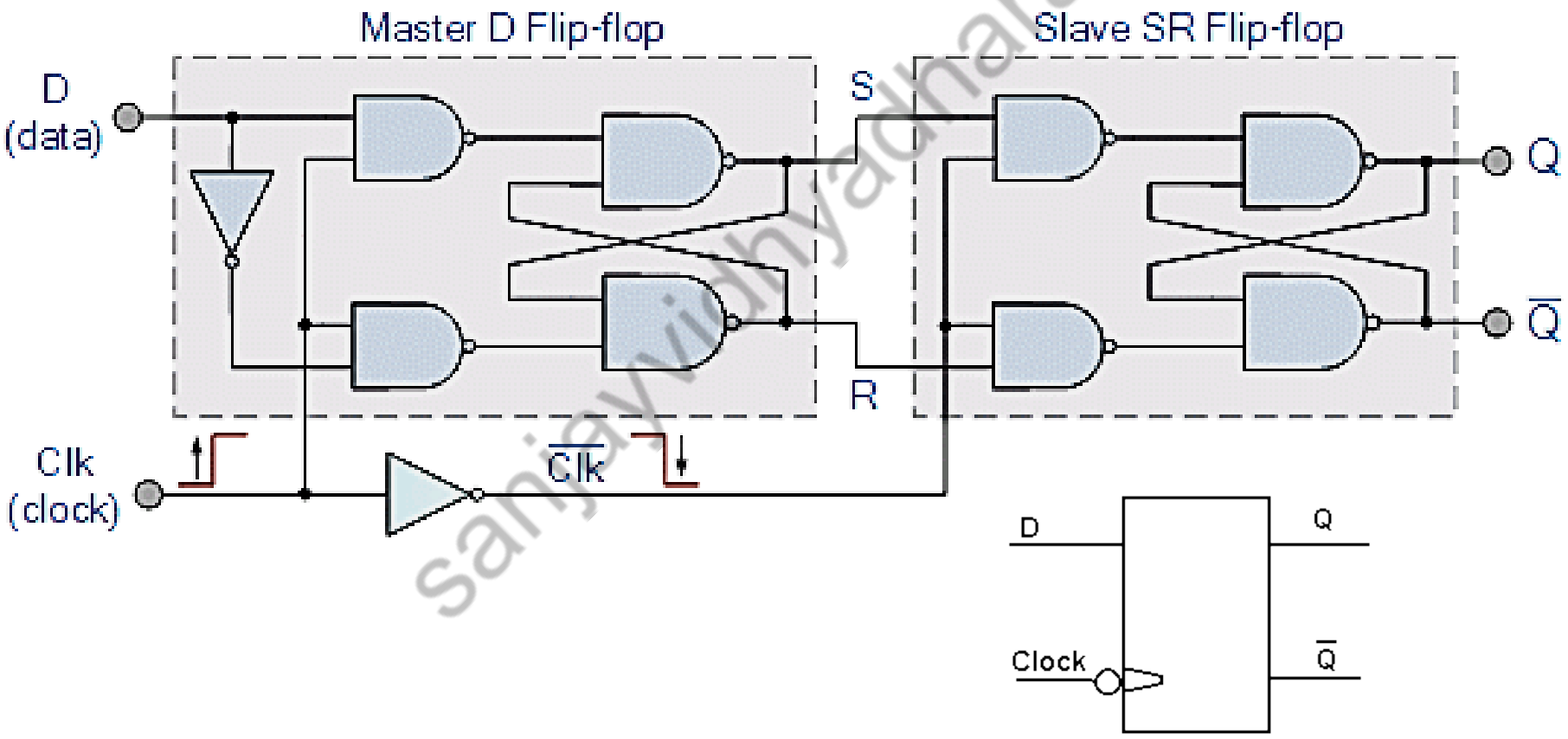
Two ways to build a flip flop

Special configuration of two latches to isolate the output of flip-flop

Gate based design which triggers only during signal transition of clock and is disabled during rest of clock pulse

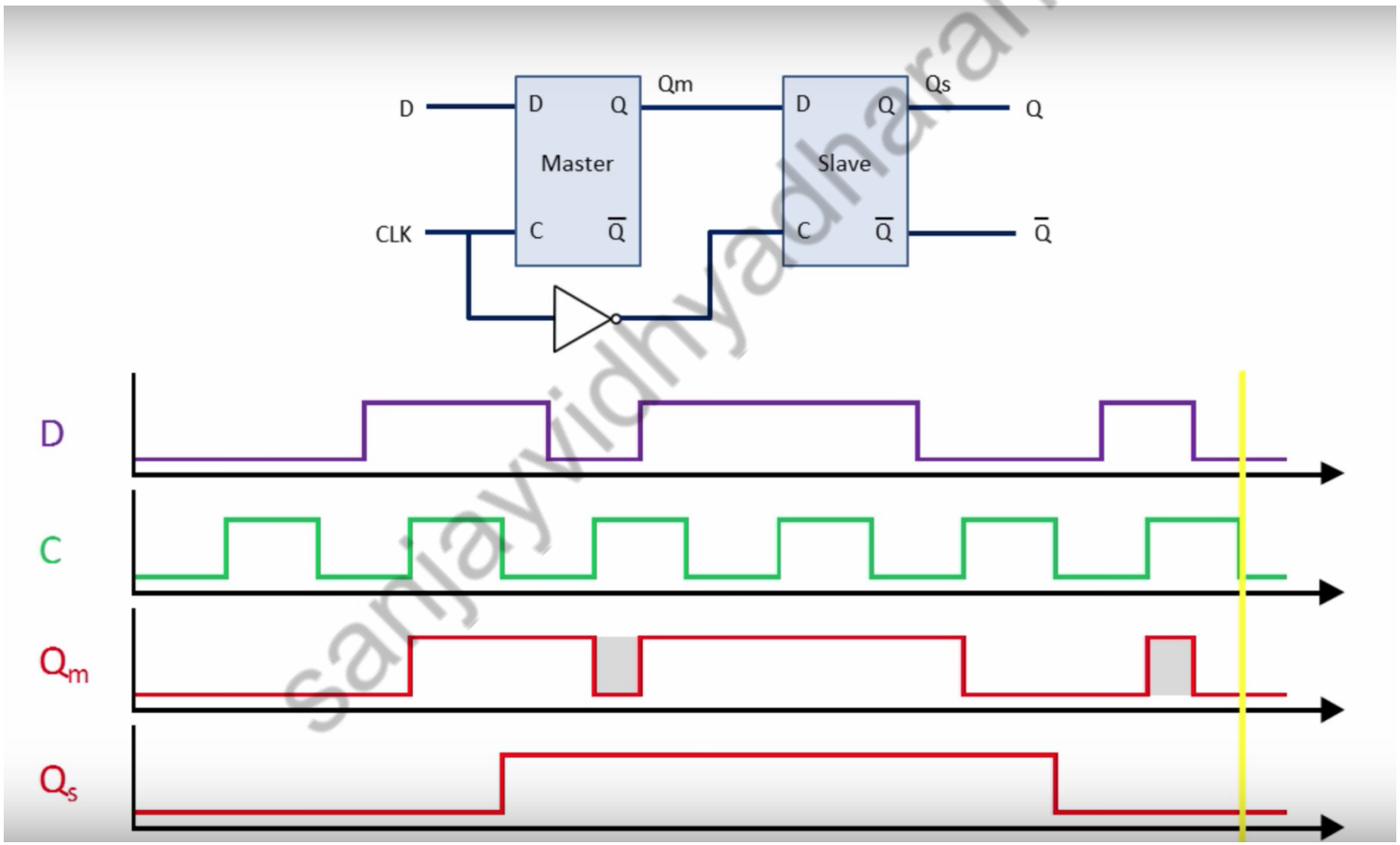
Flip-flops

Master-Slave Flip-flop



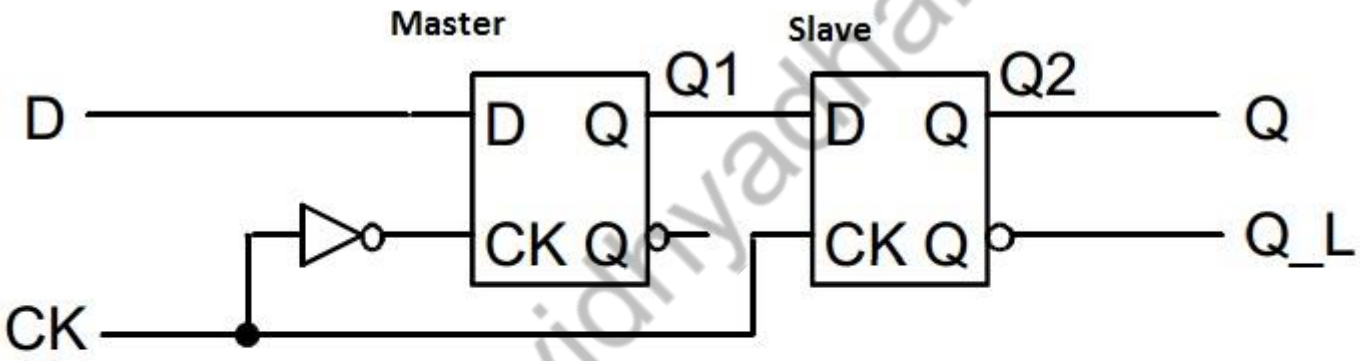
Flip-flops

Master-Slave Flip-flop



Flip-flops

Master-Slave Flip-flop

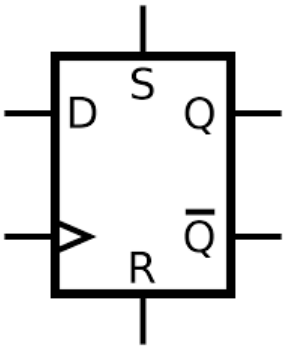


MASTER-SLAVE D FLIP FLOP

i) Positive edge triggered

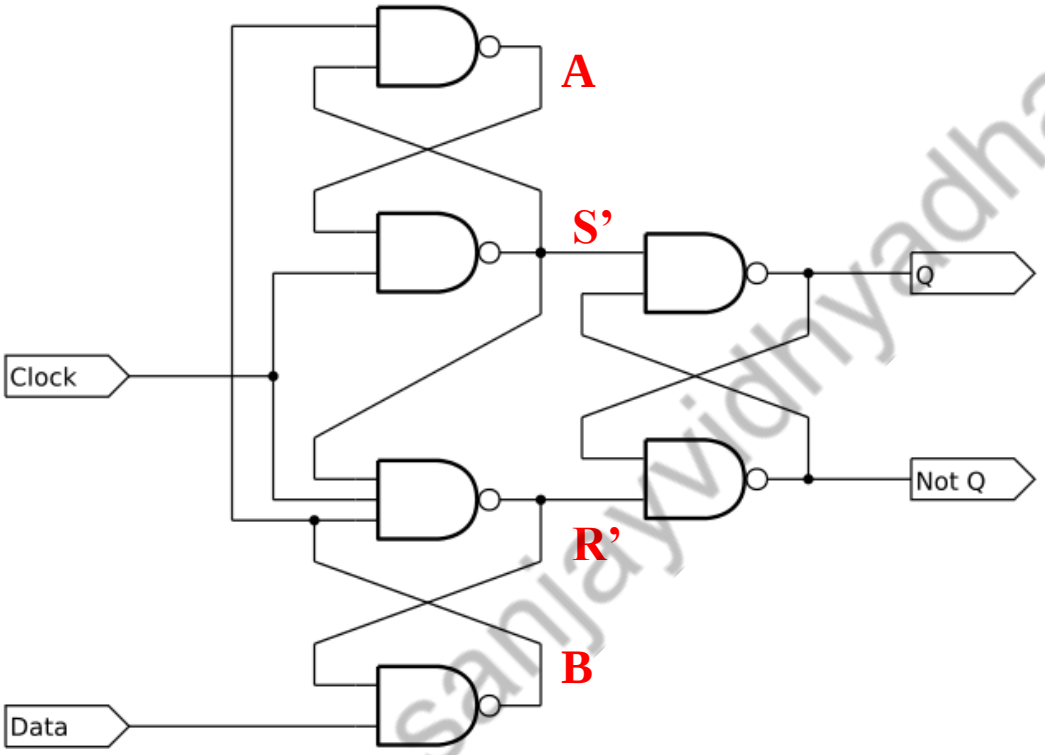
ii) Note that Slave is controlled by Clk and Master by Clk'

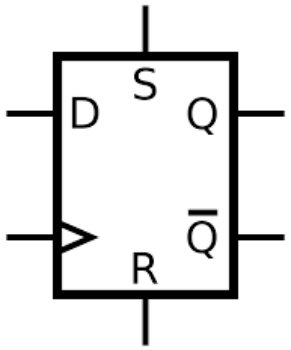
iii) In Negative Edge Triggered, Master is run with Clk



Edge Triggered D Flip-Flops

D-type positive edge triggered





Case I:

CLK = 0

CLK = 0 => S'=1, R'=1

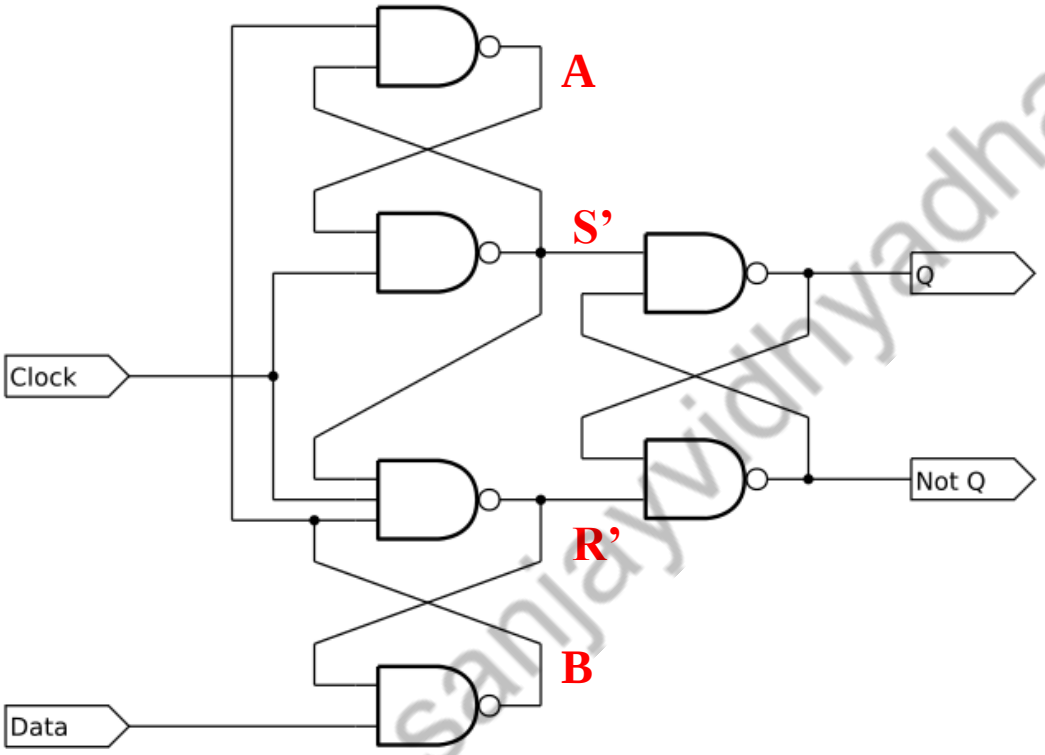
D = 0 ->1 -> 0

S' = 1, R' = 1 for S'R' latch

Hence Previous state of Q and Q' is maintained

Edge Triggered D Flip-Flops

D-type positive edge triggered



Case 2:

CLK = 1 , D=0, S'=1, R'=0
B=1, A=0

D -> 0 -> 1 -> 0
B =1 Since R'=0

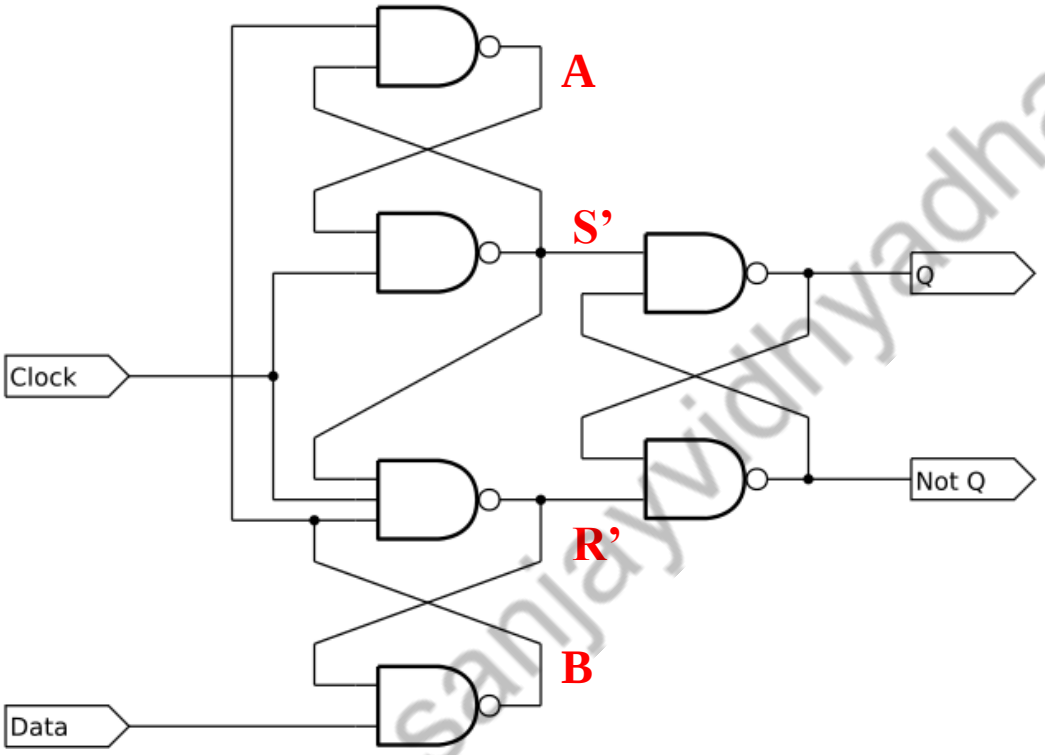
Case 3:

CLK = 1 , D=1, S'=0, R'=1
B=0, A=1
D -> 1 -> 0-> 0
B -> 0-> 1> 0
R'=1 Since S'=0
A=1 Since S'=0

Hence Initial state of Q and Q' is maintained

Edge Triggered D Flip-Flops

D-type positive edge triggered



Case 4:

CLK = 0 , D=0, S'=1, R'=0

B=1, A=1, Q=0

D ->1

B=0

CLK->1

R'=1

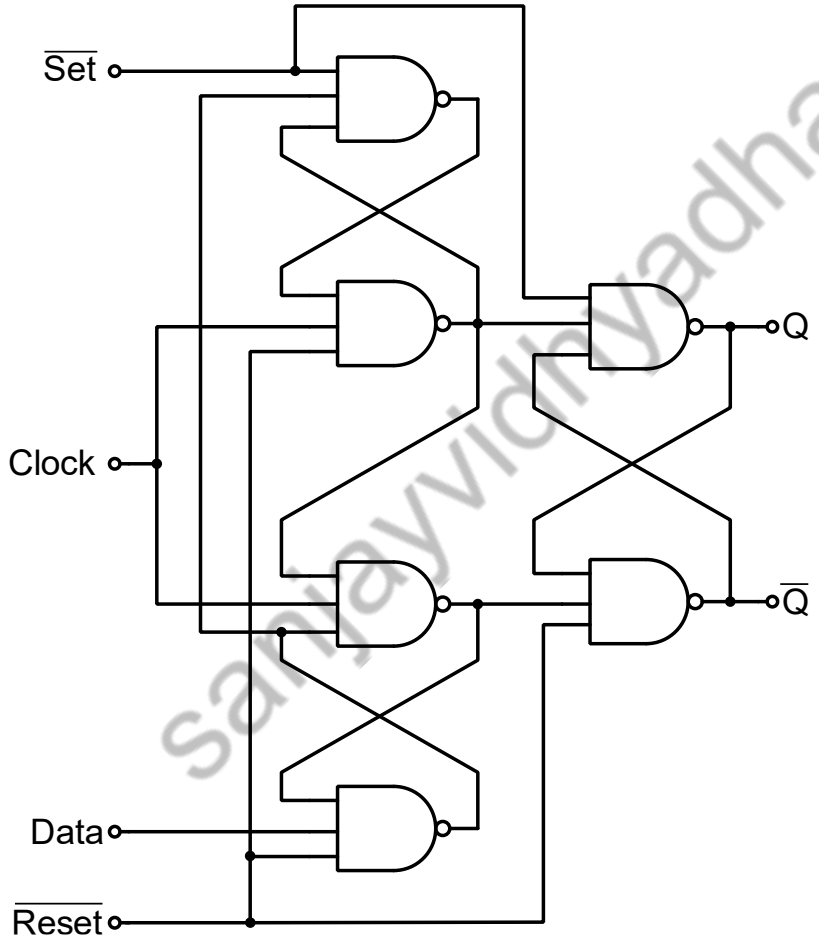
A=1

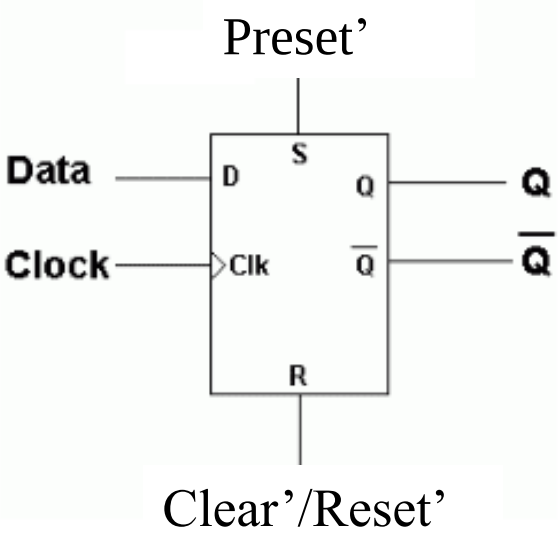
S'=0

Q=1

Edge Triggered D Flip-Flops

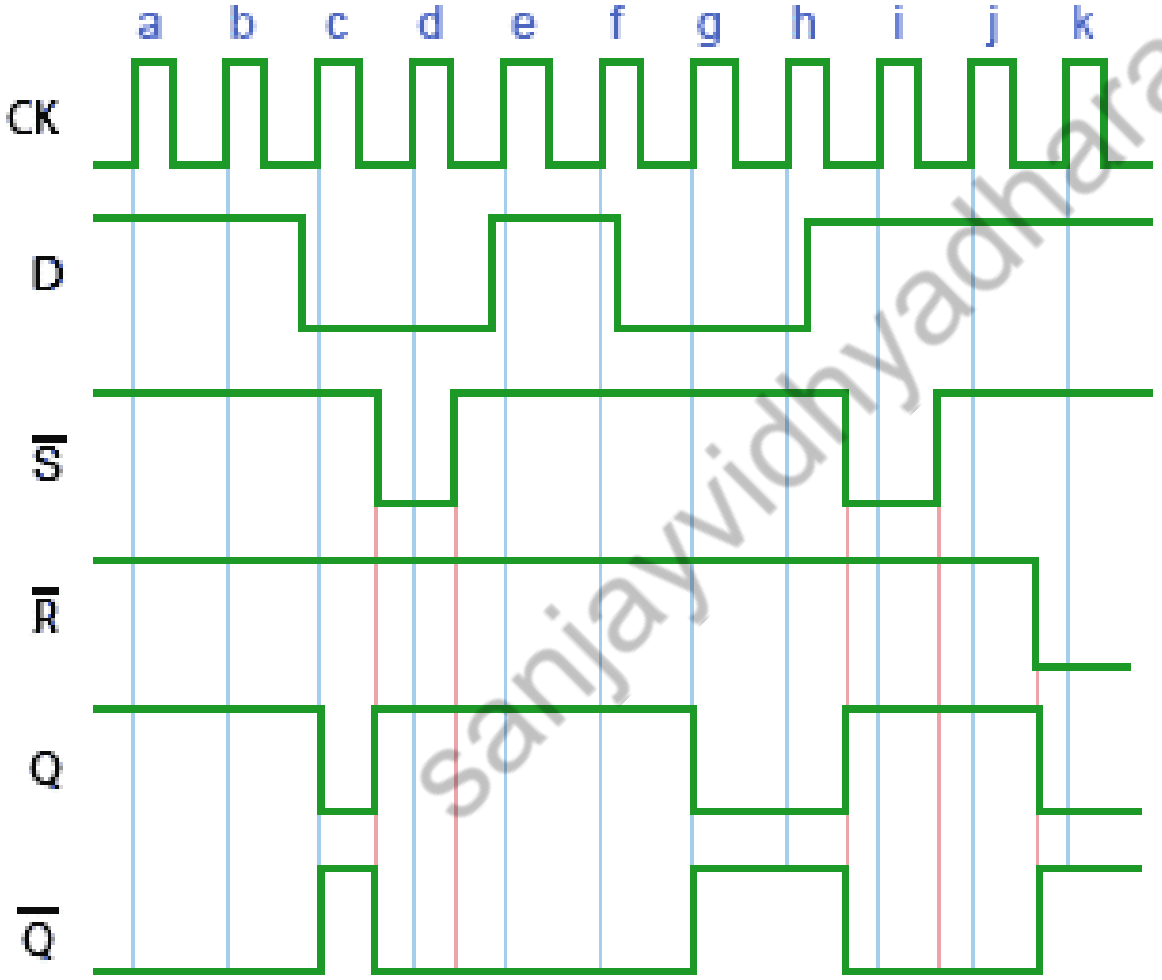
D-type positive edge triggered

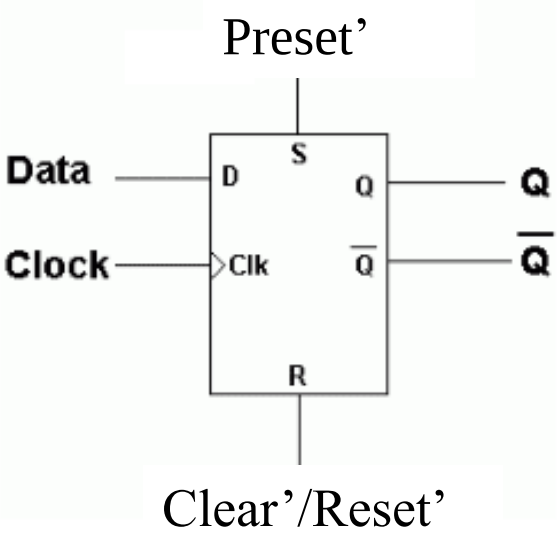




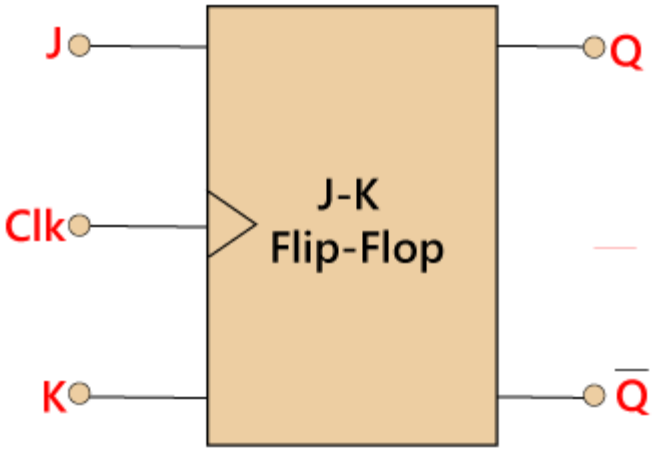
Edge Triggered D Flip-Flops

D-type positive edge triggered





JK Flip-Flop



Characteristic Table

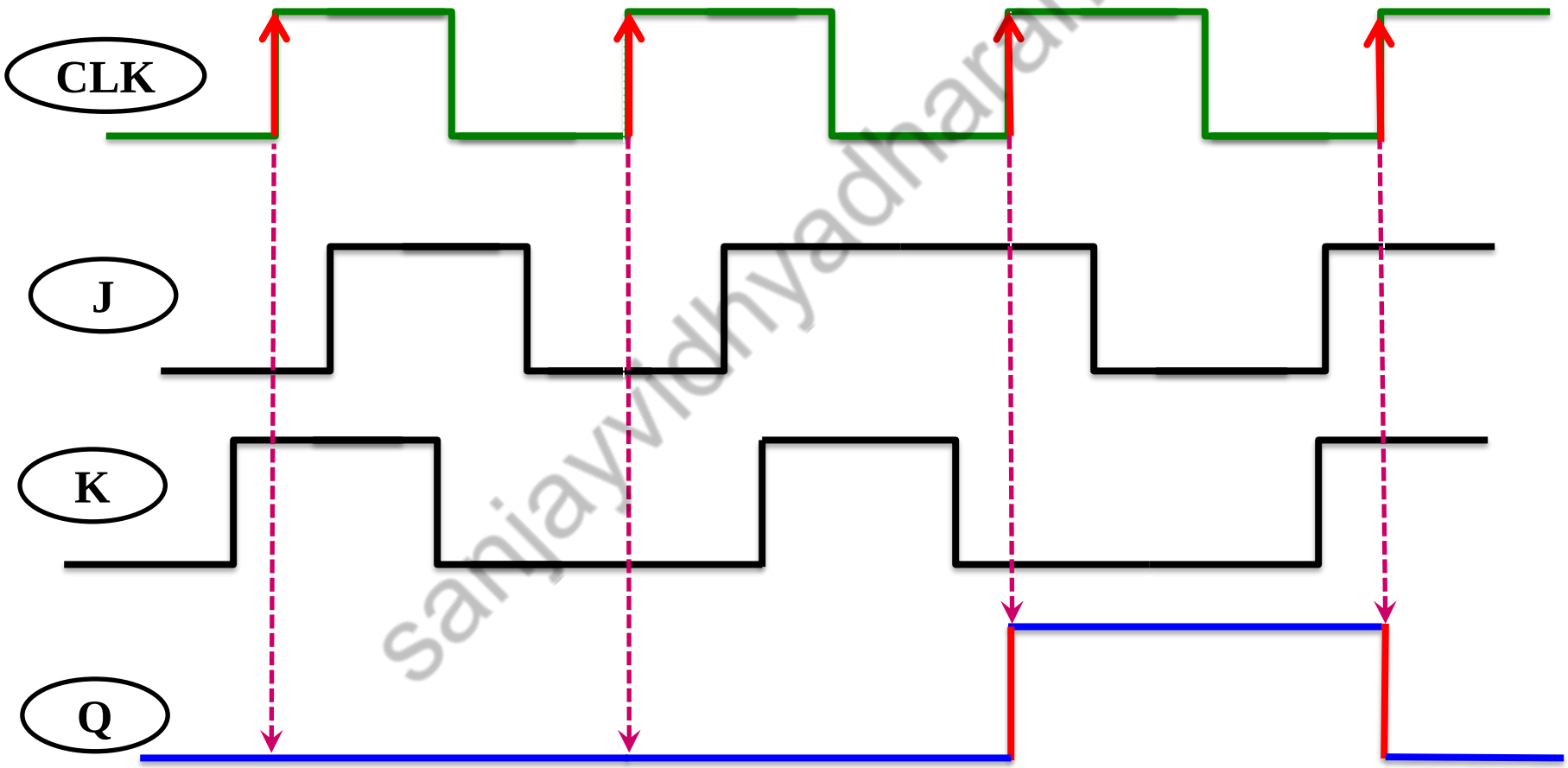
J	K	Q(t+1)	
0	0	Q(t)	No Change
0	1	0	Reset
1	0	1	Set
1	1	Q'(t)	Toggle/Complement

Characteristic Equation??

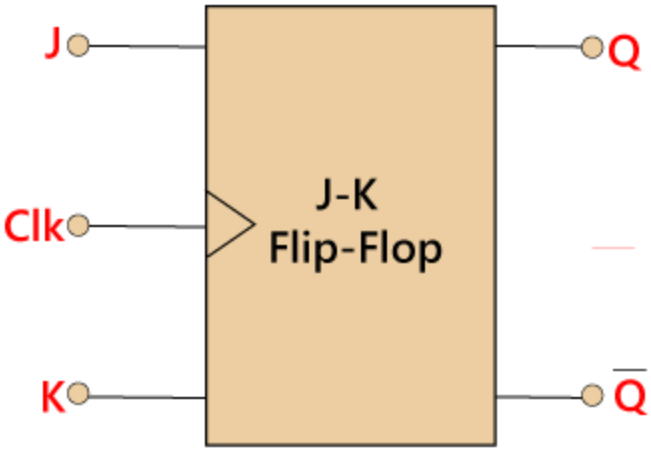
$$Q(t+1) = JQ' + K'Q$$

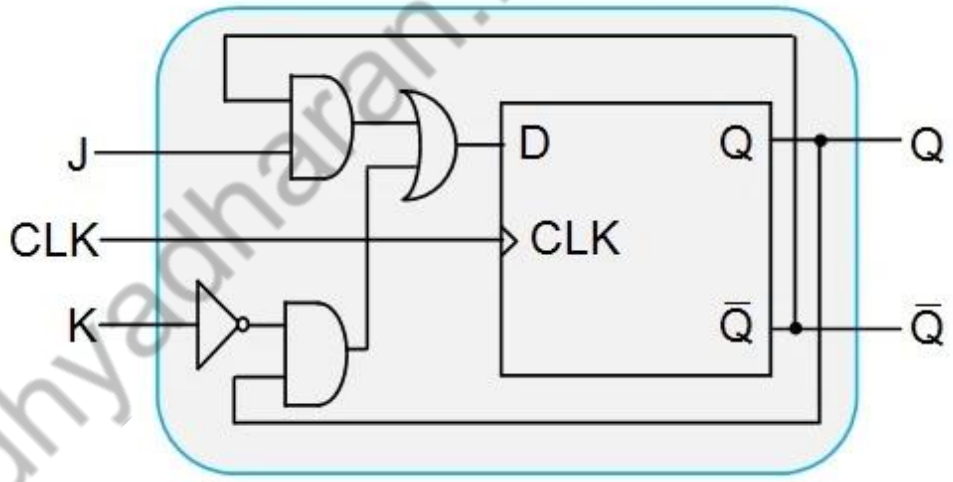
JK Flip-Flop

Positive Edge triggered



JK Flip-Flop



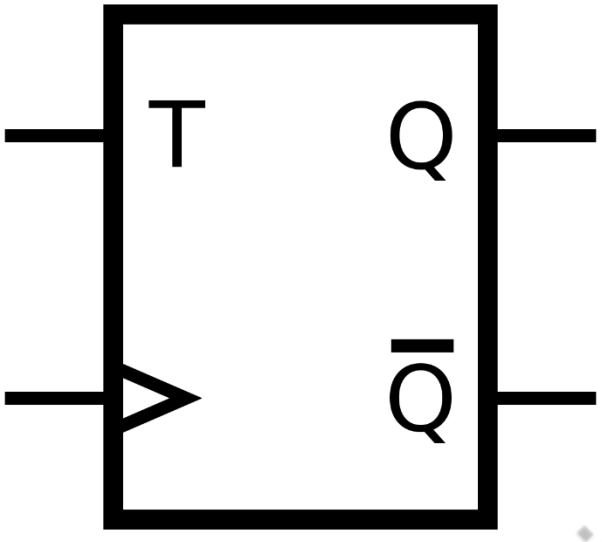


Design J-K Flip-flop using D flip-flop

$Q(t+1) = D$

$Q(t+1) = JQ' + K'Q$

T Flip-Flop



Characteristic Table

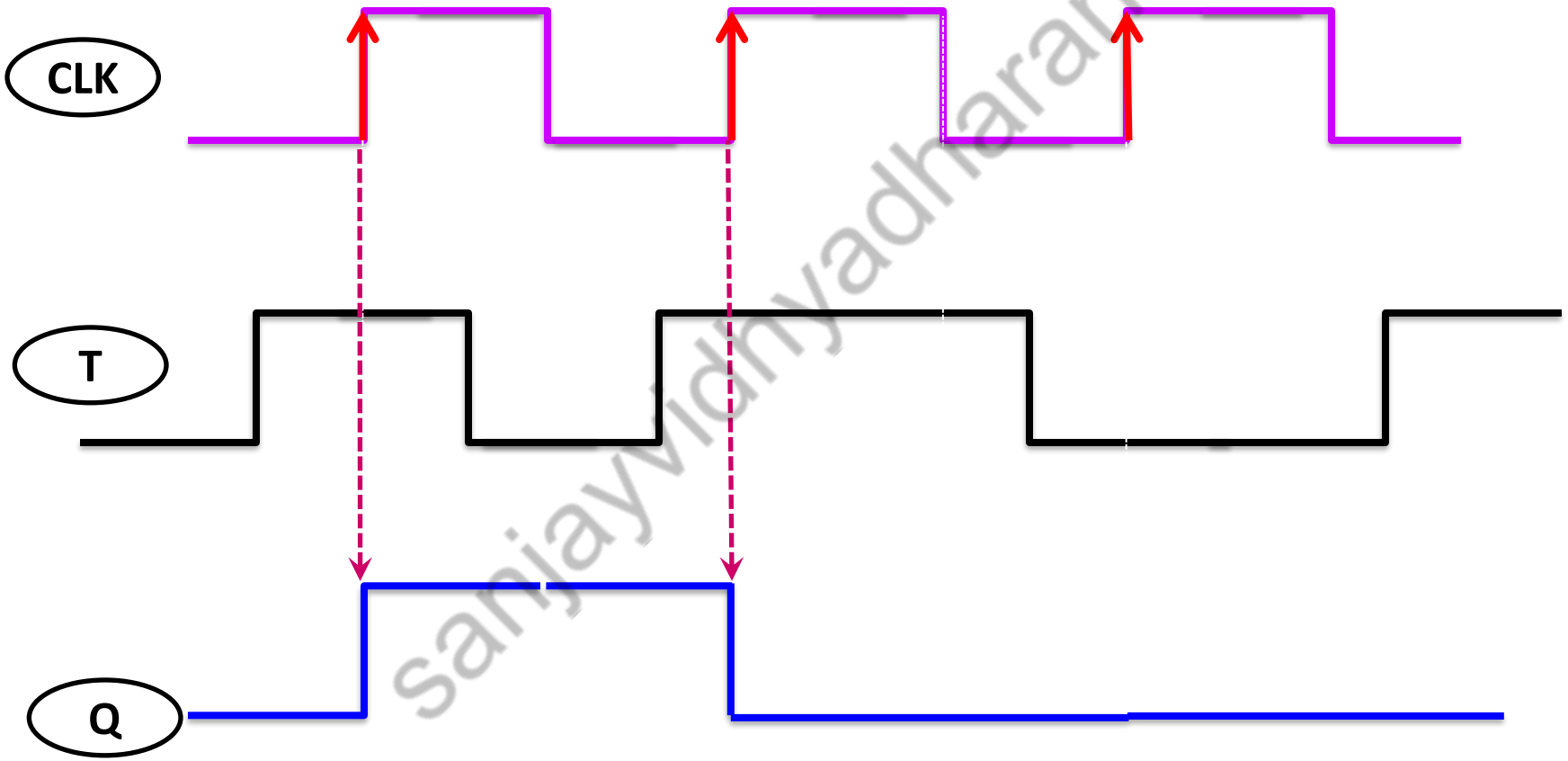
T	Q(t+1)	
0	Q(t)	No Change
1	Q'(t)	Toggle

Characteristic Equation??

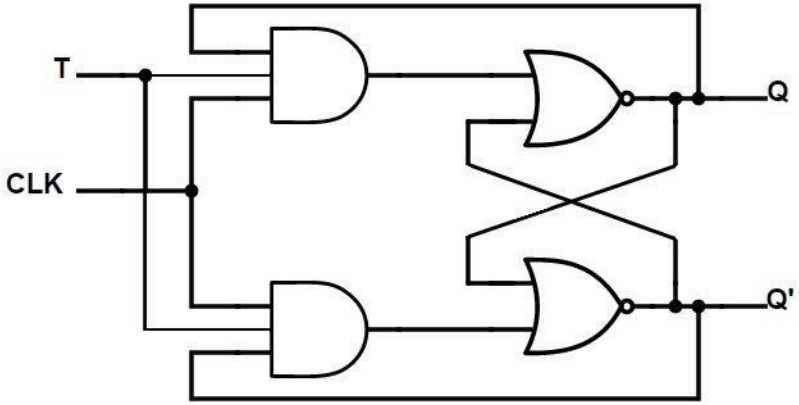
$$Q(t+1) = T \oplus Q$$

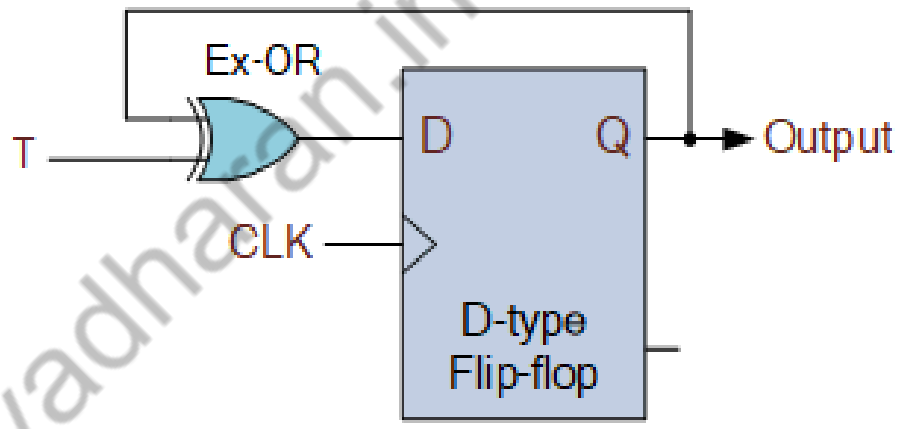
T Flip-Flop

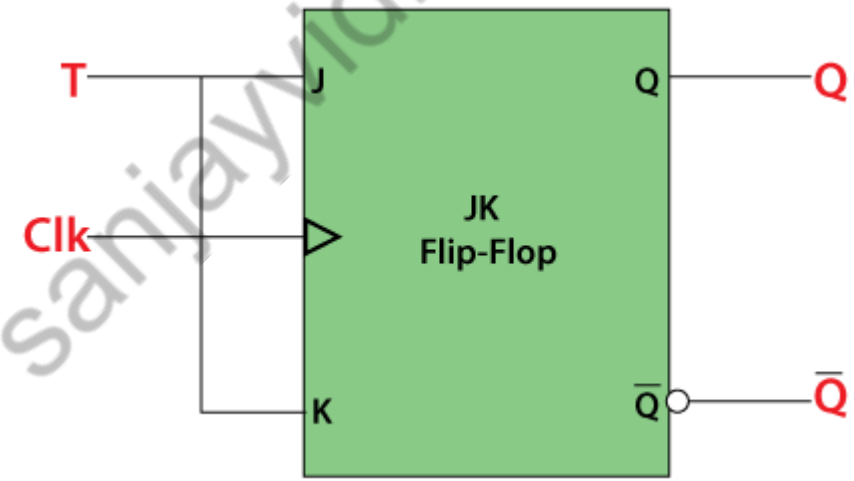
Positive Edge triggered



T Flip-Flop







Thank you