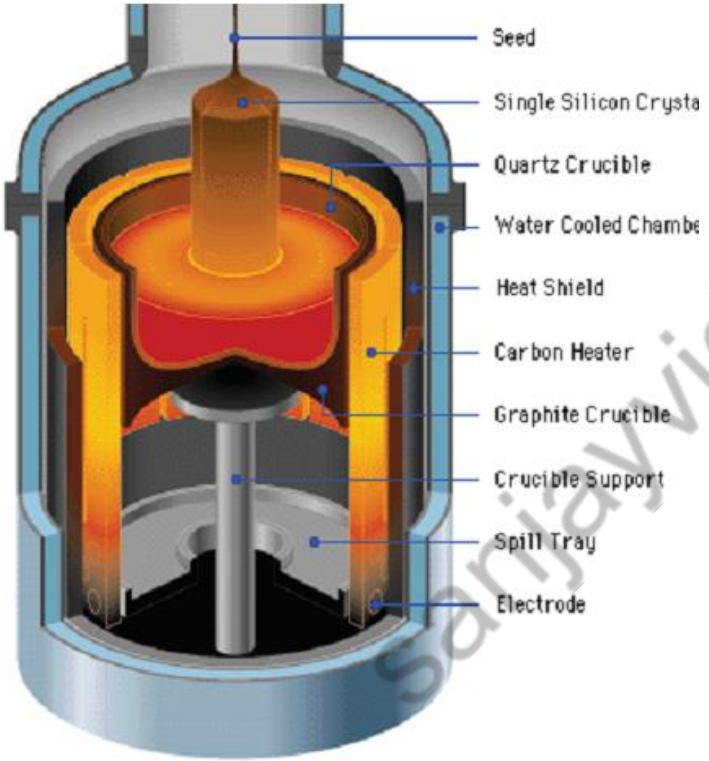
VLSI Design : 2021-22
Lecture 4
CMOS Technology

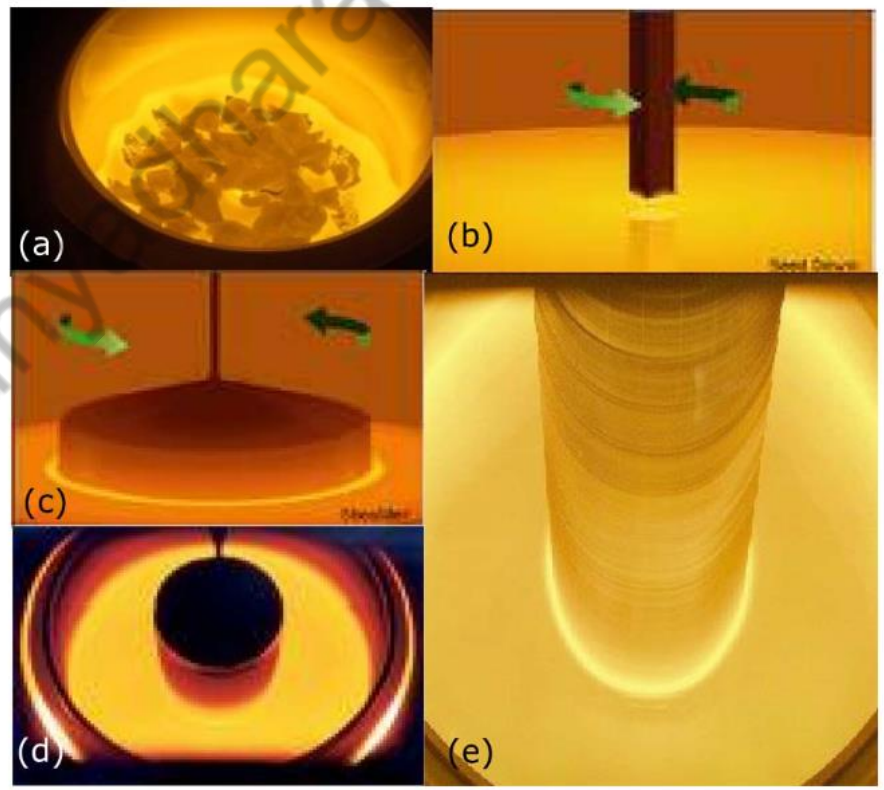
By Dr. Sanjay Vidhyadharan

Crystal Growth

99.999999999% pure Si is needed for IC fabrication!!

i.e.,1mg of sugar dissolved in an Olympic-size swimming pool



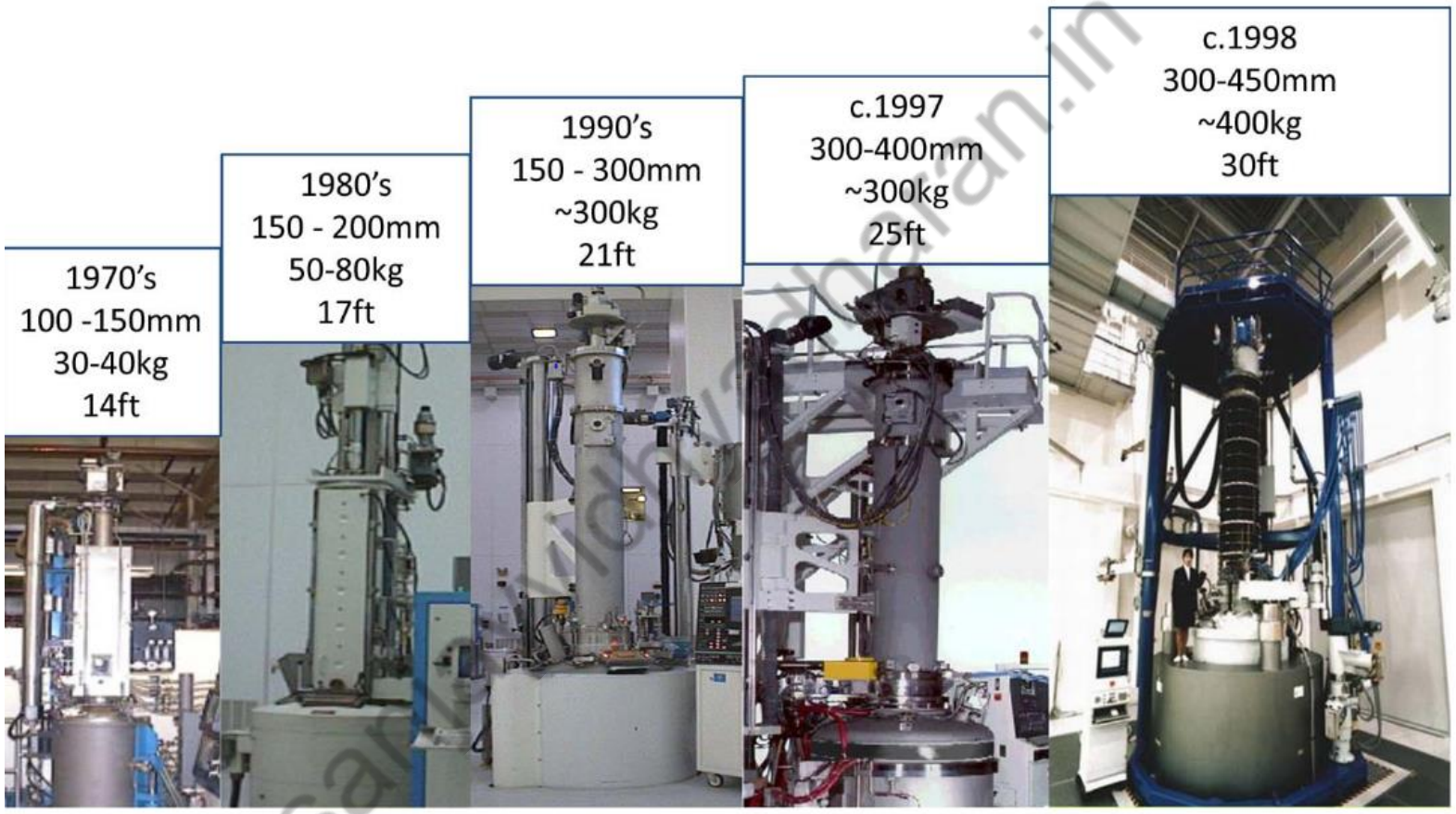


https://www.youtube.com/watch?v=skRmyhSOu28

Crystal Growth

https://www.youtube.com/watch?v=skRmyhSOu28

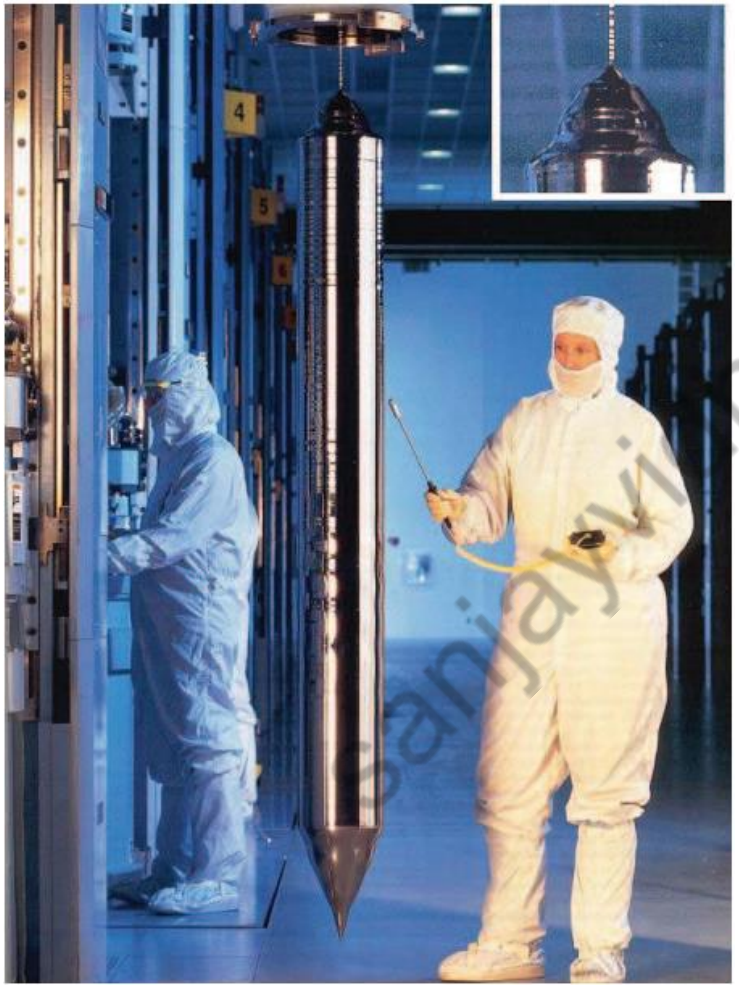
Silicon Ingot

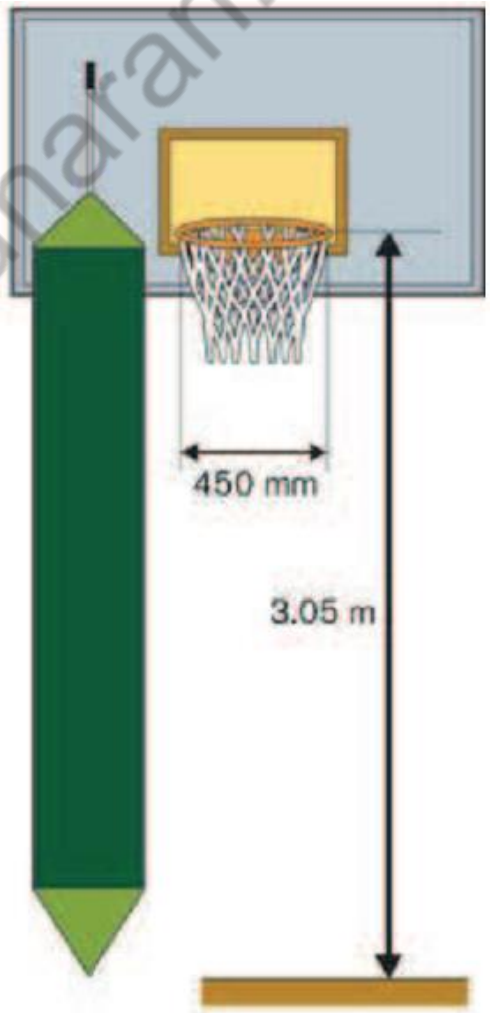


Examples of progress in Czochralski crystal puller

Silicon Ingot

In 2017, the wafer diameter has reached 18 inch (i.e., 450 mm) and weight is several hundred kilograms



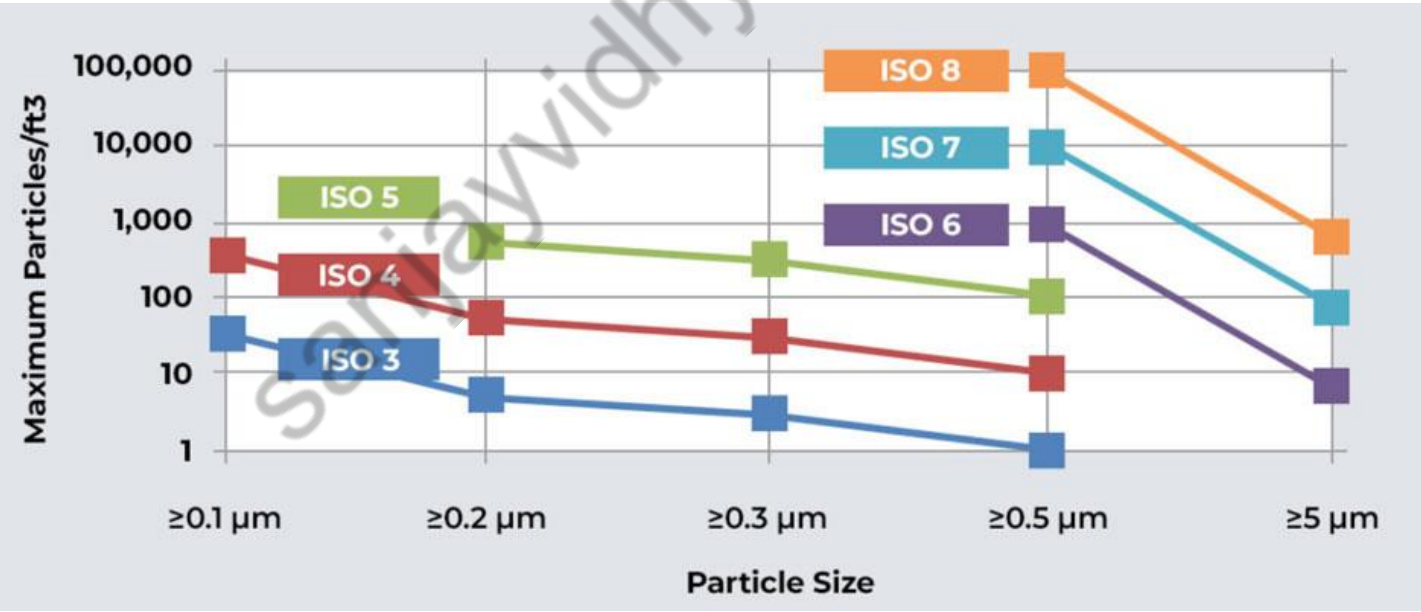


Choosing a Substrate

- **Type of the substrate (p- or n-type)?**
  - **Prefer P-type**
- **Resistivity or doping level?**
  - **Substrate doping level 10^{15} cm^{-3} → resistivity 25-50 ohm-cm**
- **Crystal orientation (111) or (100)?**
  - **Prefer (100) surface in order to have better Si/SiO_2 interface and few imperfection (i.e., unsatisfied bonds)**

Cleanroom

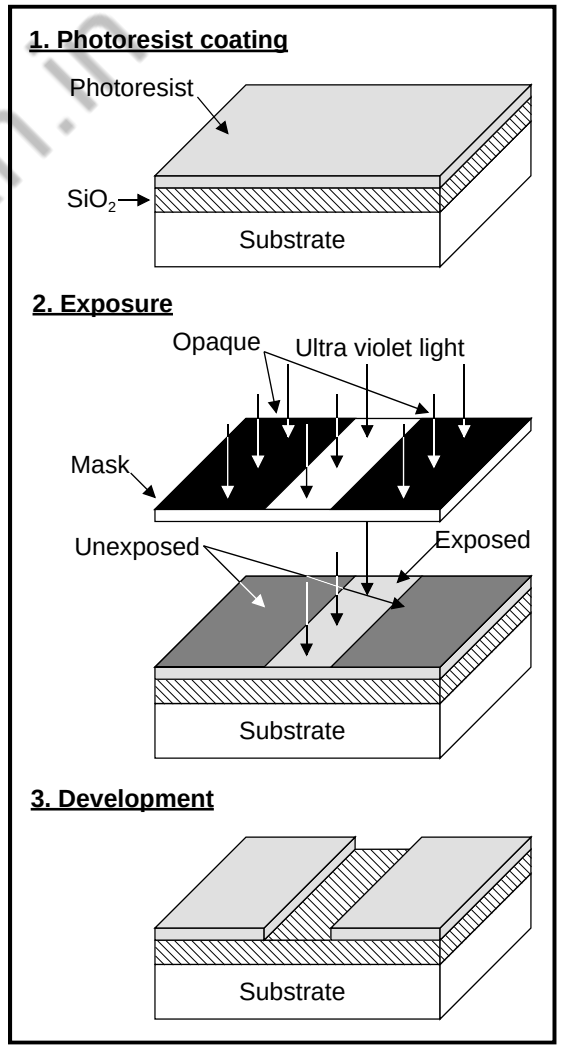
- Ambient air contains 35,000,000 particles per cubic meter with 0.5 mm and larger in diameter!
- Clean Room : It is a controlled environment with low level of pollutants such as dust, airborne microbes, aerosol particles, and chemical vapors.
- Semiconductor fabs follow the ISO 14644 standard. Specification for device fabrication cleanrooms vary based on process type, line width, and wafer size requirements. Semiconductor cleanrooms requirements can range from ISO-4 (Class 10) to ISO-6 (Class 1,000) cleanrooms.



Lithography

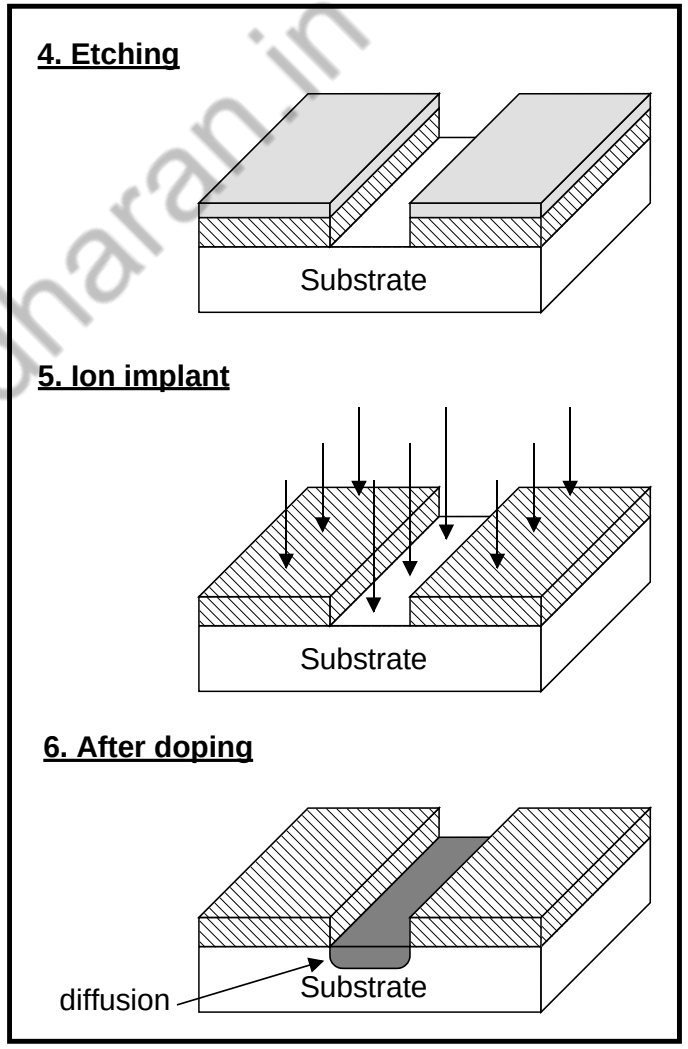
Basic sequence

- The surface to be patterned is:
  - spin-coated with photoresist
  - the photoresist is dehydrated in an oven (photo resist: light-sensitive organic polymer)
- The photoresist is exposed to ultra-violet light:
  - For a positive photoresist exposed areas become soluble and non exposed areas remain hard
- The soluble photoresist is chemically removed (development).
  - The patterned photoresist will now serve as an etching mask for the SiO_2



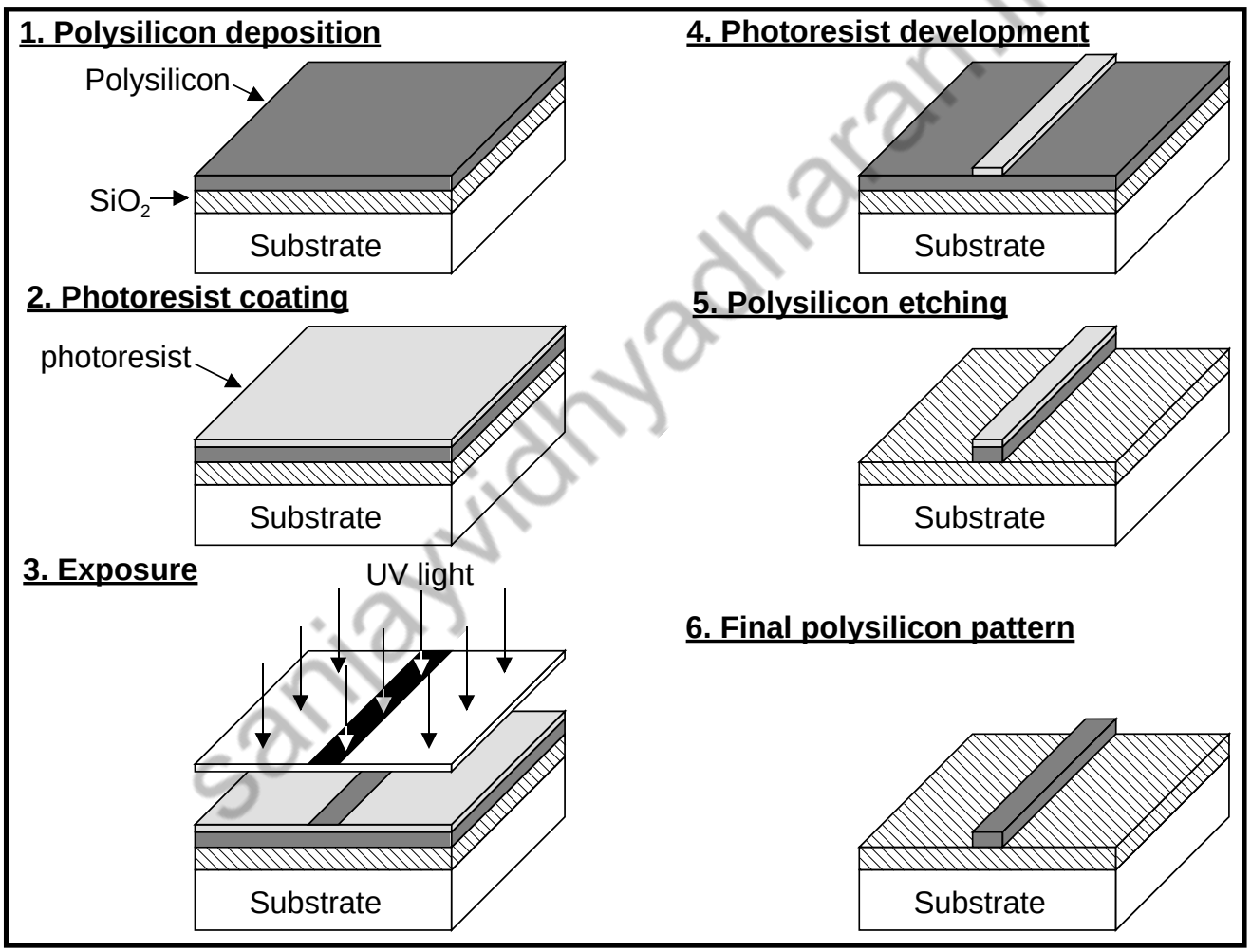
Lithography

- The SiO_2 is etched away leaving the substrate exposed:
  - the patterned resist is used as the etching mask
- Ion Implantation:
  - the substrate is subjected to highly energized donor or acceptor atoms
  - The atoms impinge on the surface and travel below it
  - The patterned silicon SiO_2 serves as an implantation mask
- The doping is further driven into the bulk by a thermal cycle



Lithography

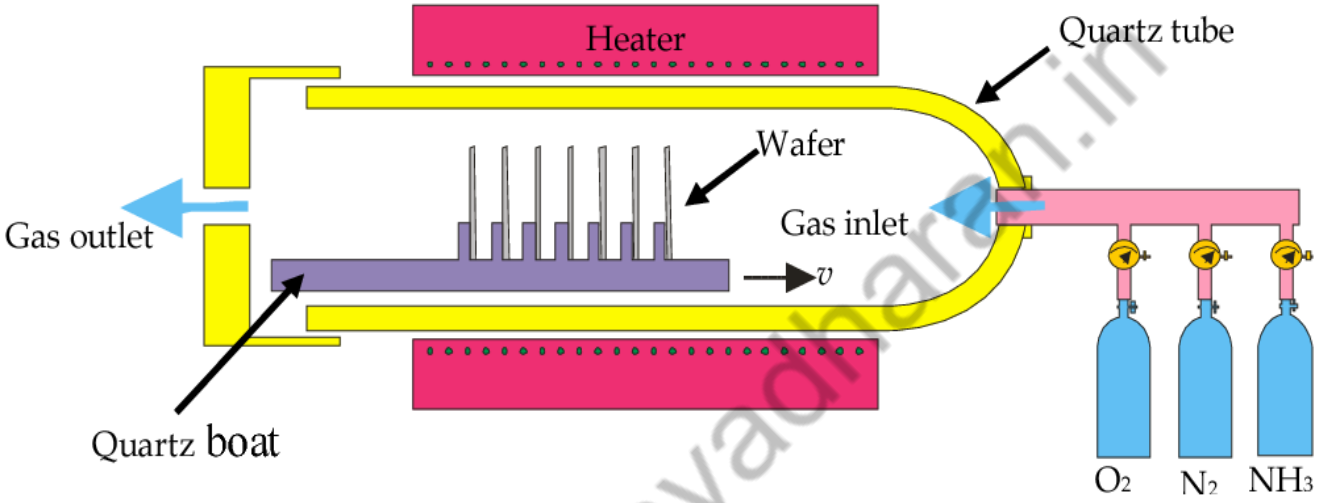
Patterning a layer above the silicon surface



Basic VLSI Fabrication Steps

1. **Crystal growth**
   - **Crystal orientation, type and resistivity**
2. **Photolithography**
3. **Oxidation**
   - **Dry or wet oxidation, duration of oxidation**
4. **Diffusion**
5. **Epitaxy**
6. **Ion-implantation**
7. **Annealing**
8. **Metallization**

Oxidation



Wet oxidation : $Si + 2H_2O \rightarrow SiO_2 + 2H_2$

This process is done by 900 to 1000 °C.

The characteristics if wet thermal oxidation are:

- fast growth even on low temperatures
- less quality than dry oxides

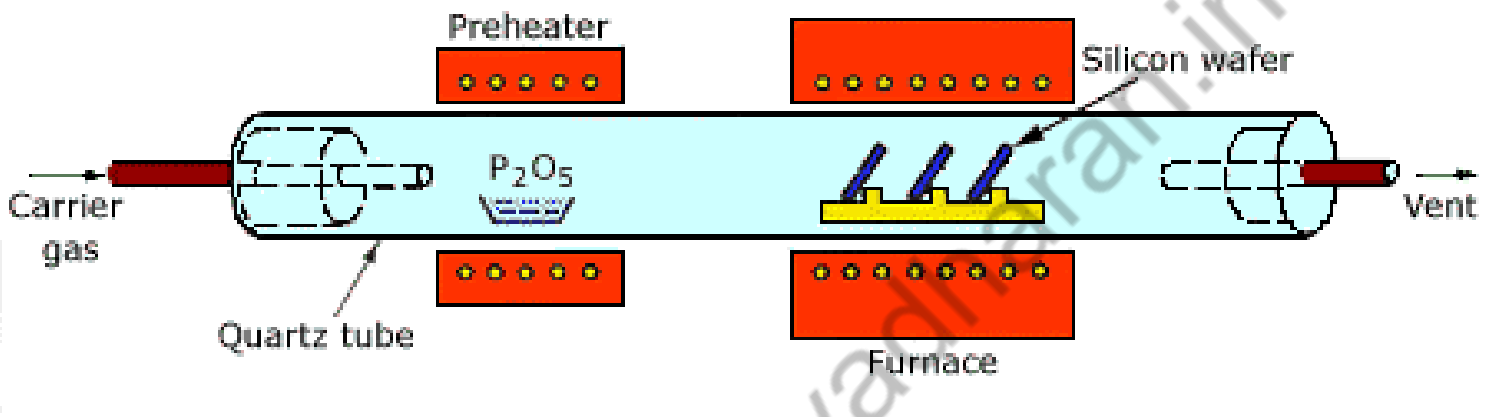
Dry oxidation $Si + O_2 \rightarrow SiO_2$

This process is done at 1000 to 1200 °C actually. To create a very thin and stable oxide the process can be done at lower temperatures of about 800 °C.

Characteristic of the dry oxidation:

- slow growth of oxide
- high density
- high breakdown voltage

Diffusion



Fick's Laws

Element	D_o (cm^2/s)
B	10.5
Al	8.00
Ga	3.60
In	16.5
P	10.5
As	0.32
Sb	5.60

$$J = -D\frac{d\varphi}{dx}$$

Where,

J: diffusion flux

D: diffusivity

φ: concentration

x: position

$$\frac{\partial\varphi}{\partial t} = D\frac{\partial^2\varphi}{\partial x^2}$$

Where,

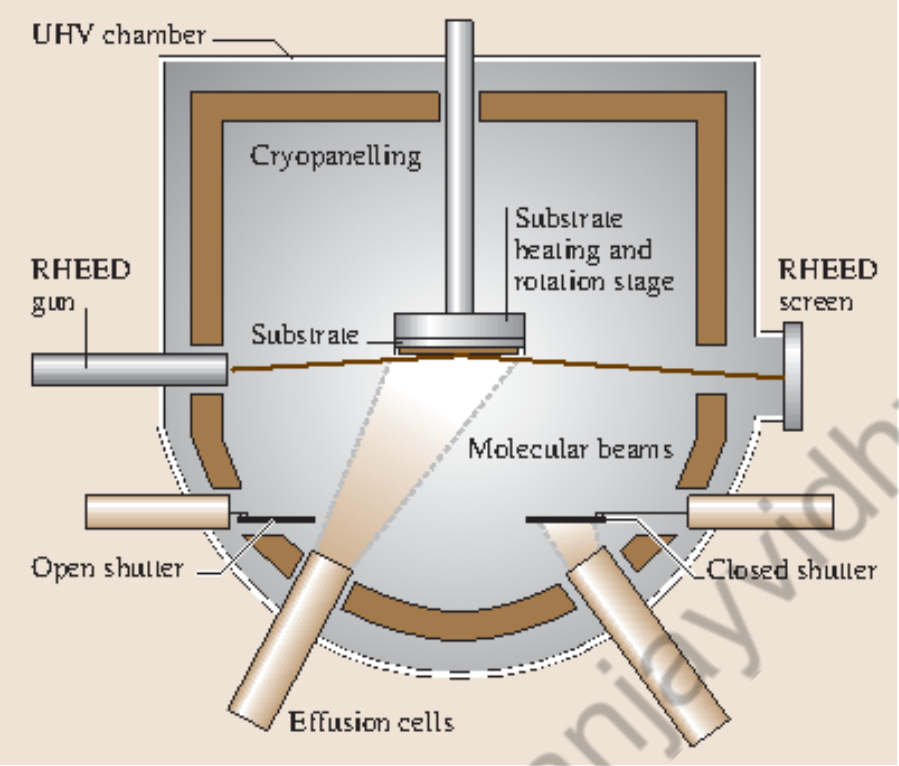
D: diffusivity

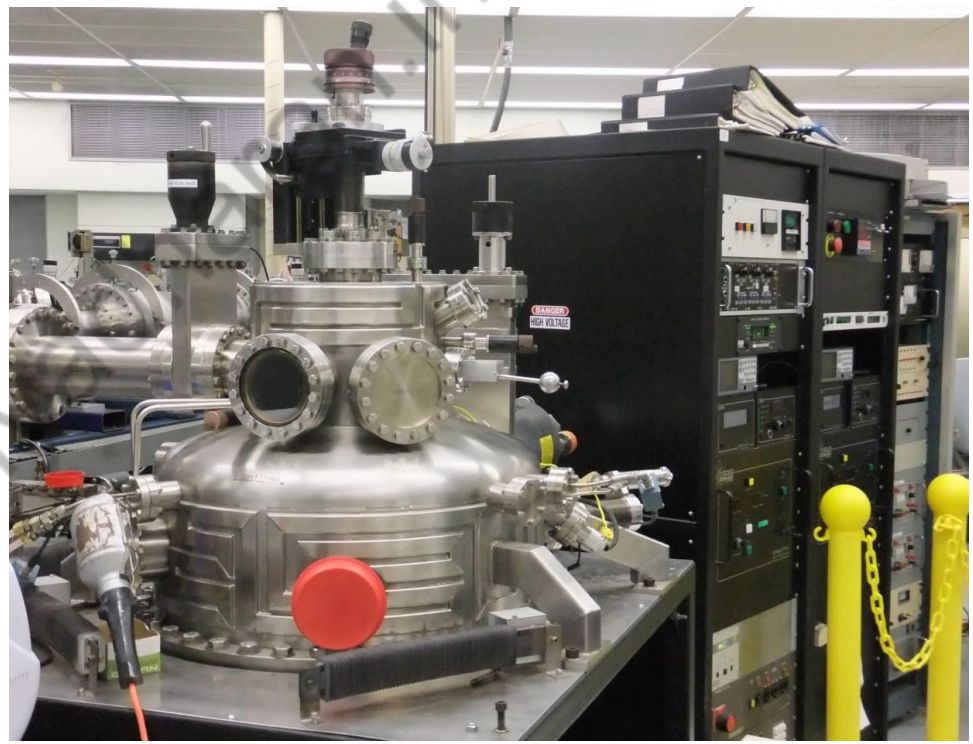
t: time

x: position

Φ: concentration

Epitaxy





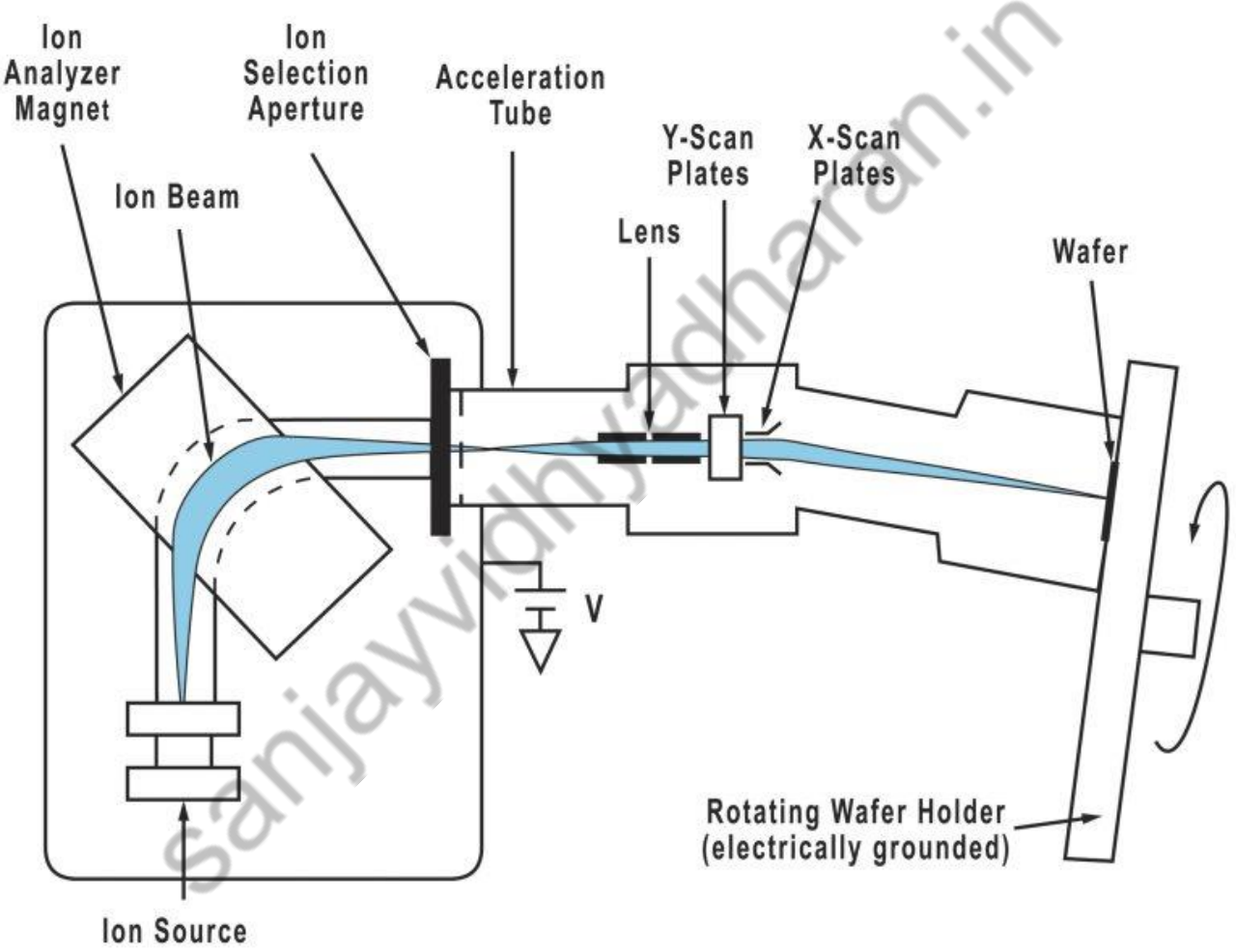
Reflection high energy electron diffraction

Epitaxy

The chemical reactions used for the production of undoped and doped epitaxial silicon and $Si_{1-x}Ge_x$ include:

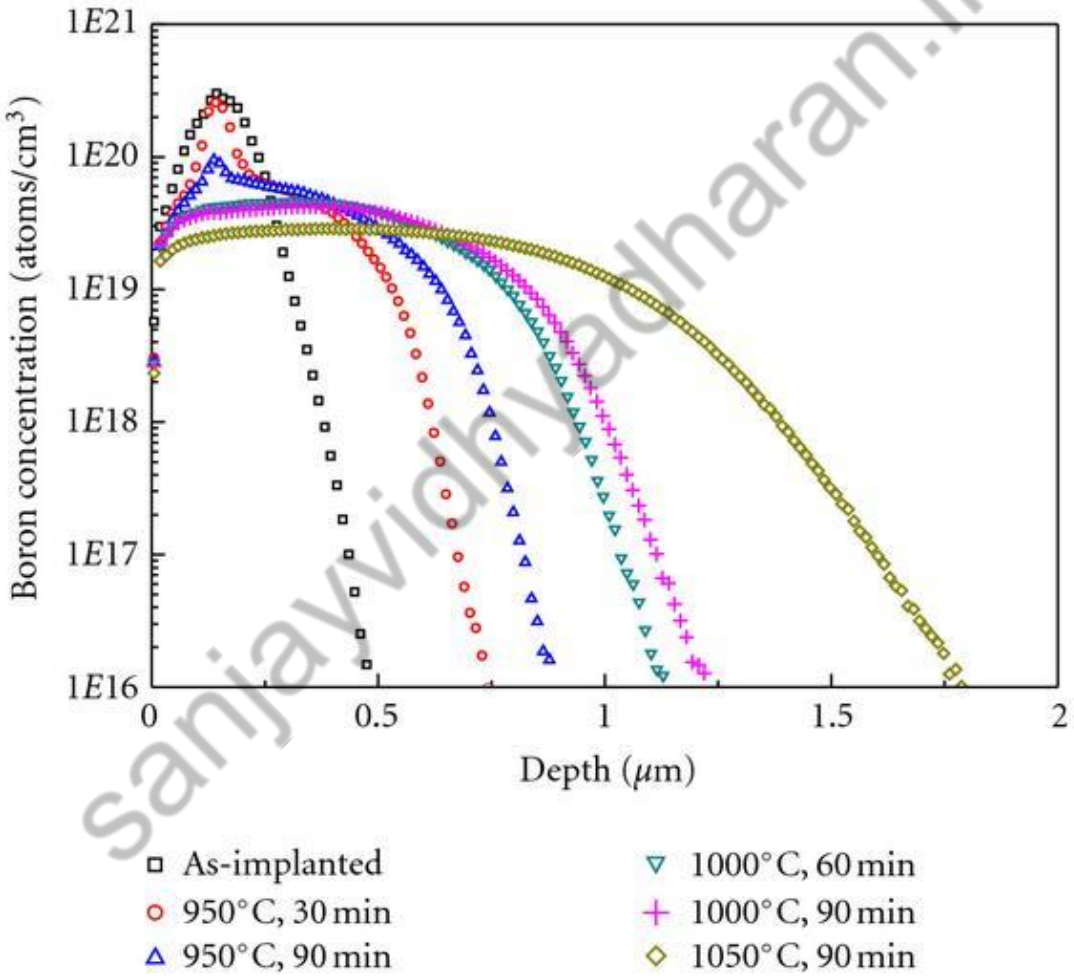
- $SiCl_4 + 2H_2 \rightarrow Si + 4HCl$ (~1200°C)
- $SiHCl_3 + H_2 \rightarrow Si + 3HCl$ (~1150°C)
- $SiH_2Cl_2 \rightarrow Si + 2HCl$ (~1100°C)
- $SiH_4 \rightarrow Si + 2H_2$ (~1050°C)
- $GeH_4 \rightarrow Ge + 2H_2$
- $B_2H_6 \rightarrow 2B + 3H_2$
- $PH_3 \rightarrow P + 3/2H_2$
- $AsH_3 \rightarrow As + 3/2H_2$

Ion-implantation

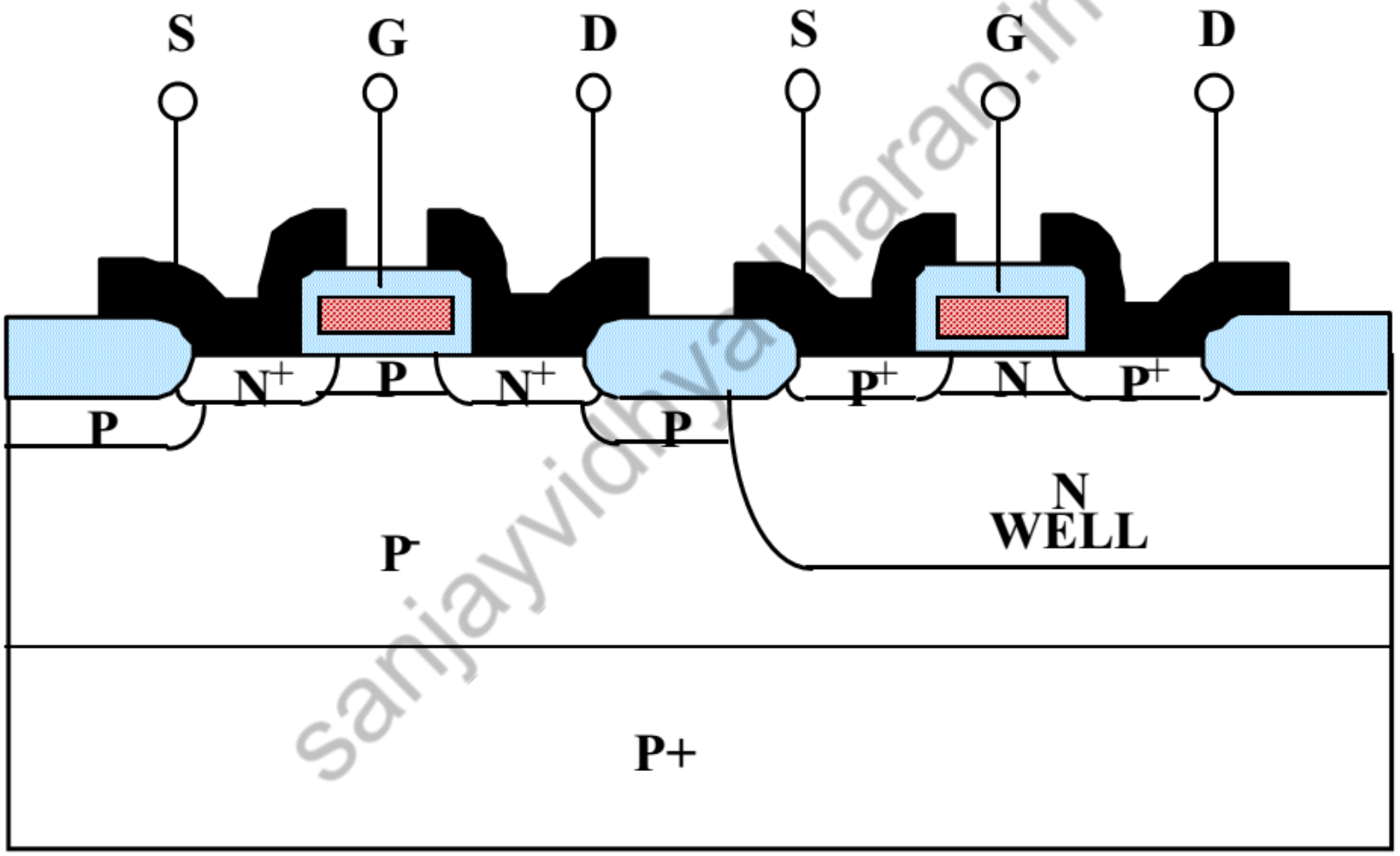


Ion-implantation

Annealing



How do you fabricate??



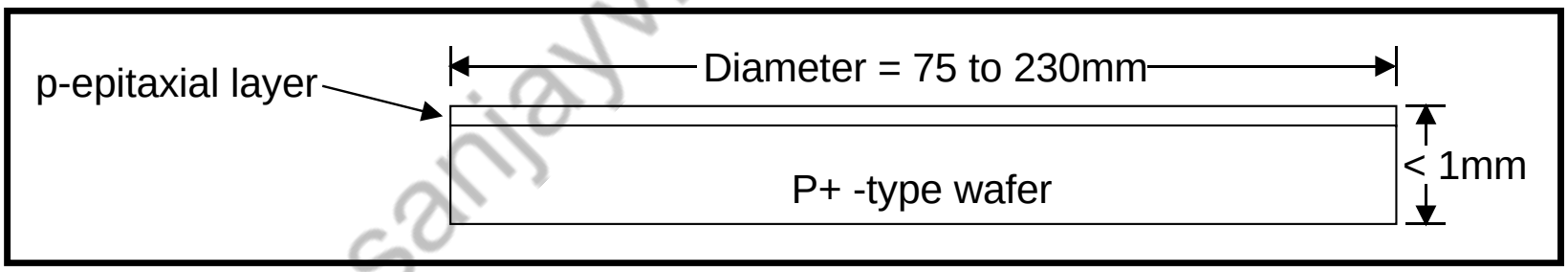
CMOS Fabrication Sequence

0. Start:

- For an n-well process the starting point is a p-type silicon wafer:
- wafer: typically 75 to 230mm in diameter and less than 1mm thick

1. Epitaxial growth:

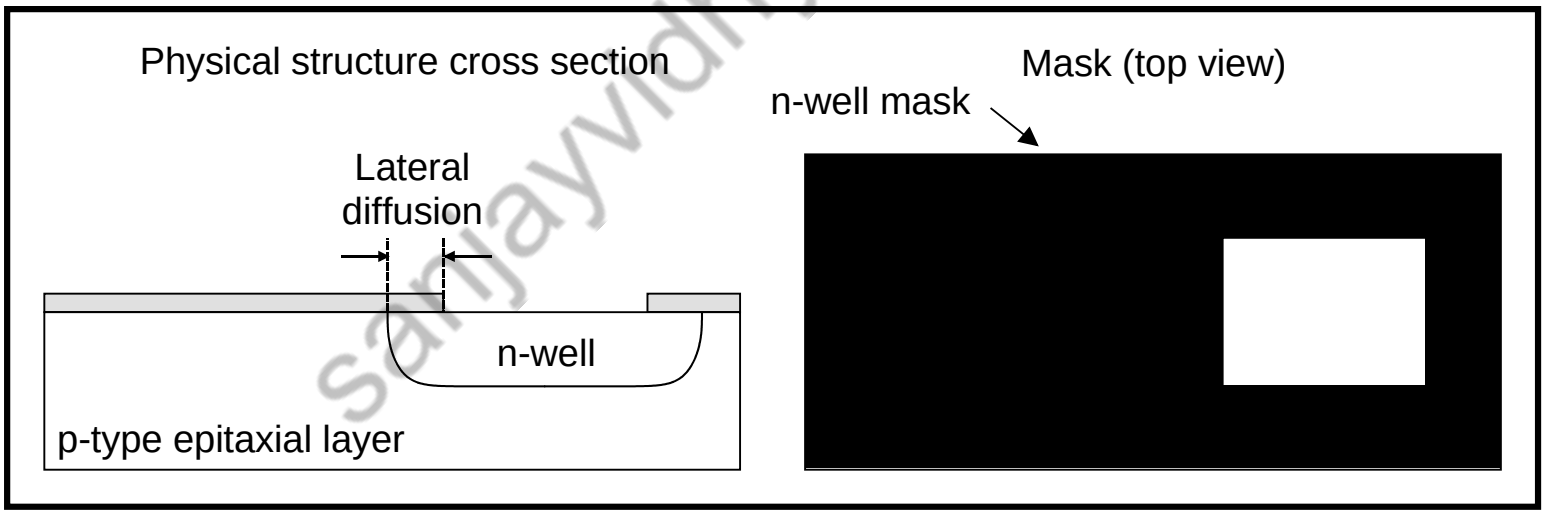
- A single p-type single crystal film is grown on the surface of the wafer by:
  - subjecting the wafer to high temperature and a source of dopant material
- The epi layer is used as the base layer to build the devices



CMOS Fabrication Sequence

2. N-well Formation:

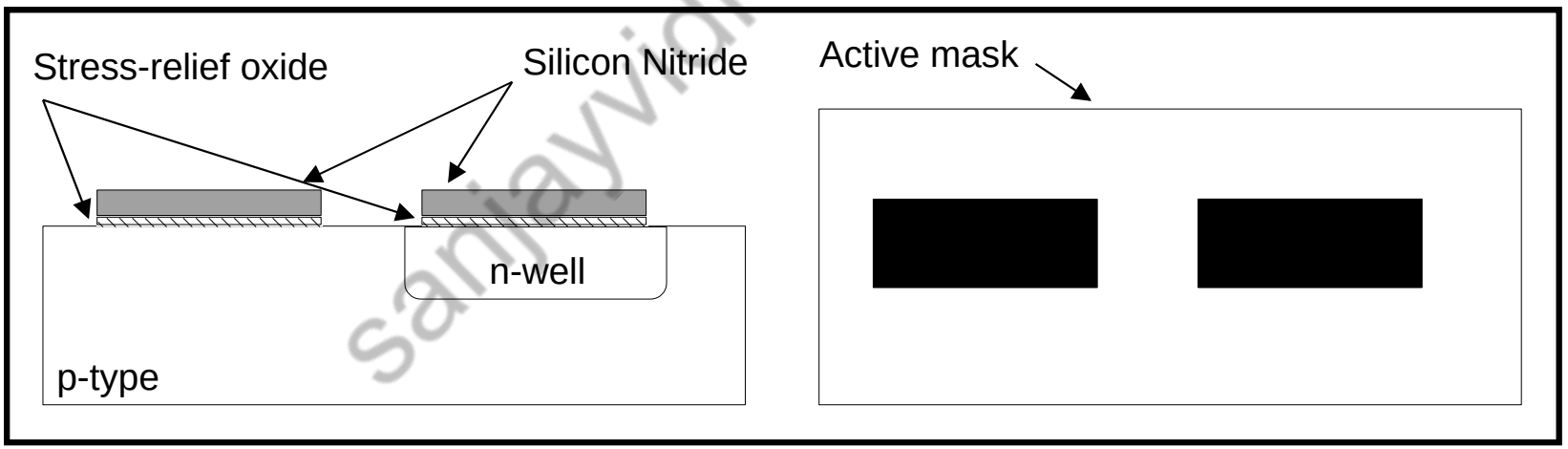
- PMOS transistors are fabricated in n-well regions
- The first mask defines the n-well regions
- N-well's are formed by ion implantation or deposition and diffusion
- Lateral diffusion limits the proximity between structures
- Ion implantation results in shallower wells compatible with today's fine-line processes



CMOS Fabrication Sequence

3. Active area definition:

- Active area:
  - planar section of the surface where transistors are build
  - defines the gate region (thin oxide)
  - defines the n+ or p+ regions
- A thin layer of SiO_2 is grown over the active region and covered with silicon nitride



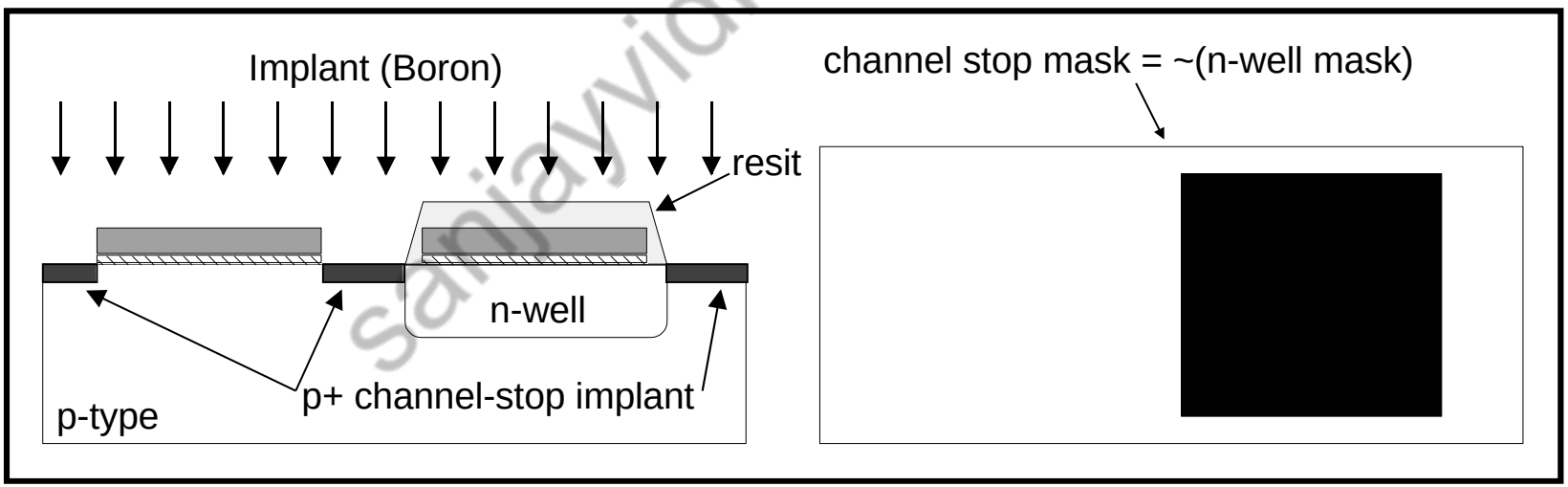
CMOS Fabrication Sequence

4. Isolation:

- Parasitic (unwanted) FET's exist between unrelated transistors (Field Oxide FET's)
- Source and drains are existing source and drains of wanted devices
- Gates are metal and polysilicon interconnects
- The threshold voltage of FOX FET's are higher than for normal FET's

4.1 Channel-stop implant

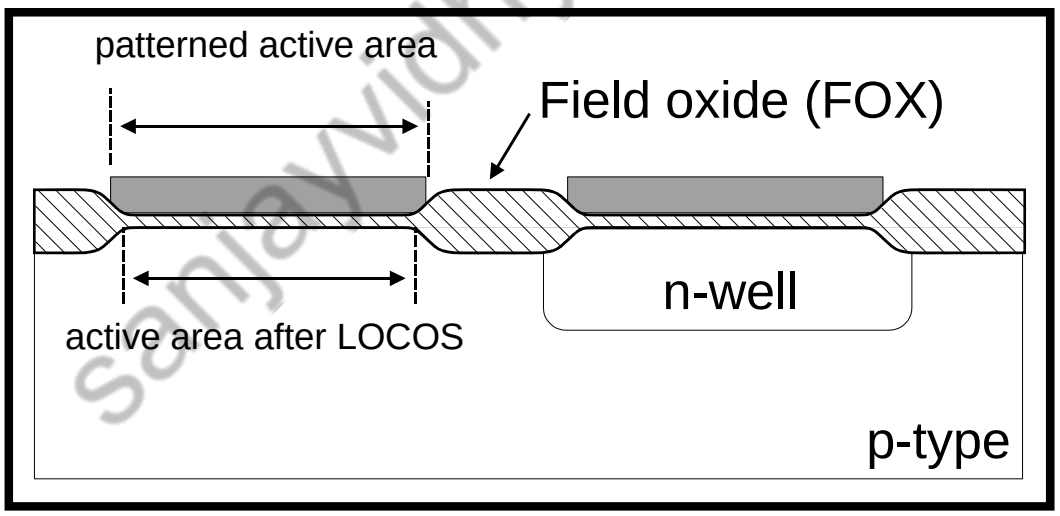
The silicon nitride (over n-active) and the photoresist (over n-well) act as masks for the channel-stop implant



CMOS Fabrication Sequence

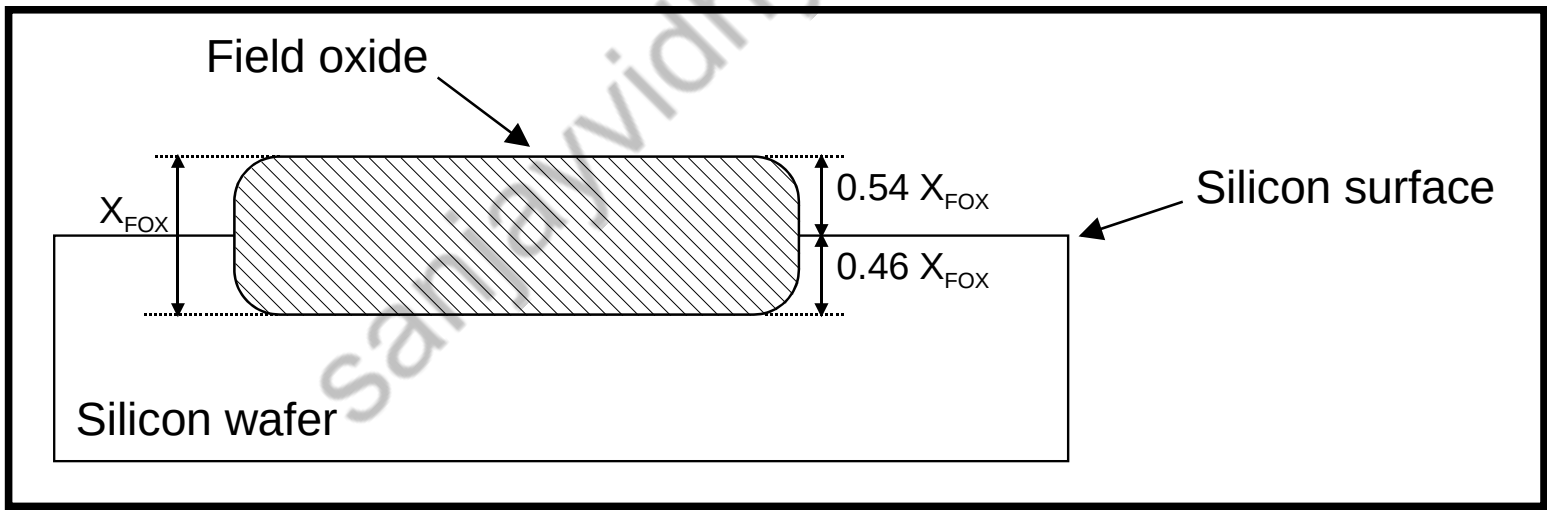
4.2 Local oxidation of silicon (LOCOS)

- The photoresist mask is removed
- The SiO_2/SiN layers will now act as a masks
- The thick field oxide is then grown by:
  - exposing the surface of the wafer to a flow of oxygen-rich gas
- The oxide grows in both the vertical and lateral directions
- This results in a active area smaller than patterned



CMOS Fabrication Sequence

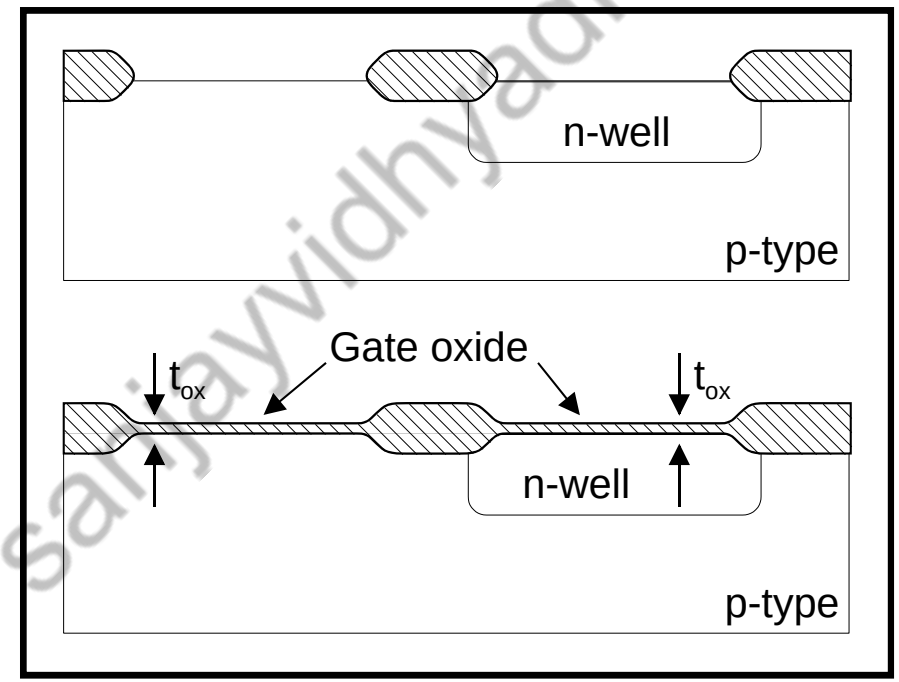
- Silicon oxidation is obtained by:
  - Heating the wafer in a oxidizing atmosphere:
    - Wet oxidation: water vapor, T = 900 to 1000ºC (rapid process)
    - Dry oxidation: Pure oxygen, T = 1200ºC (high temperature required to achieve an acceptable growth rate)
- Oxidation consumes silicon
  - SiO_2 has approximately twice the volume of silicon
  - The FOX is recedes below the silicon surface by $0.46X_{FOX}$



CMOS Fabrication Sequence

5. Gate oxide growth

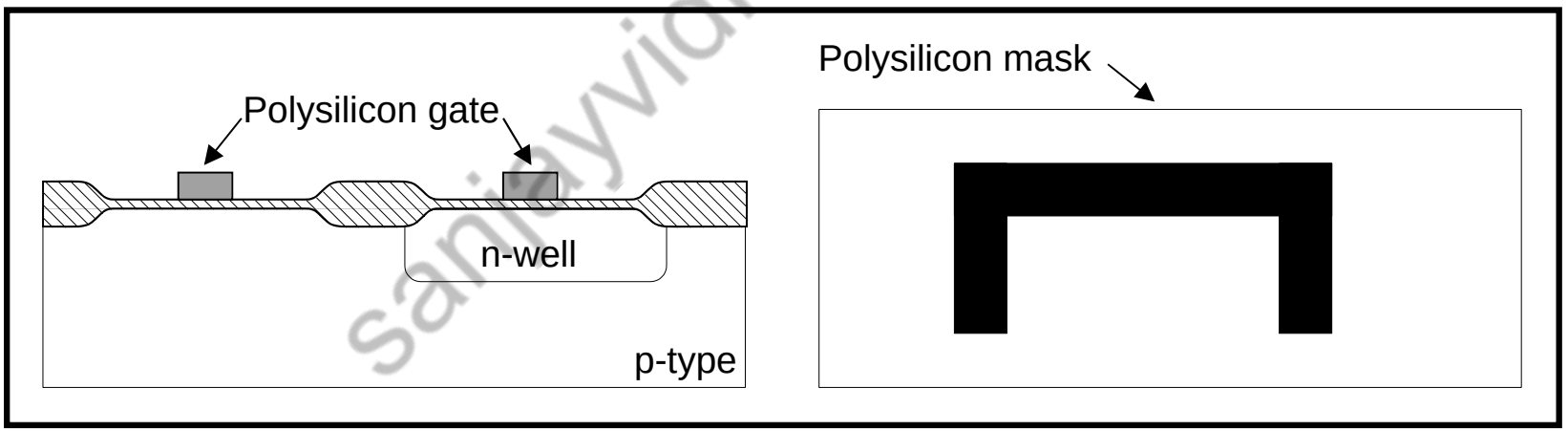
- The nitride and stress-relief oxide are removed
- The devices threshold voltage is adjusted by:
  - adding charge at the silicon/oxide interface
- The well controlled gate oxide is grown with thickness t_{ox}



CMOS Fabrication Sequence

6. Polysilicon deposition and patterning

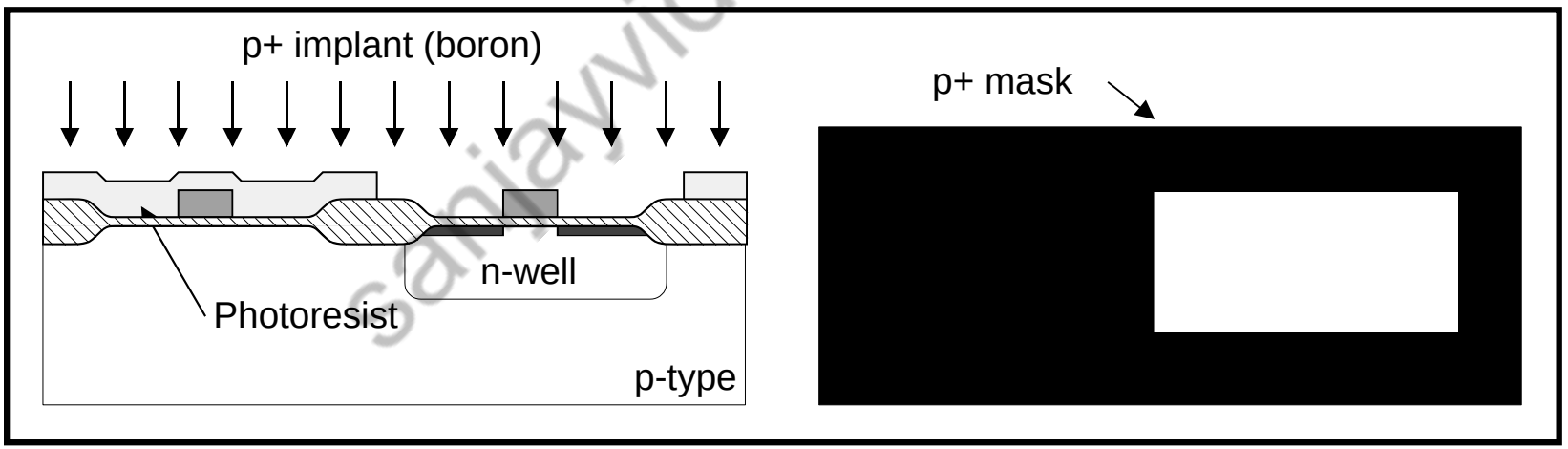
- A layer of polysilicon is deposited over the entire wafer surface
- The polysilicon is then patterned by a lithography sequence
- All the MOSFET gates are defined in a single step
- The polysilicon gate can be doped (n+) while is being deposited to lower its parasitic resistance (important in high speed fine line processes)



CMOS Fabrication Sequence

7. PMOS formation

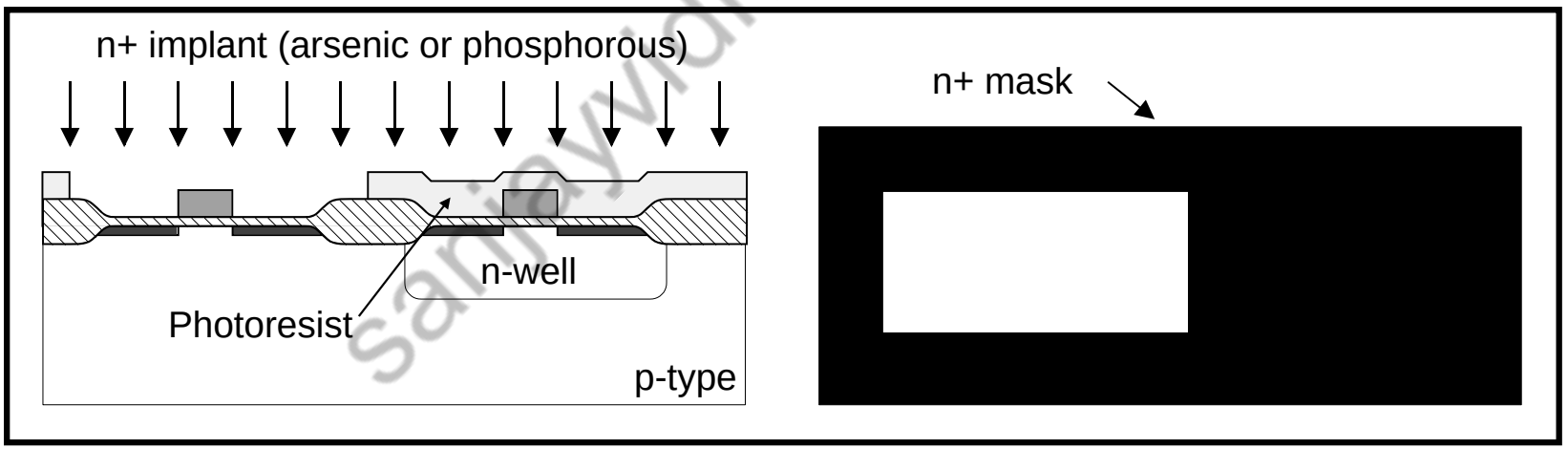
- Photoresist is patterned to cover all but the p+ regions
- A boron ion beam creates the p+ source and drain regions
- The polysilicon serves as a mask to the underlying channel
  - This is called a **self-aligned process**
  - It allows precise placement of the source and drain regions
- During this process the gate gets doped with p-type impurities
  - Since the gate had been doped n-type during deposition, the final type (n or p) will depend on which dopant is dominant



CMOS Fabrication Sequence

8. NMOS formation

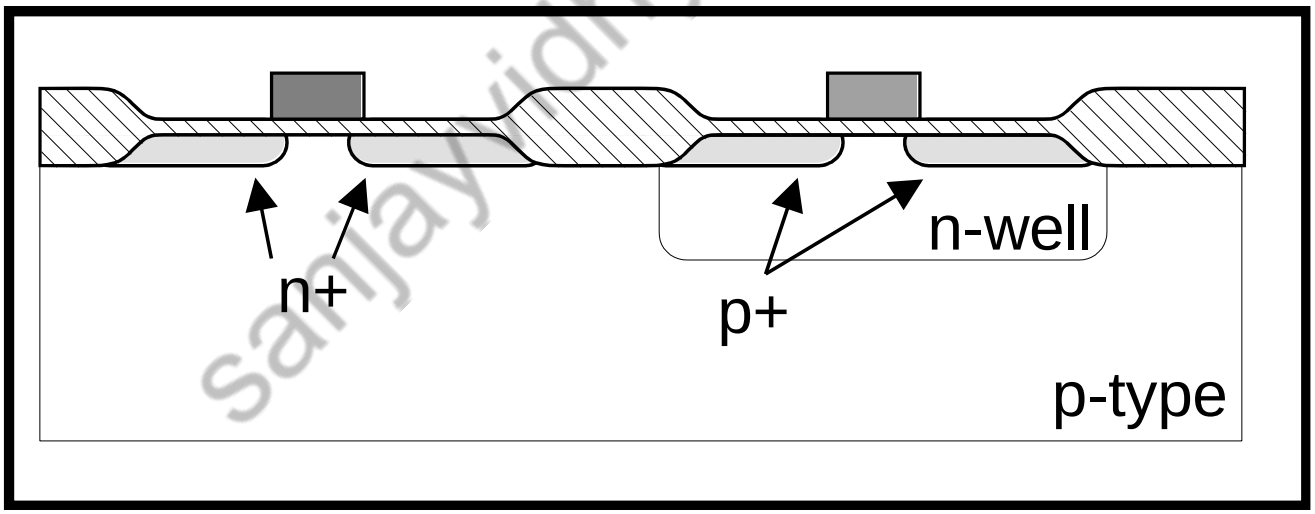
- Photoresist is patterned to define the n+ regions
- Donors (arsenic or phosphorous) are ion-implanted to dope the n+ source and drain regions
- The process is self-aligned
- The gate is n-type doped



CMOS Fabrication Sequence

9. Annealing

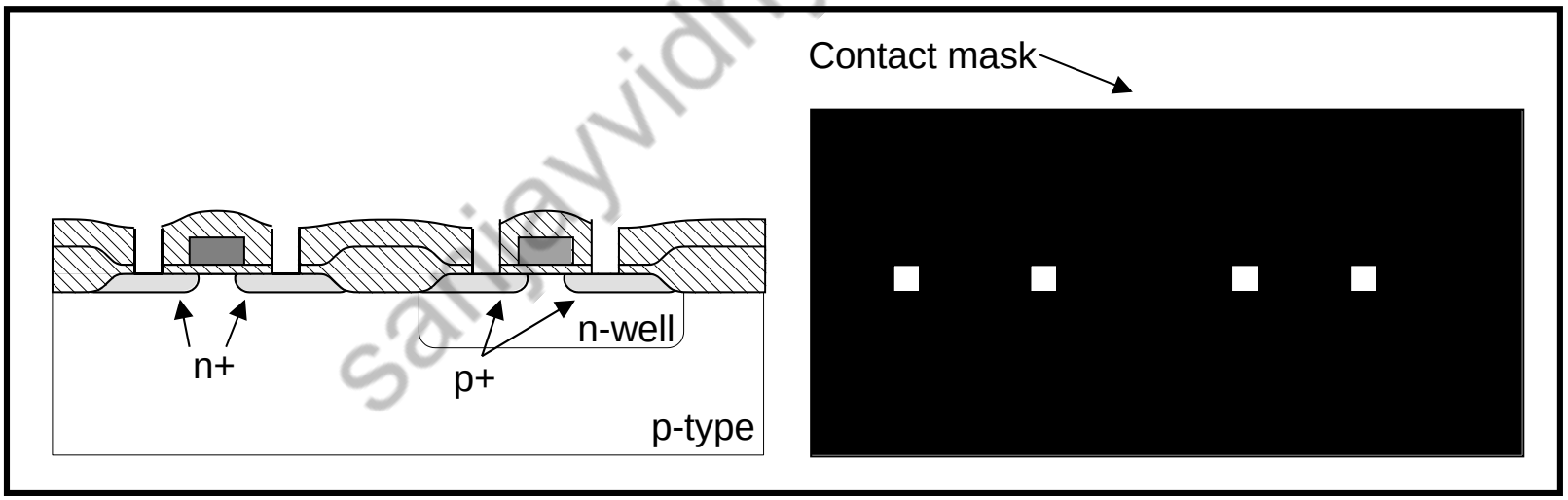
- After the implants are completed a thermal annealing cycle is executed
- This allows the impurities to diffuse further into the bulk
- After thermal annealing, it is important to keep the remaining process steps at as low temperature as possible



CMOS Fabrication Sequence

10. Contact cuts

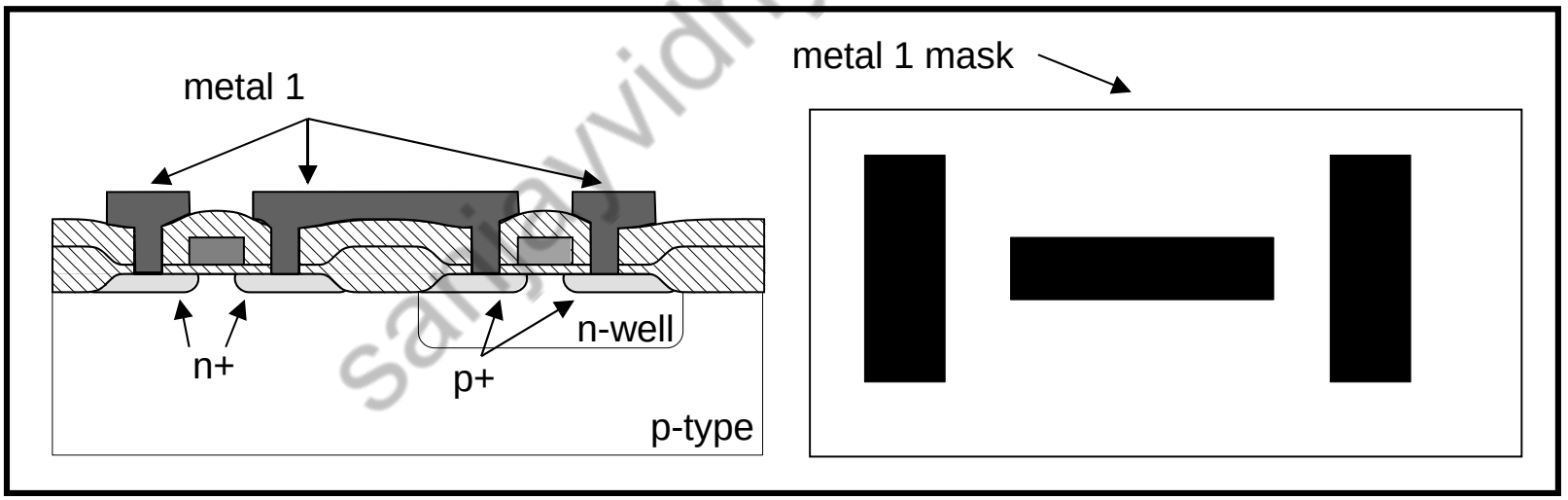
- The surface of the IC is covered by a layer of CVD oxide
  - The oxide is deposited at low temperature (LTO) to avoid that underlying doped regions will undergo diffusive spreading
- Contact cuts are defined by etching SiO_2 down to the surface to be contacted
- These allow metal to contact diffusion and/or polysilicon regions



CMOS Fabrication Sequence

11. Metal 1

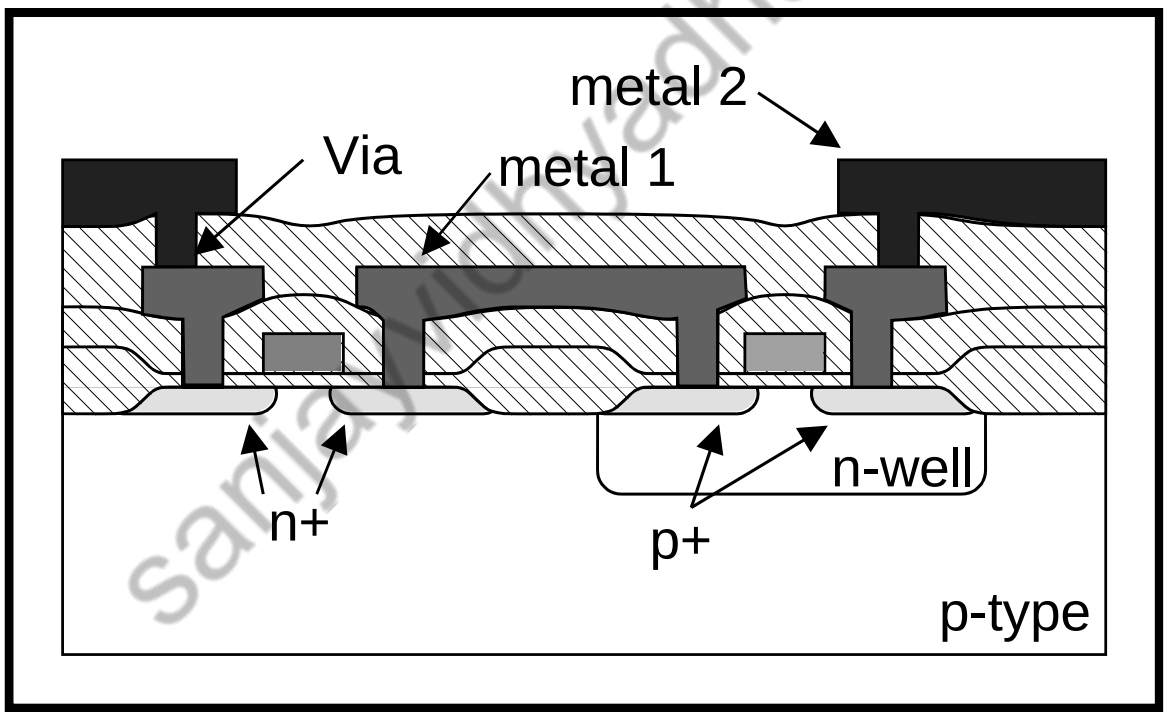
- A first level of metallization is applied to the wafer surface and selectively etched to produce the interconnects



CMOS Fabrication Sequence

12. Metal 2

- Another layer of LTO CVD oxide is added
- Via openings are created
- Metal 2 is deposited and patterned



CMOS Fabrication Sequence

13. Over glass and pad openings

- A protective layer is added over the surface:
- The protective layer consists of:
  - A layer of SiO_2
  - Followed by a layer of silicon nitride
- The SiN layer acts as a diffusion barrier against contaminants (passivation)
- Finally, contact cuts are etched, over metal 2, on the passivation to allow for wire bonding.

Detailed Mask Views

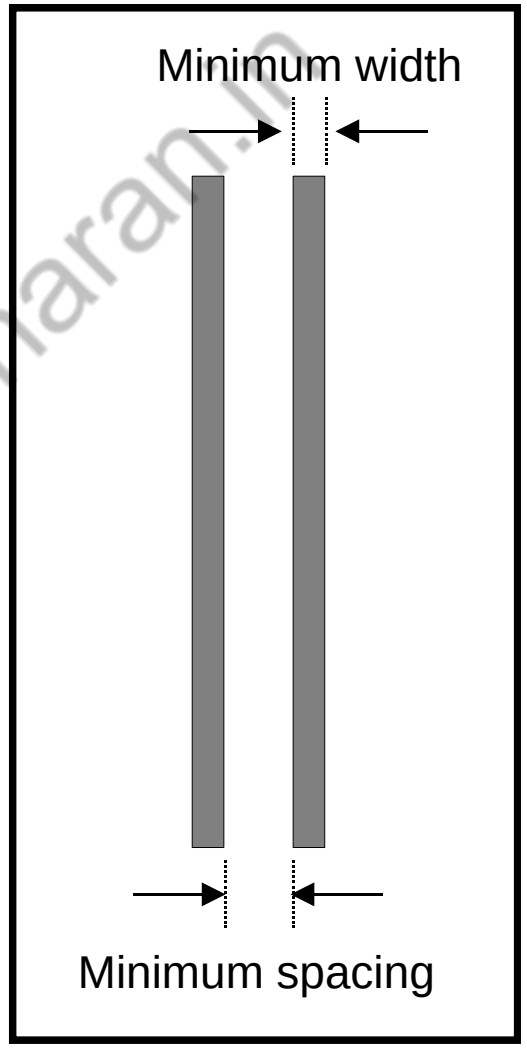
- Six masks
  - n-well
  - Polysilicon
  - n+ diffusion
  - p+ diffusion
  - Contact
  - Metal

Design rules

- The limitations of the patterning process give rise to a set of mask design guidelines called design rules
- Design rules are a set of guidelines that specify the minimum dimensions and spacings allowed in a layout drawing
- Violating a design rule might result in a non-functional circuit or in a highly reduced yield
- The design rules can be expressed as:
  - A list of minimum feature sizes and spacings for all the masks required in a given process
  - Based on single parameter λ that characterize the linear feature (e.g. the minimum grid dimension). λ base rules allow simple scaling. **Generally λ = L/2.**

Design rules

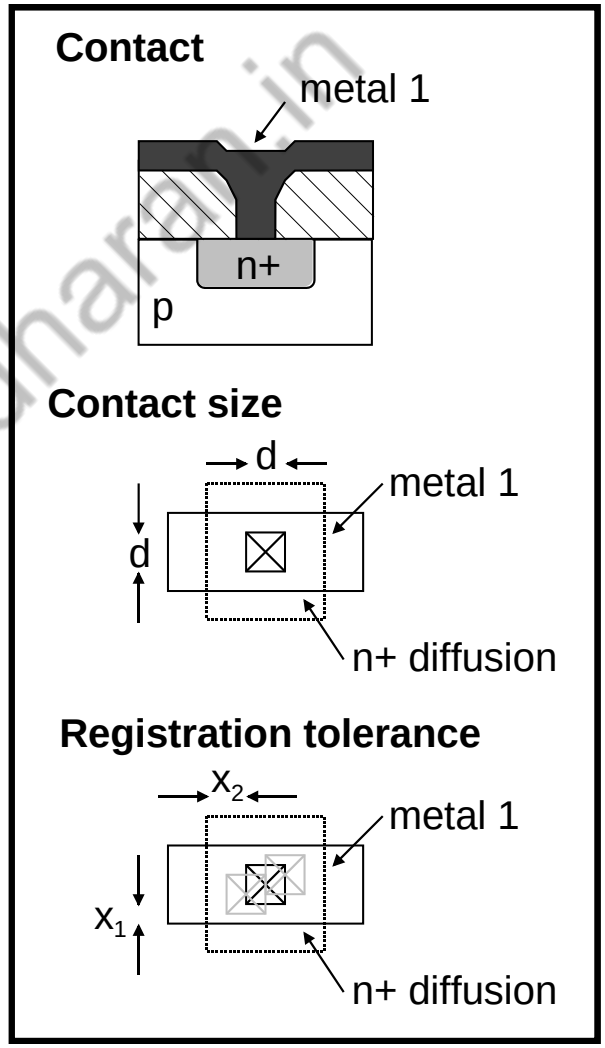
- Minimum line-width:
  - smallest dimension permitted for any object in the layout drawing (minimum feature size)
- Minimum spacing:
  - smallest distance permitted between the edges of two objects
- This rules originate from the resolution of the optical printing system, the etching process, or the surface roughness



Minimum line width of a process is 2λ

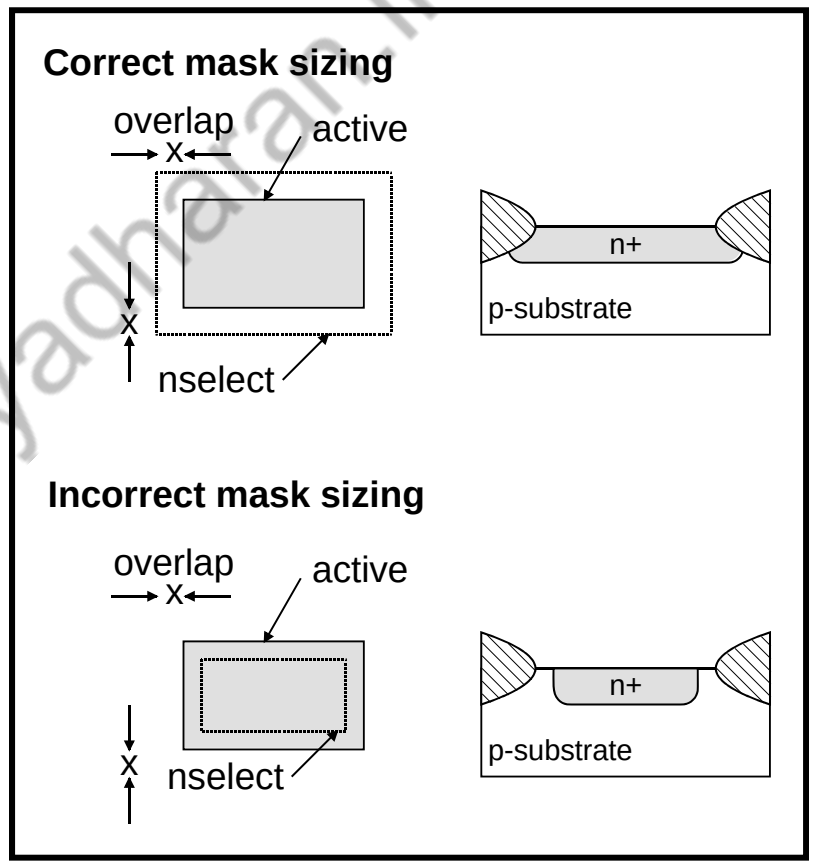
Design rules

- Contacts and vias:
  - minimum size limited by the lithography process
  - large contacts can result in cracks and voids
  - Dimensions of contact cuts are restricted to values that can be reliably manufactured
  - A minimum distance between the edge of the oxide cut and the edge of the patterned region must be specified to allow for misalignment tolerances (registration errors)



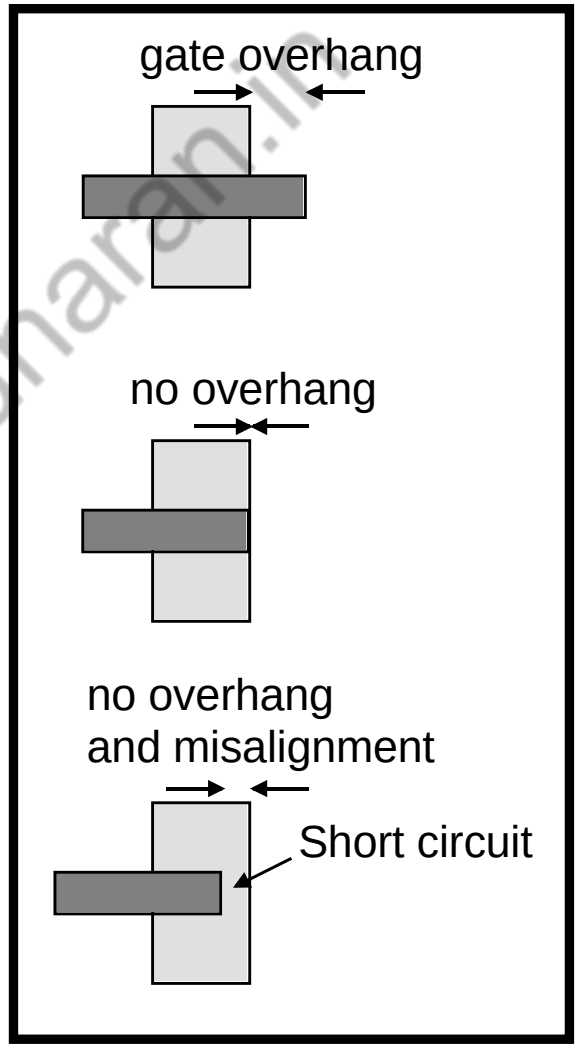
Design rules

- MOSFET rules
  - n+ and p+ regions are formed in two steps:
    - the active area openings allow the implants to penetrate into the silicon substrate
    - the nselect or pselect provide photoresist openings over the active areas to be implanted
  - Since the formation of the diffusions depend on the overlap of two masks, the nselect and pselect regions must be larger than the corresponding active areas to allow for misalignments



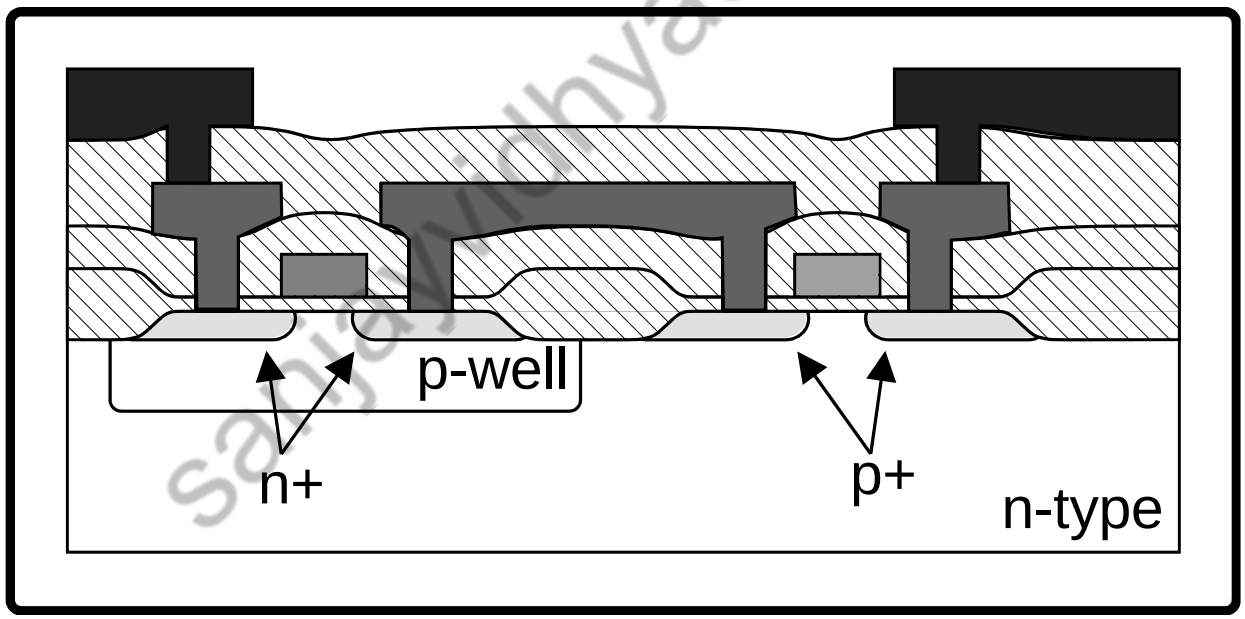
Design rules

- Gate overhang:
  - The gate must overlap the active area by a minimum amount
  - This is done to ensure that a misaligned gate will still yield a structure with separated drain and source regions
- A modern process has may hundreds of rules to be verified
  - Programs called Design Rule Checkers assist the designer in that task



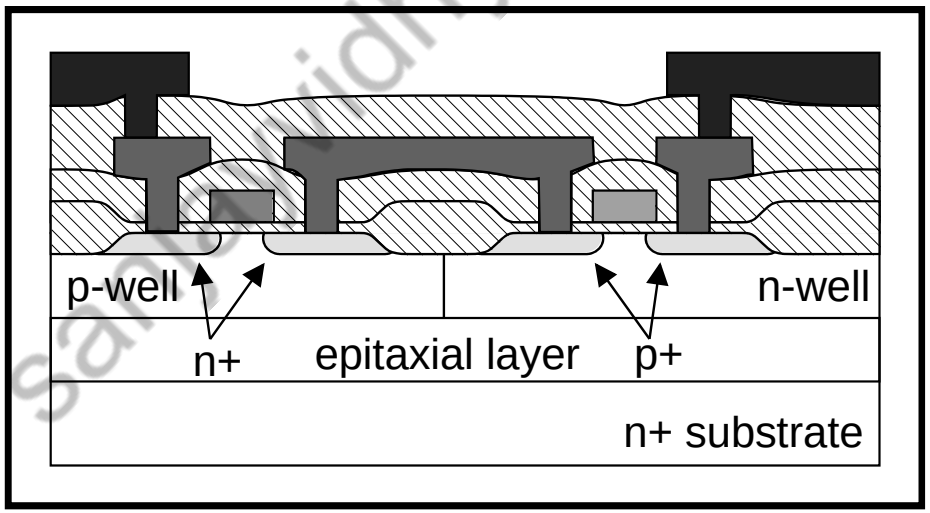
Other Processes

- **P-well process**
  - NMOS devices are build on a implanted p-well
  - PMOS devices are build on the substrate
  - P-well process moderates the difference between the p- and the n-transistors since the P devices reside in the native substrate
  - Advantages: better balance between p- and n-transistors



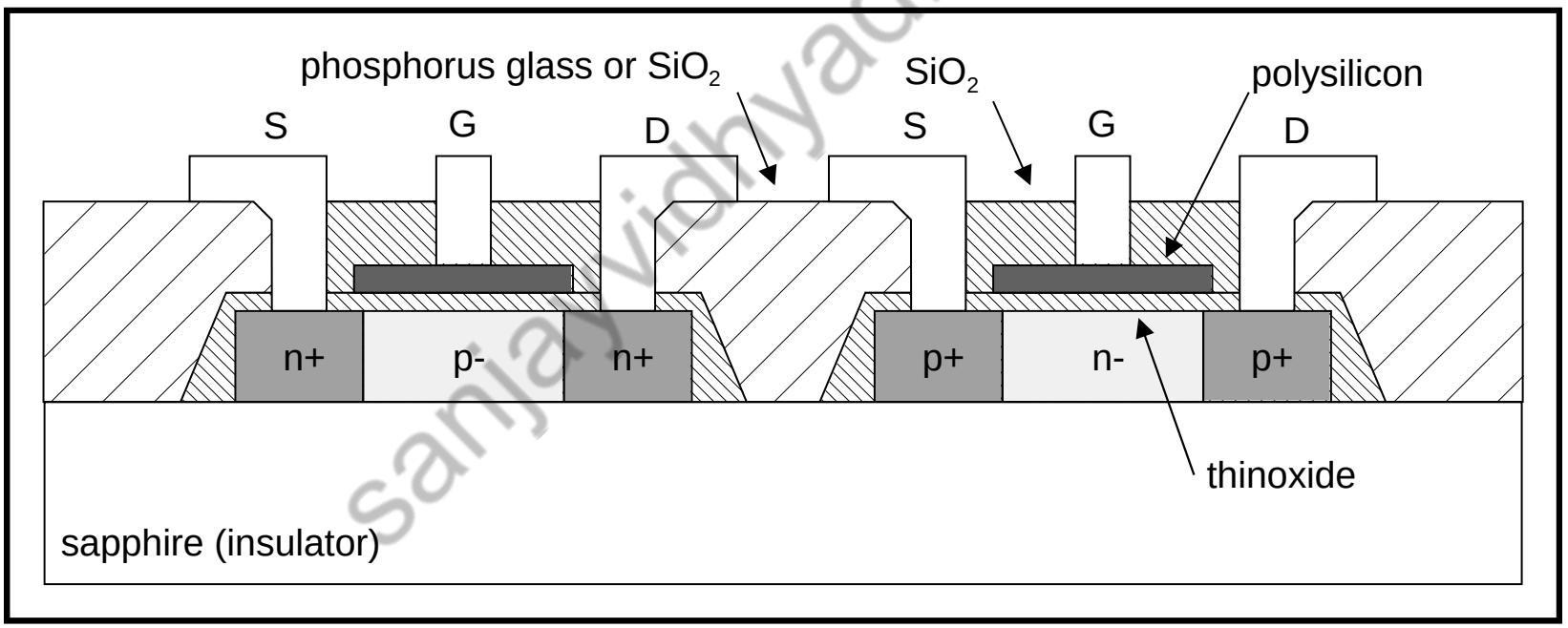
Other Processes

- **Twin-well process**
  - n+ or p+ substrate plus a lightly doped epi-layer (latchup prevention)
  - wells for the n- and p-transistors
  - Advantages, simultaneous optimization of p- and n-transistors:
    - threshold voltages
    - body effect
    - gain



Other Processes

- **Silicon On Insulator (SOI)**
  - Islands of silicon on an insulator form the transistors



Other Processes

Silicon On Insulator (SOI)

- Advantages:
  - No wells ⇒ denser transistor structures
  - Lower substrate capacitances
  - Very low leakage currents
  - No FOX FET exists between unrelated devices
  - No latchup
  - No body-effect:
    - However, the absence of a backside substrate can give origin to the “kink effect”
  - Radiation tolerance
- Disadvantages:
  - Absence of substrate diodes (hard to implement protection circuits)
  - Higher number of substrate defects ⇒ lower gain devices
  - More expensive processing

Process Enhancements

- Up to six metal levels in modern processes
- Copper for metal levels 2 and higher
- Stacked contacts and vias
- Chemical Metal Polishing for technologies with several metal levels
- For analogue applications some processes offer:
  - capacitors
  - resistors
  - bipolar transistors (BiCMOS)

Thank you