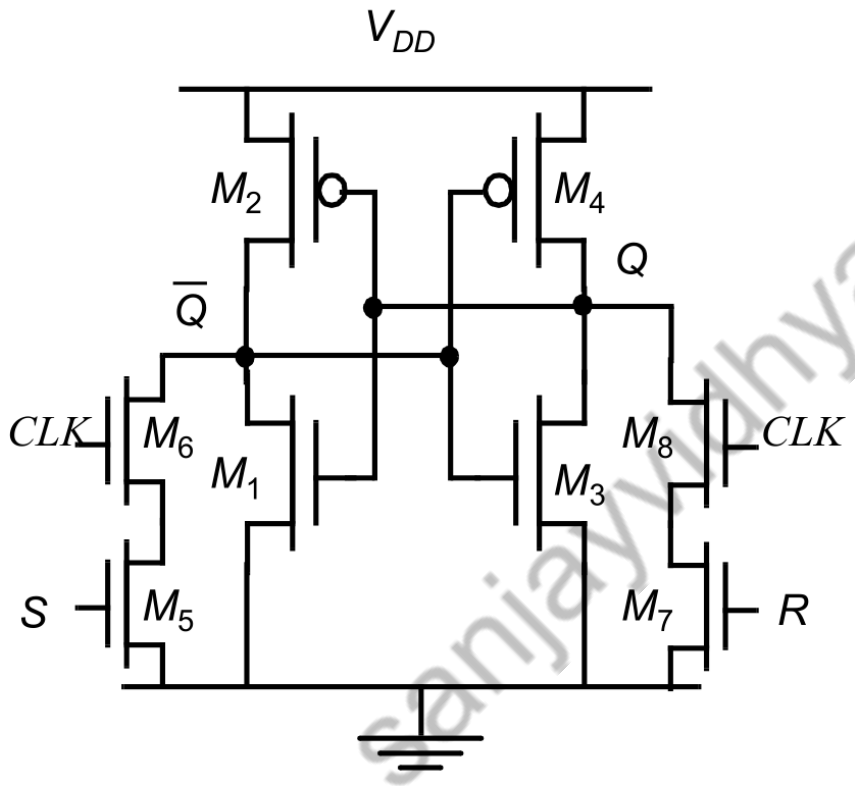
Advanced VLSI Design: 2021-22
Lecture 3
Dynamic Registers

By Dr. Sanjay Vidhyadharan

Static CMOS Latch



- Area Large
- Complexity
- Static Dissipation
- Dynamic Dissipation
  - Short Circuit
  - Switching Loss

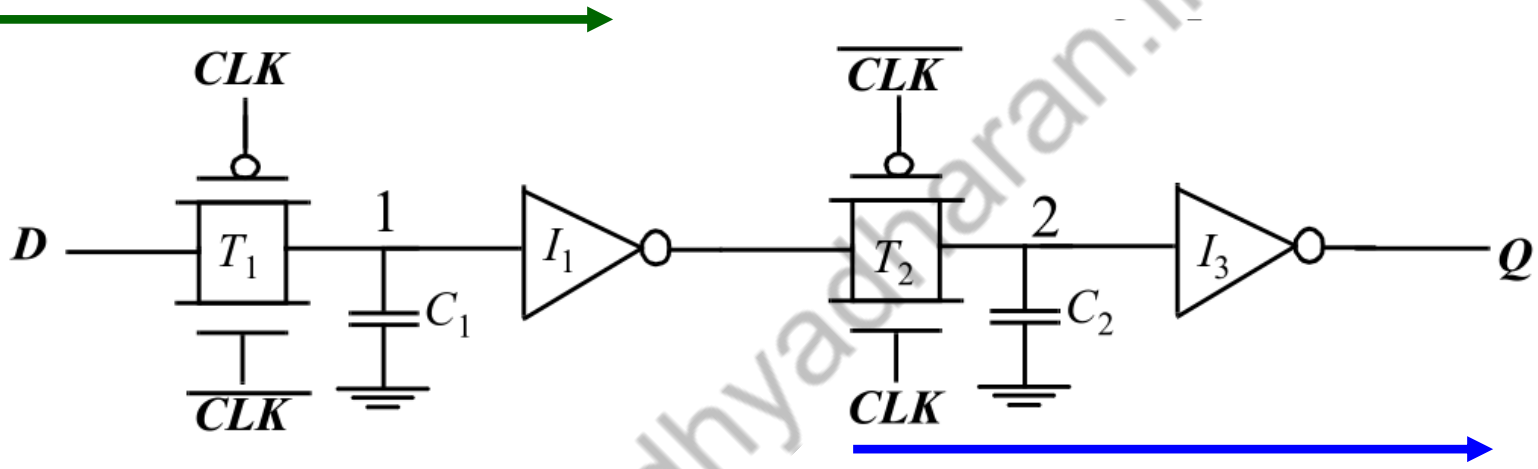
Dynamic Register

Principle of Operation:

- Temporary storage of charge on parasitic capacitors.
- A stored value can hence only be kept for a limited amount of time, typically in the range of milliseconds.
- To preserve signal integrity, a periodic refresh of its value
- Registers are used in computational structures are constantly clocked such as pipelined datapath.

Dynamic Register

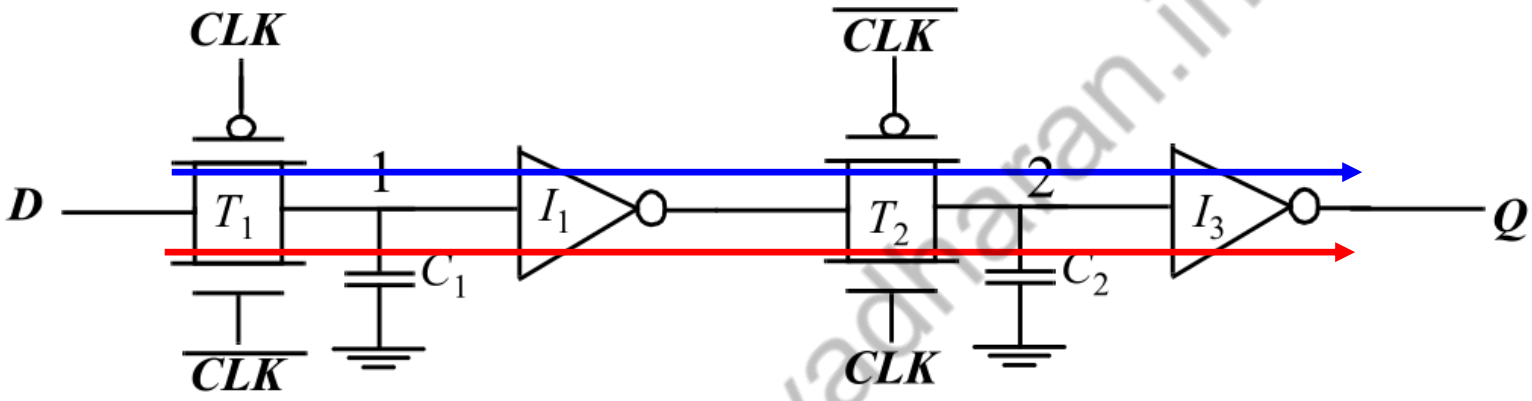
Dynamic Positive edge-triggered register



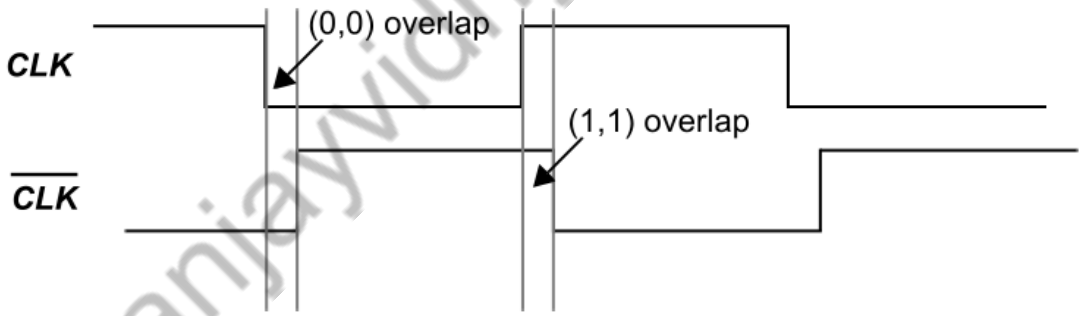
- Only 8 transistors
- Only 6 transistors if NMOS Gates used
- Low Power
- Low Propagation Delay (One Pass Transistor Delay + One Inverter Delay)
- Set-up Time : (One Pass Transistor Delay + One Inverter Delay)
- Hold Time : Nil

Dynamic Register

Dynamic Positive edge-triggered register



Limitations

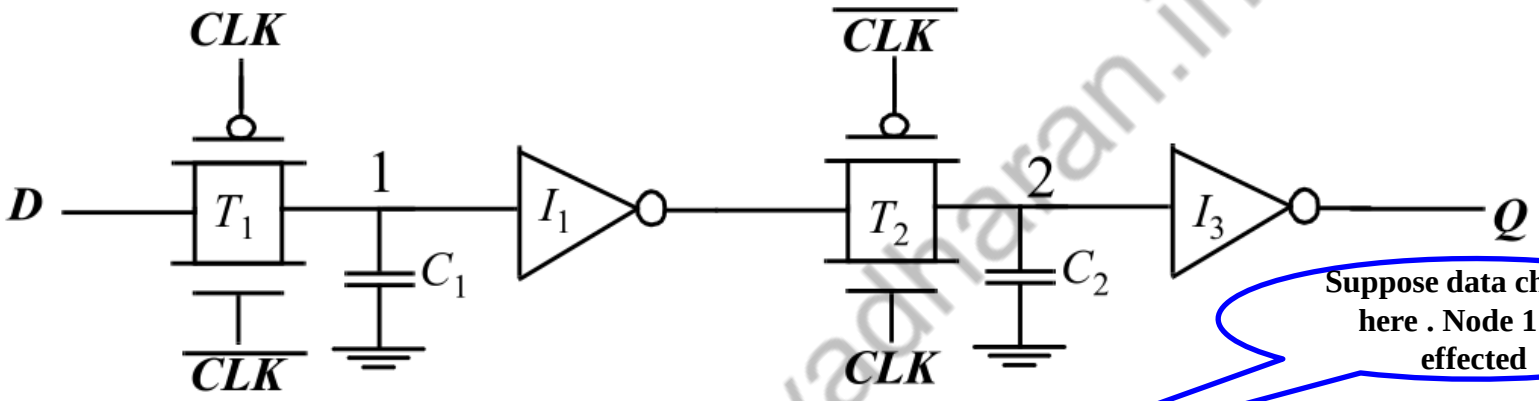


During the 0-0 overlap direct path for data from D to Q ($T1_{PMOS} - T2_{PMOS}$)

During the 1-1 overlap direct path for data from D to Q ($T1_{NMOS} - T2_{NMOS}$)

Dynamic Register

Dynamic Positive edge-triggered register



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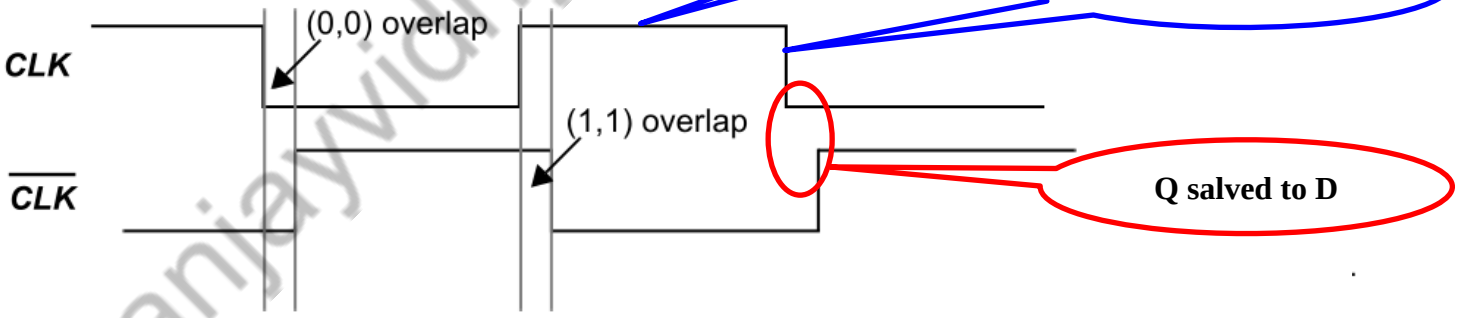
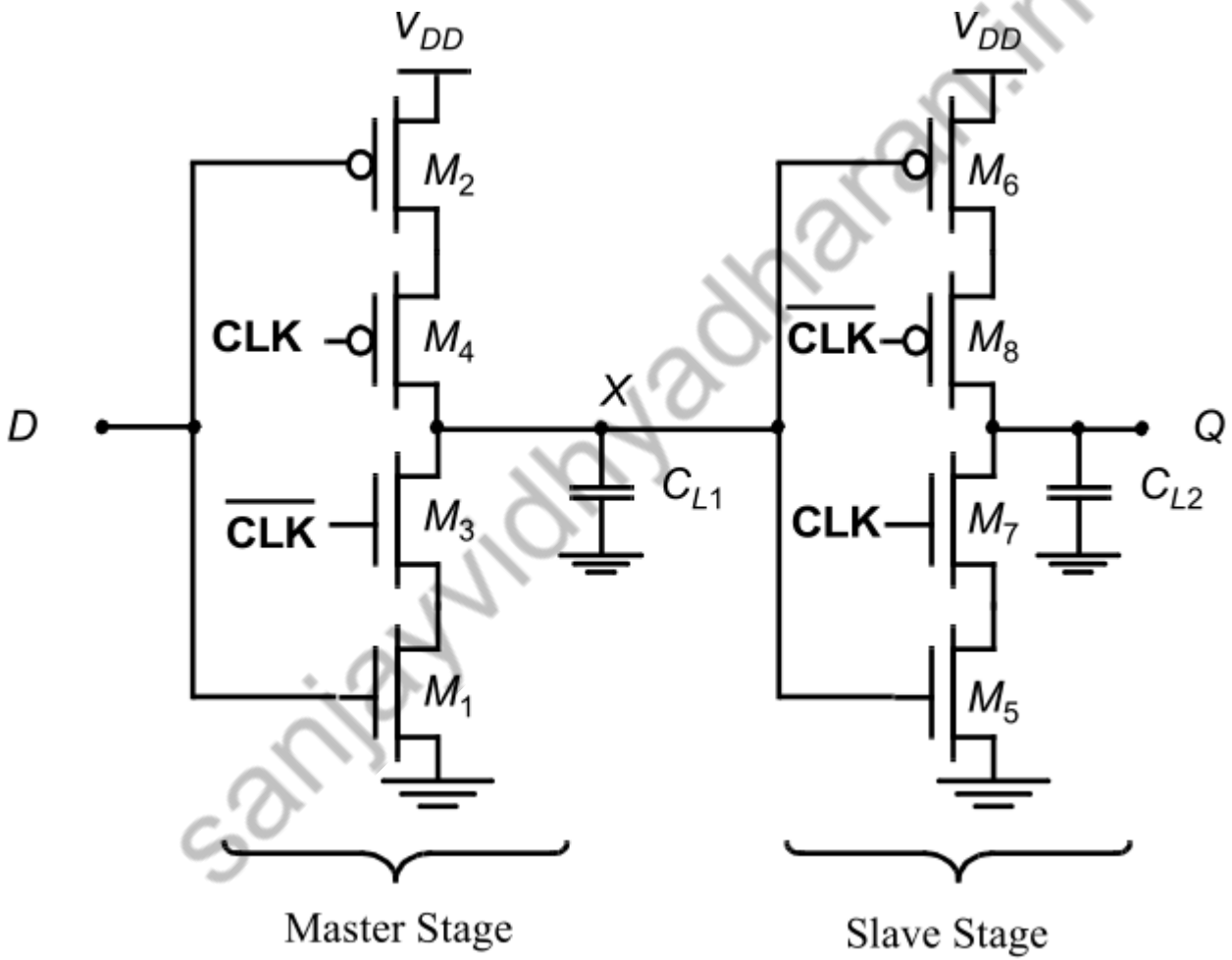


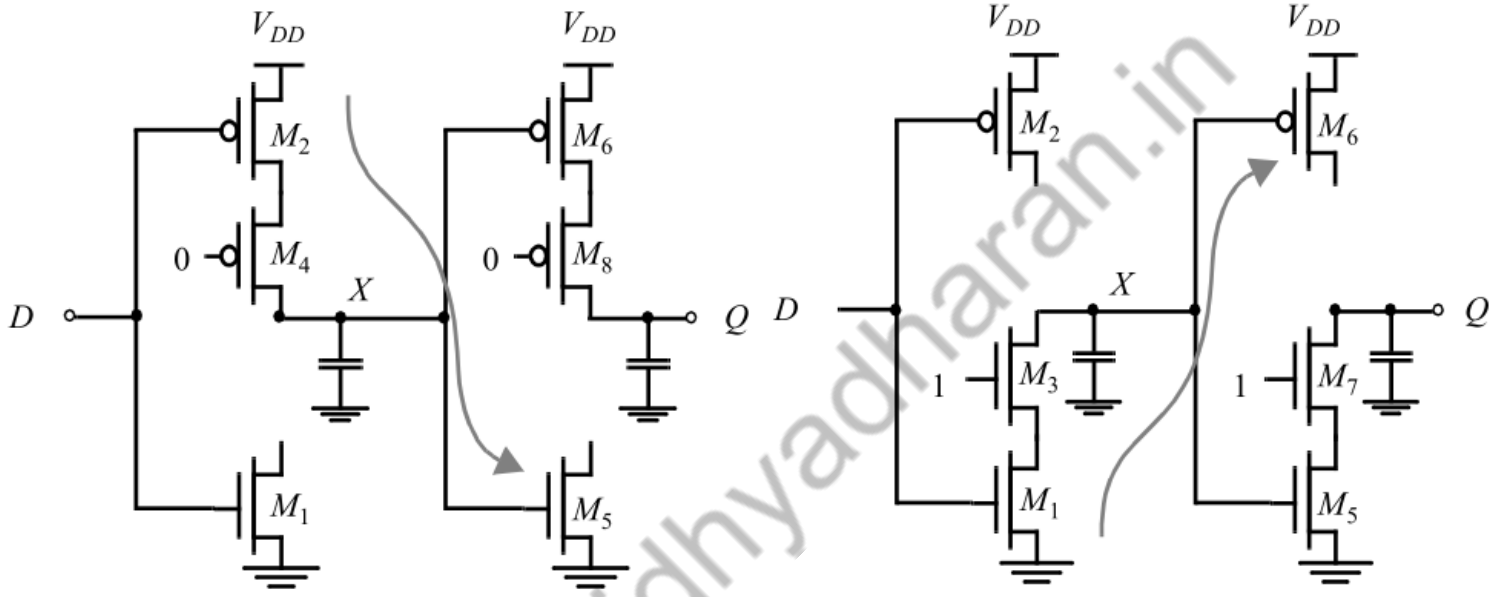
Q can change on the falling edge

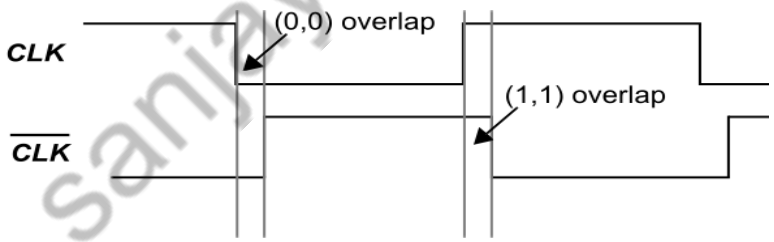
$$t_{overlap0-0} < t_{T1} + t_{I1} + t_{T2}$$

Clock-Skew Insensitive C^{2}MOS Register



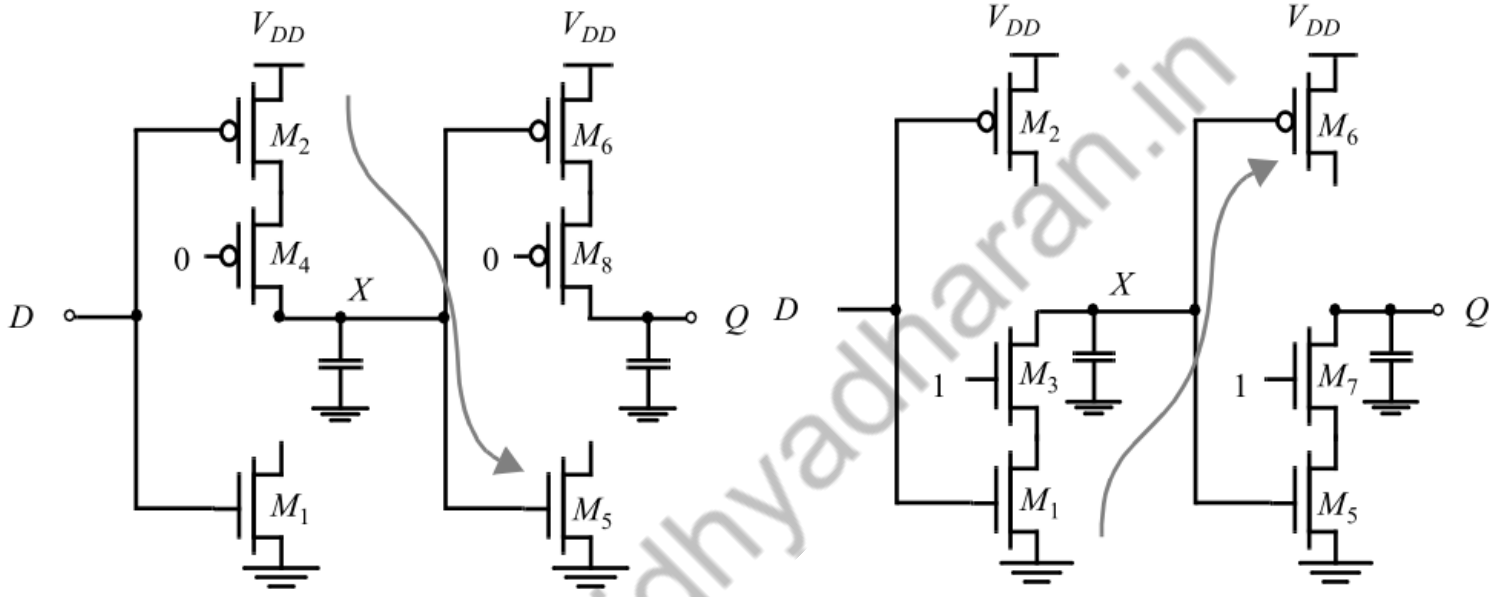
Clock-Skew Insensitive C^{2}MOS Register

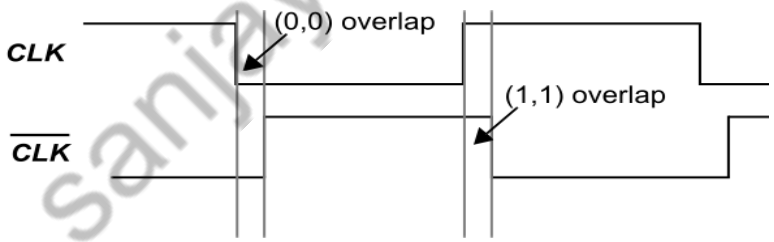




If the D input changes during the overlap period, node X can make a transition, but cannot propagate to the output.

Clock-Skew Insensitive C^{2}MOS Register





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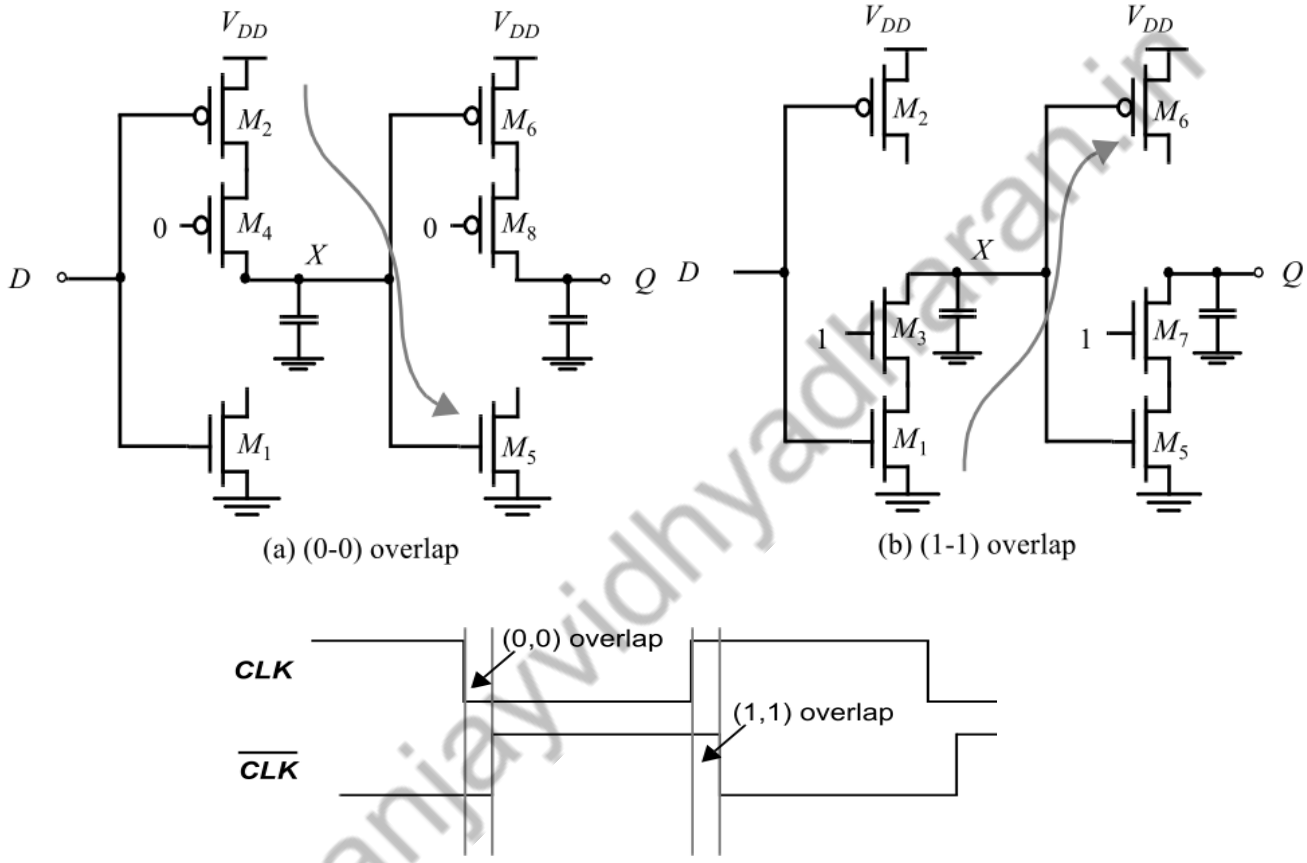
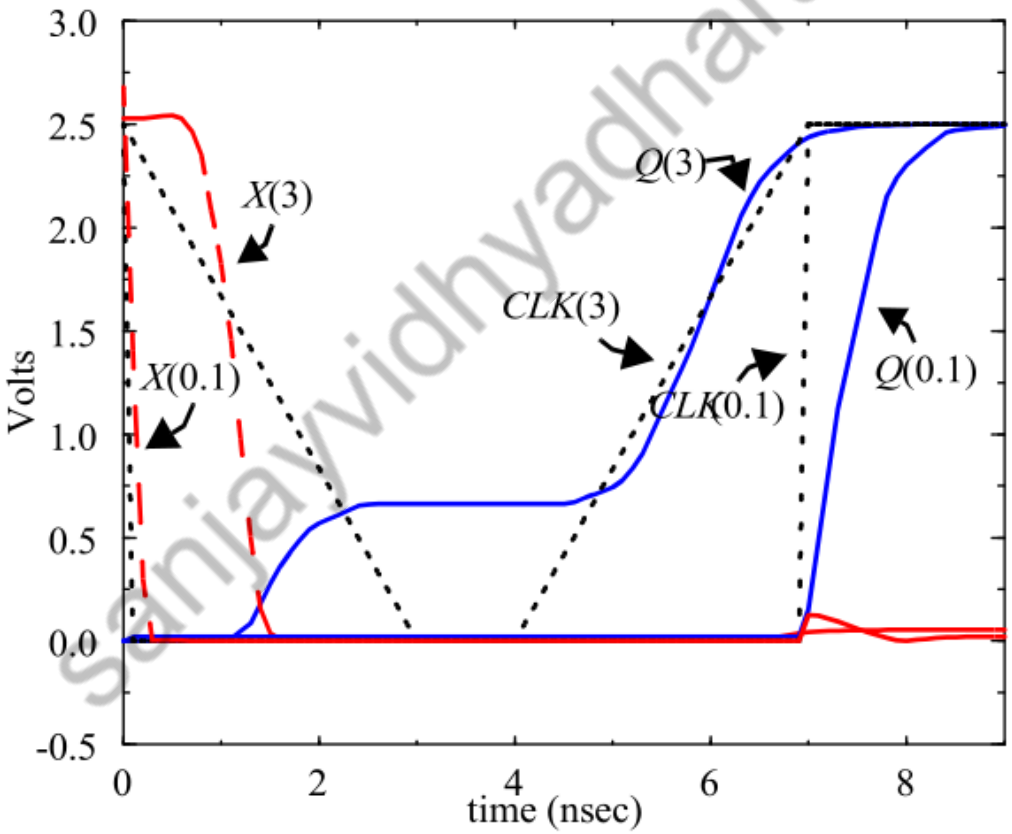
Clock-Skew Insensitive C^{2}MOS Register



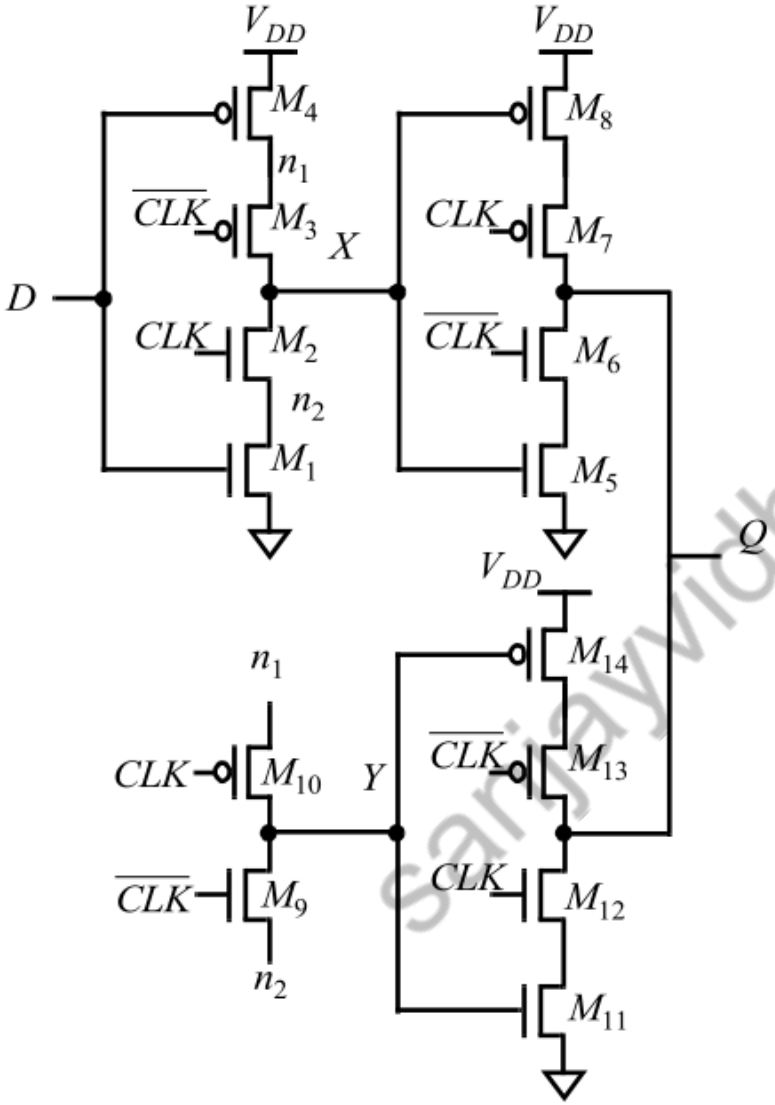
If the D input changes during the overlap period, node X can make a transition, but cannot propagate to the output. However, as soon as the overlap period is over, the PMOS M_8 is turned on and the 0 propagates to output. This effect is not desirable. The problem is fixed by imposing a hold time constraint on the input data, D, or, in other words, the data D should be stable during the overlap period.

Clock-Skew Insensitive C^{2}MOS Register

Clock rise time (or fall time) should be smaller than approximately five times the propagation delay of the register.

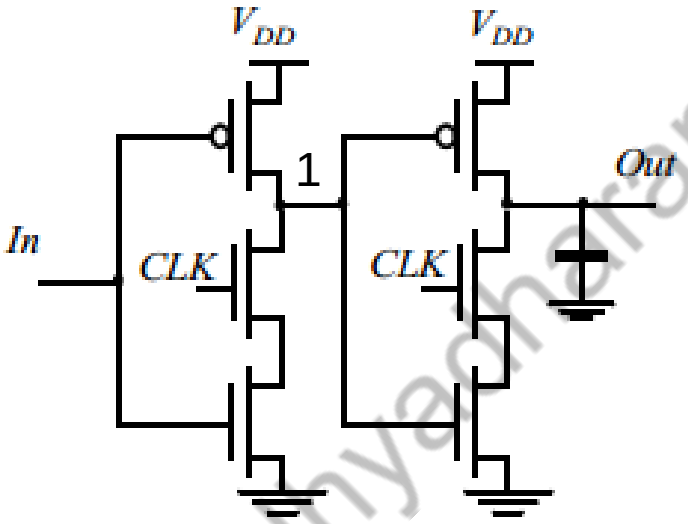


Dual-edge Registers



- Input sampled on both edges
- Lower frequency for same functional throughput
- Power savings in the clock distribution network

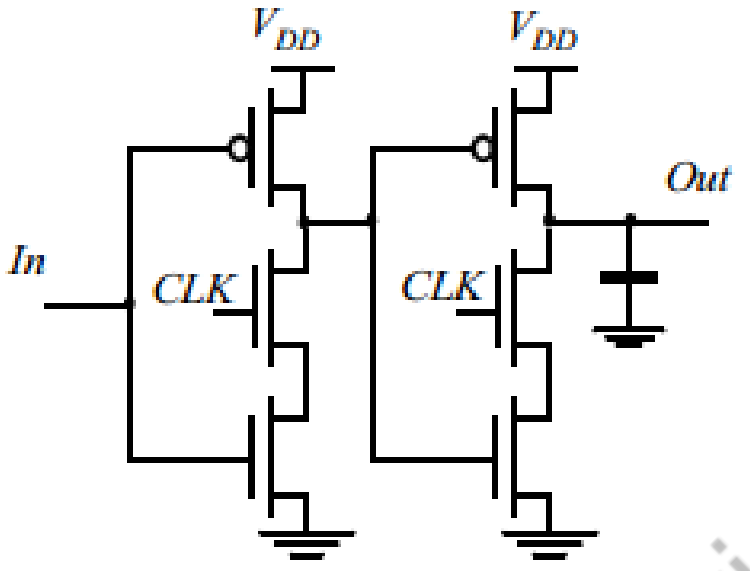
True Single-Phase Clocked Register (TSPCR)



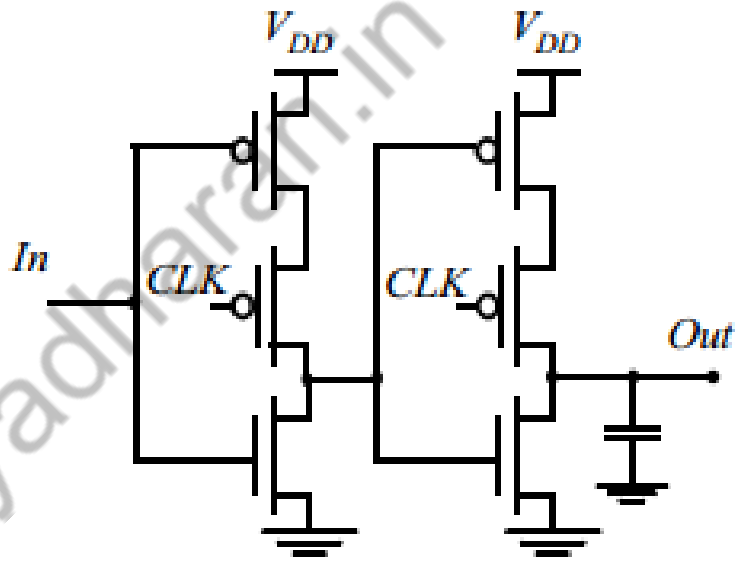
Positive Latch

- When Clock is Low :
  - If data is 0 , *Node 1* is Charged to 'High'. *Node Out* retains previous value.
  - If data is 1 , *Node 1* is retains previous value. *Node Out* retains previous value.
- When Clock is High :
  - Chain of two inverters Latch is transparent and Q slaved to D

True Single-Phase Clocked Register (TSPCR)



Positive Latch

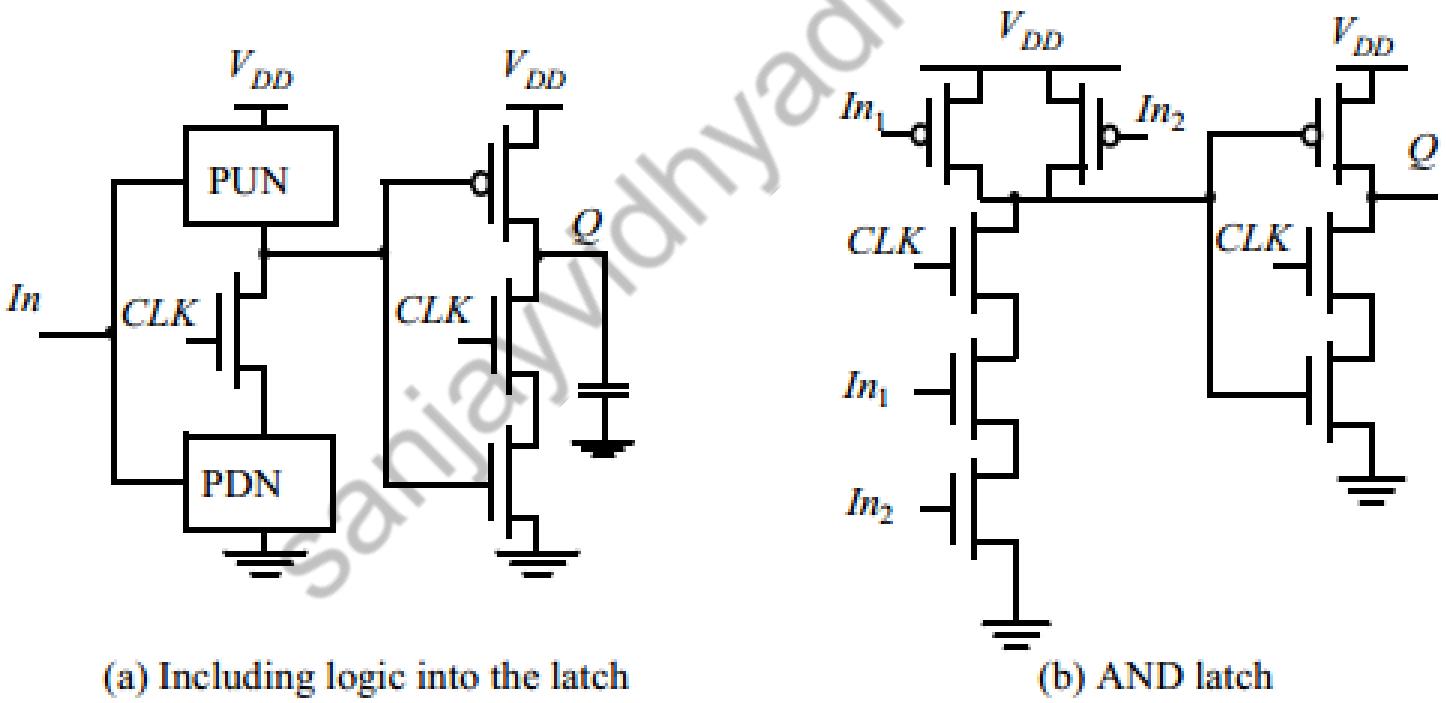


Negative Latch

- In two-phase clocking schemes, care must be taken in routing the two clock signals to ensure that overlap is minimized.
- A register can be constructed by cascading positive and negative latches.
- The main advantage is the use of a single clock phase.
- The disadvantage is the slight increase in the number of transistors -12 transistors are required.

True Single-Phase Clocked Register (TSPCR)

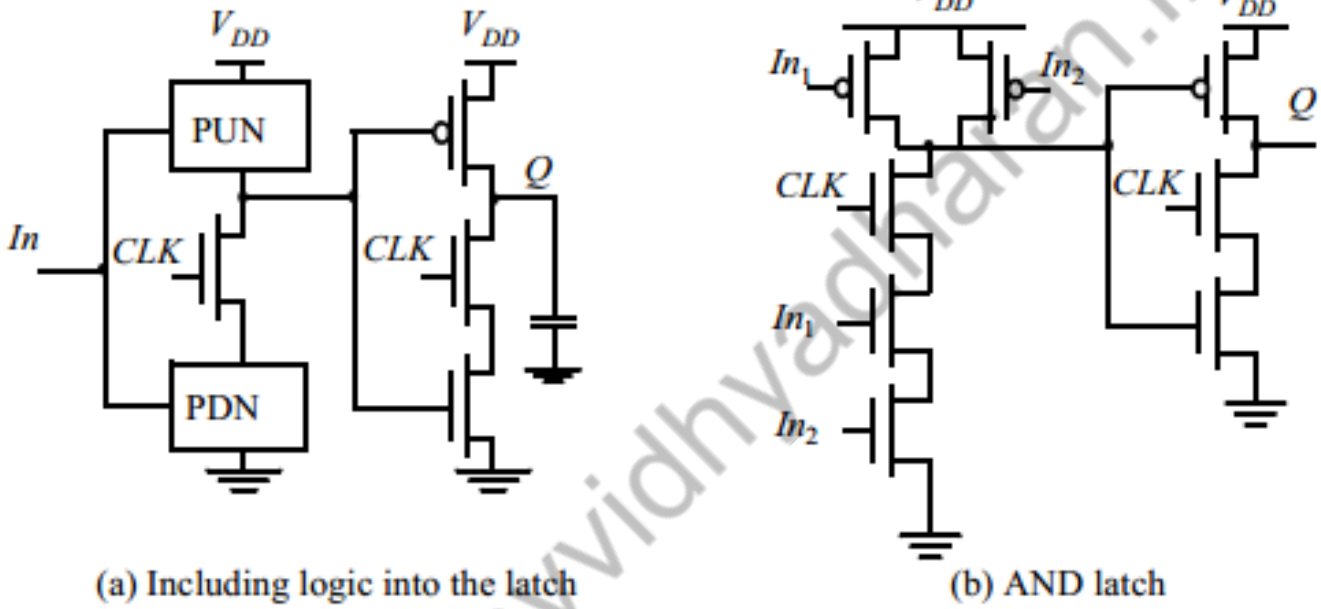
- TSPC offers an additional advantage: the possibility of embedding logic functionality into the latches.
- This reduces the delay overhead associated with the latches.
- This approach of embedding logic into latches has been used extensively in the design of high-performance processors.



(a) Including logic into the latch

(b) AND latch

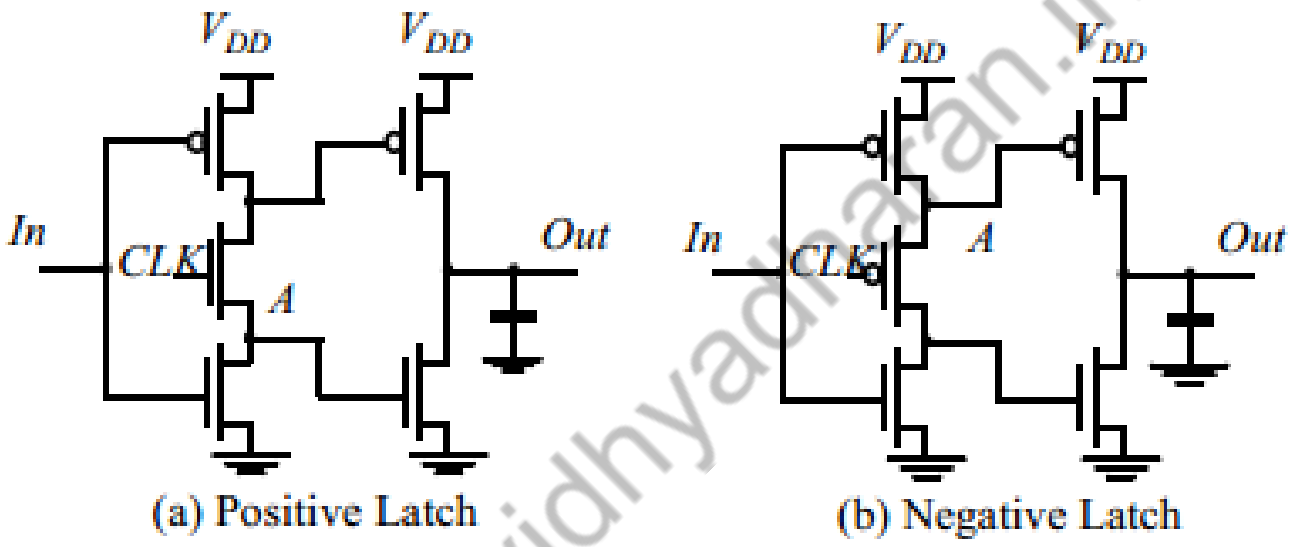
True Single-Phase Clocked Register (TSPCR)



(a) Including logic into the latch (b) AND latch

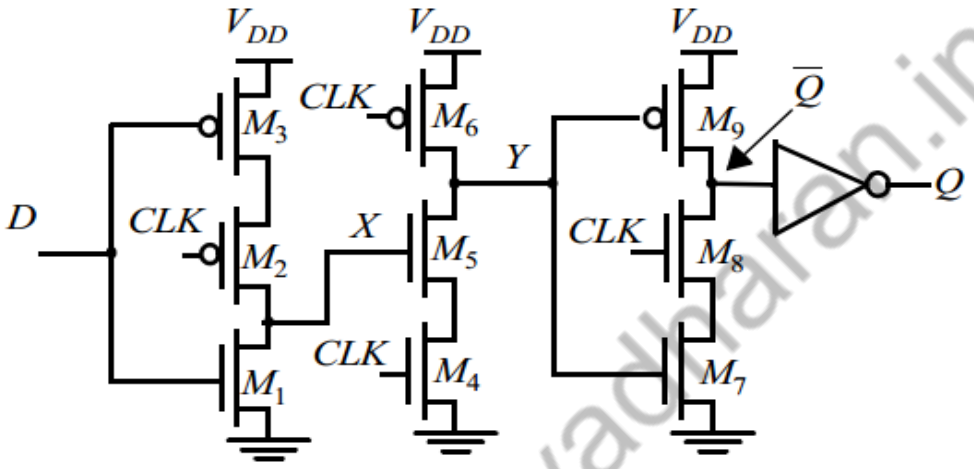
In a 0.25 μm, the *set-up time* of such a circuit using minimum-size devices is 140 psec. A conventional approach, composed of an AND gate followed by a positive latch has an effective *set-up time* of 600 psec (we treat the AND plus latch as a black box that performs both functions). The embedded logic approach hence results in significant performance improvements.

True Single-Phase Clocked Register (TSPCR)



- The TSPC latch circuits can be further reduced in complexity, where only the first inverter is controlled by the clock.
- Not all node voltages in the latch experience the full logic swing the voltage at node *A* (for *Vin* = 0 V) for the positive latch maximally equals $V_{DD}- V_{Tn}$, which results in a reduced drive for the output NMOS transistor and a loss in performance.

Positive Edge-Triggered Register TSPC



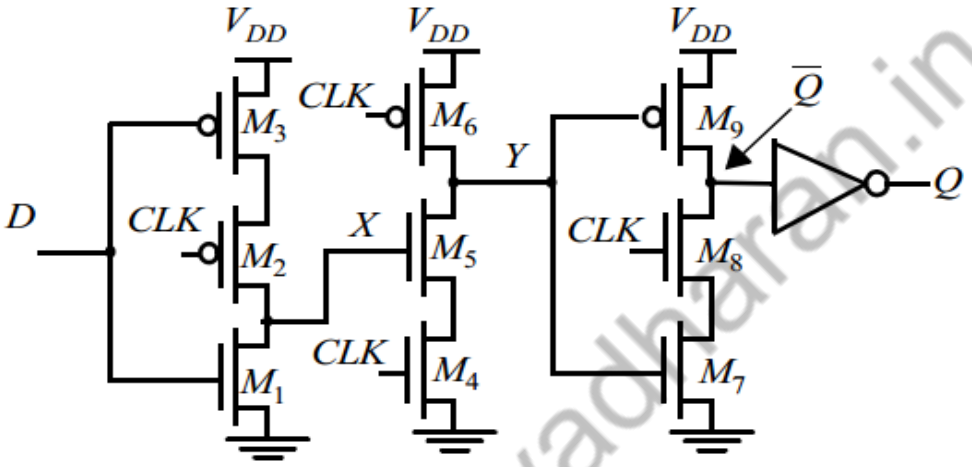
When $CLK = 0$:

The input inverter is sampling the inverted D input on node X.
The second (dynamic) inverter is in the precharge mode, Y to V_{DD}.
The third inverter is in the *hold* mode, since M_8 and M_9 are *off*.

On the rising edge of the clock :

The dynamic inverter M_4-M_6 evaluates. If X is high on the rising edge, Y discharges.
The third inverter M_7-M_8 is on during the high phase, and the node value on Y is passed to the output Q.

Positive Edge-Triggered Register TSPC



Hold Time: On the positive phase of the clock, note that node *X* transitions to a low if the *D* input transitions to a high level. Therefore, the input must be kept stable till the value on node *X* before the rising edge of the clock propagates to *Y*. This represents the *hold time* of the register (note that the *hold time* less than 1 inverter delay since it takes 1 delay for the input to affect node *X*).

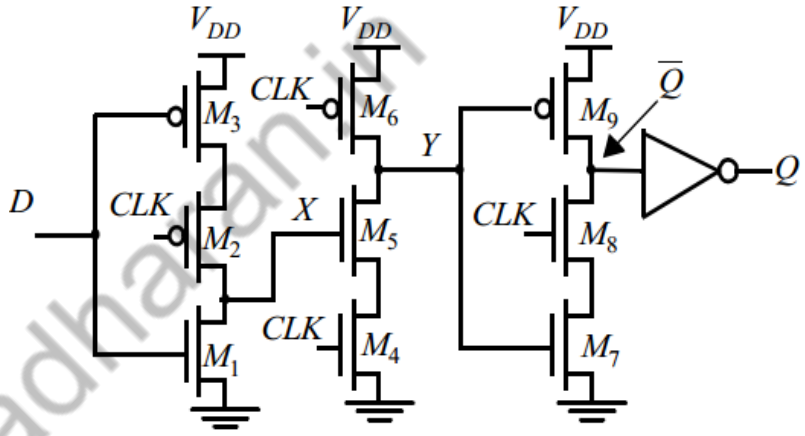
Set-up Time: The *set-up time* is the time for node *X* to be valid, which is one inverter delay.

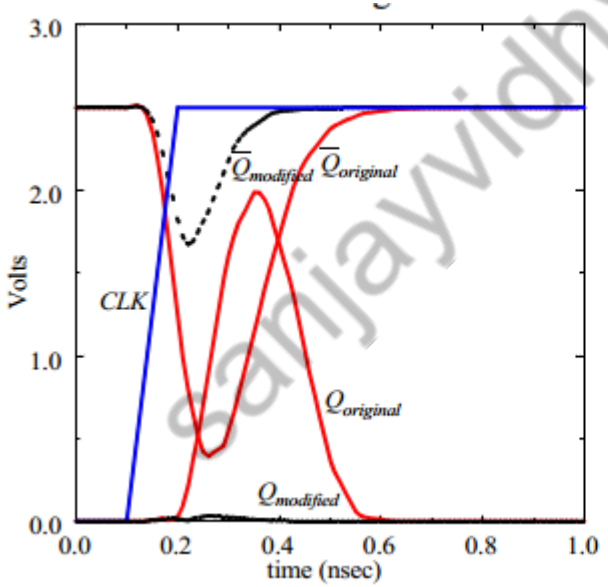
Propagation Delay : The *propagation delay* of the register is essentially three inverters since the value on node *X* must propagate to the output *Q*.

Positive Edge-Triggered Register TSPC

Transistor sizing is critical to avoid Glitch

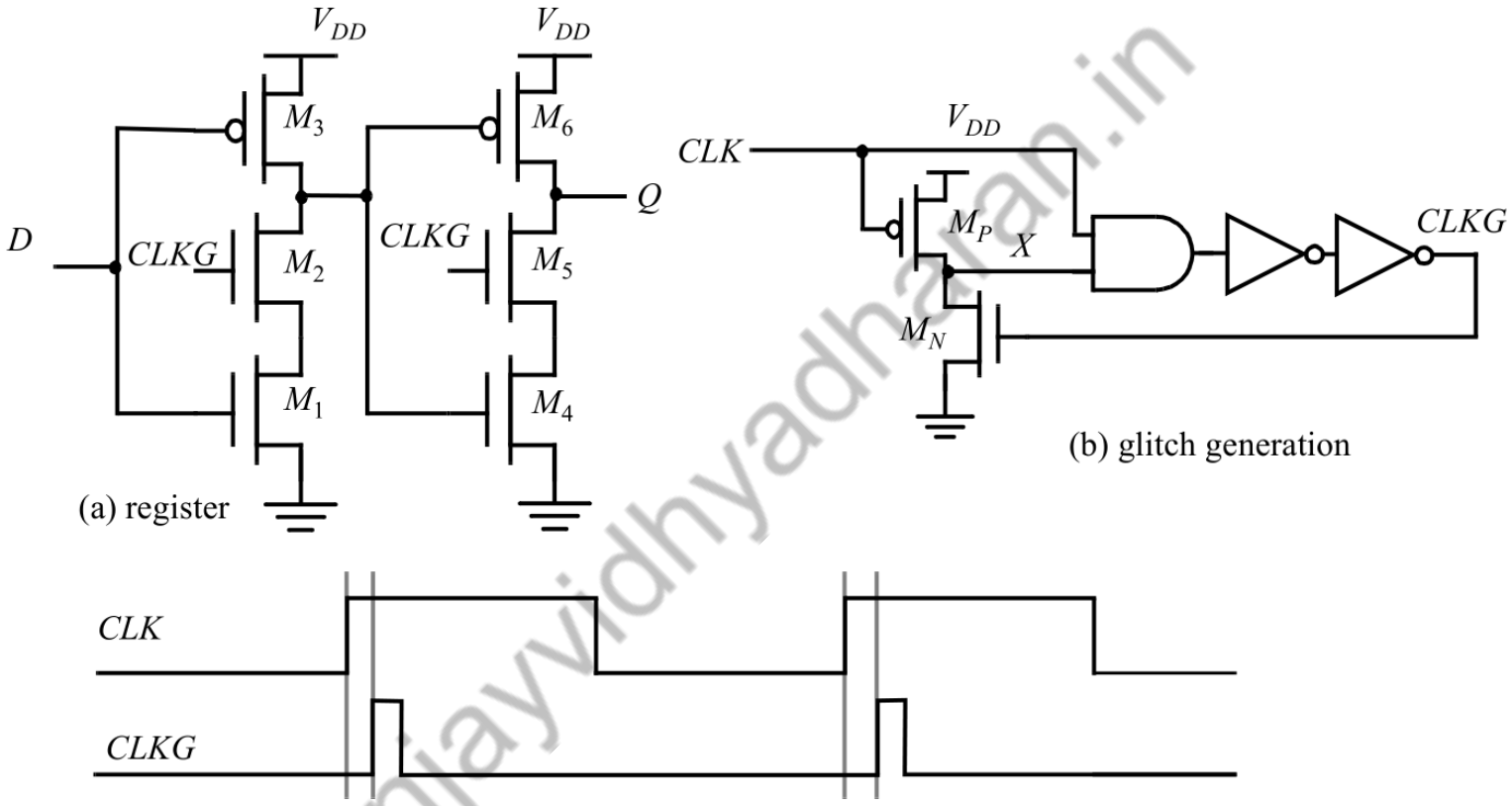
- Case D is 0
  - Y and Q' Both pulled to Zero initially and Q' pulled up again after Y brough sufficiently low
  - M4 & M5 needs to be made stronger w.r.t. M7 & M8





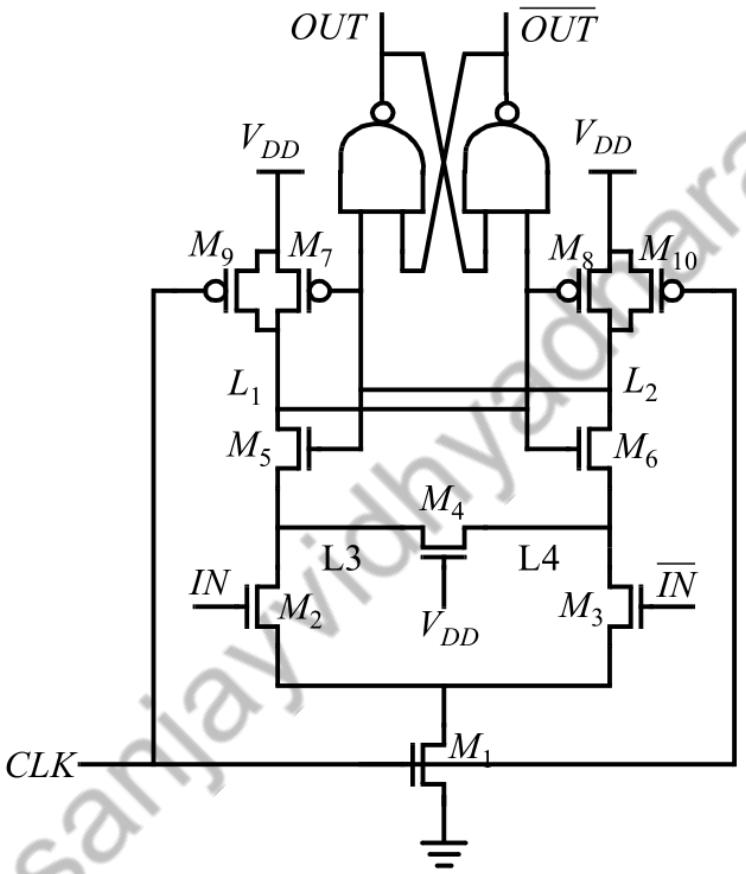
	M_4, M_5	M_7, M_8
Original Width	0.5µm	2µm
Modified Width	1µm	1µm

Pulse Register



- Propagation Delay : Two Inverter Delay
- Set-up Time : Nil
- Hold Time : Glitch Time
- The disadvantage is a substantial increase in verification complexity

Sense amplifier Register



Sense amplifier circuits are used extensively in memory cores and in low swing bus drivers to amplify small voltage swings present in heavily loaded wires.

Thank you