VLSI Design : 2021-22
Lecture 3
Deep-Submicron MOSFET operation

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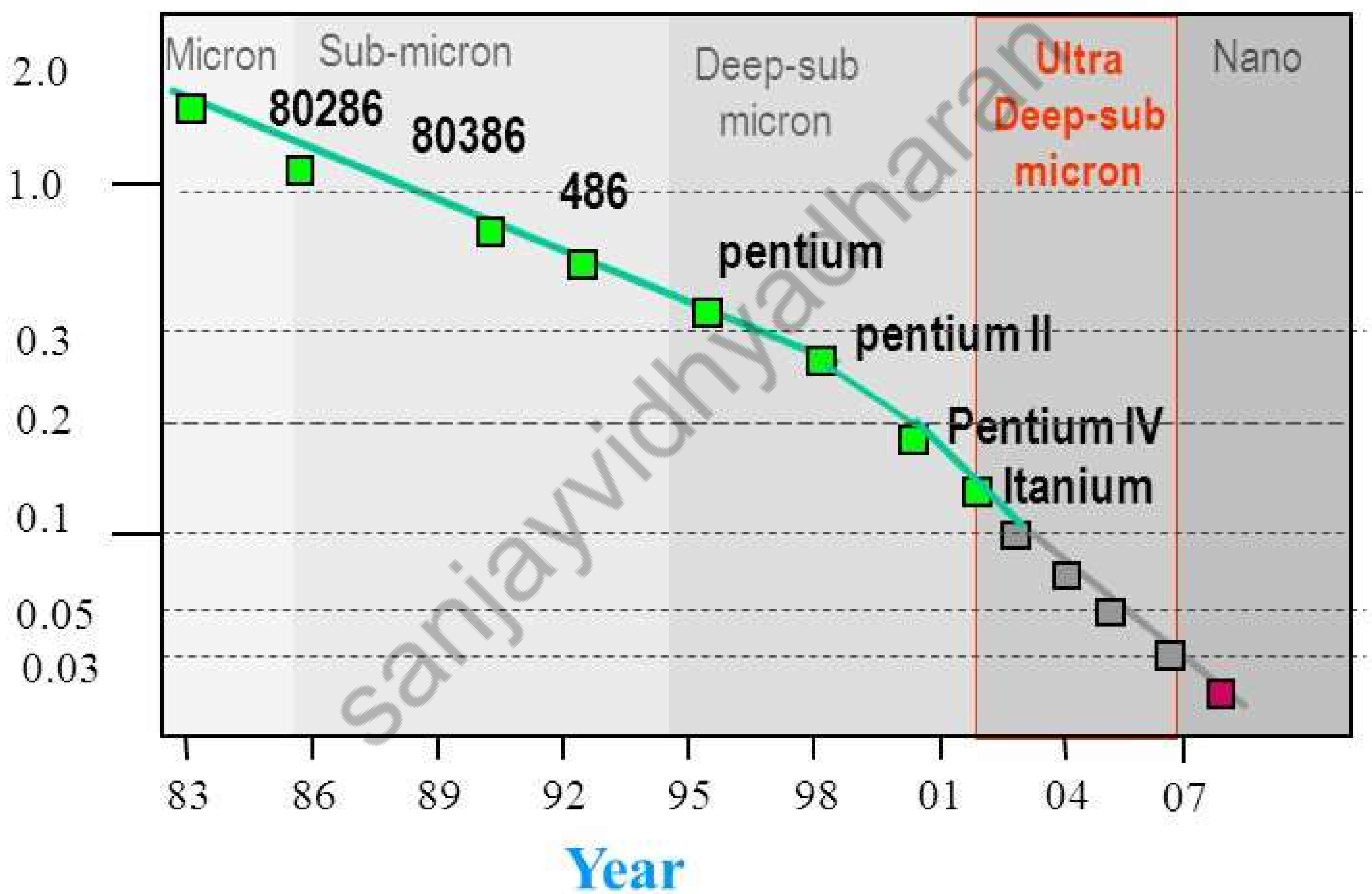
Deep-submicron MOSFET operation

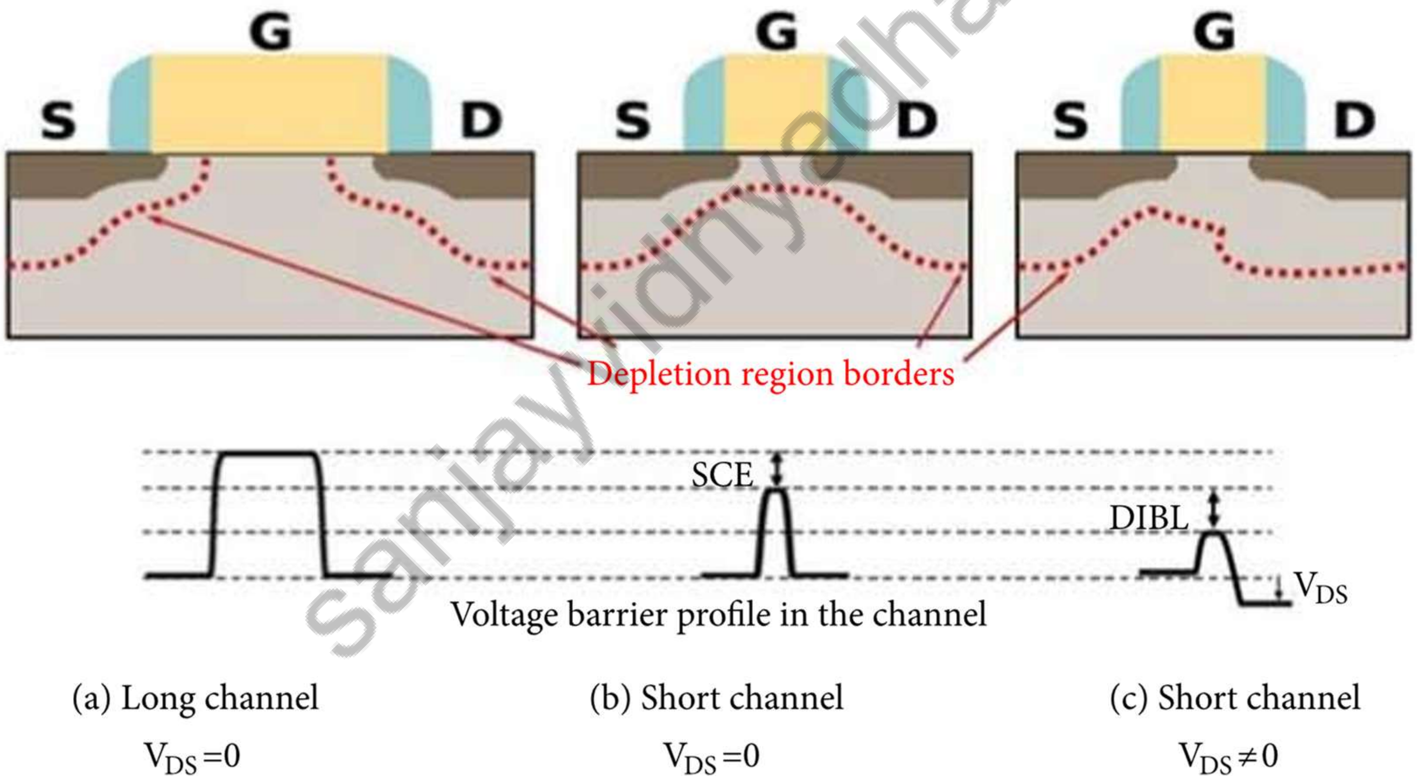


Deep-submicron MOSFET operation

- Threshold voltage reduction
  - VT Roll Off
  - Drain-induced barrier lowering (DIBL)
- Mobility degradation due to a vertical field
- Velocity saturation effects
- Channel length modulation
- Subthreshold (weak inversion) conduction
- Hot-electron effects on output resistance

VT Variation

- VT Roll Off
- Drain-induced barrier lowering (DIBL)



Mobility Degradation

There also exists a normal (vertical) field originating from the gate voltage that further inhibits channel carrier mobility. This effect, which is called mobility degradation, reduces the surface mobility with respect to the bulk mobility.

$$\mu_{n,eff} = \frac{\mu_{n0}}{1 + \eta(V_{GS} - V_T)}$$

with μ_{n0} the bulk mobility and η an empirical parameter.

Velocity Saturation Effect

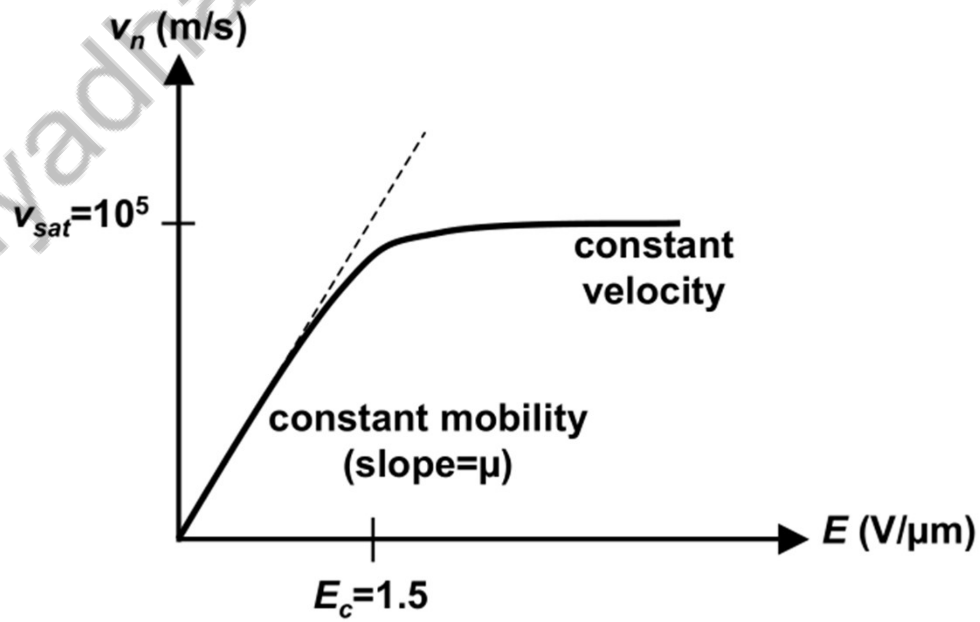
When the electric field reaches a critical value EC the velocity of the carriers tends to saturate.

$$v = \frac{\mu_n E}{1 + E/E_C} \qquad \text{for } E \le E_C$$

$$v = v_{sat} \qquad \text{for } E \ge E_C$$

$$v_{sat} = \begin{cases} 8\times10^6 \text{ cm/s} & \text{for electrons in Si} \\ 6\times10^6 \text{ cm/s} & \text{for holes in Si} \end{cases}$$

$$\varepsilon_{sat} = \frac{2v_{sat}}{\mu}$$



Velocity Saturation Effect

- **Linear region:**

$$I_{DS} = \frac{\frac{W}{L} C_{oxe} \mu_{eff,n} \left(V_{GS} - V_{Tn} - \frac{m}{2} V_{DS} \right) V_{DS}}{1 + \frac{V_{DS}}{\mathcal{E}_{sat} L}}$$

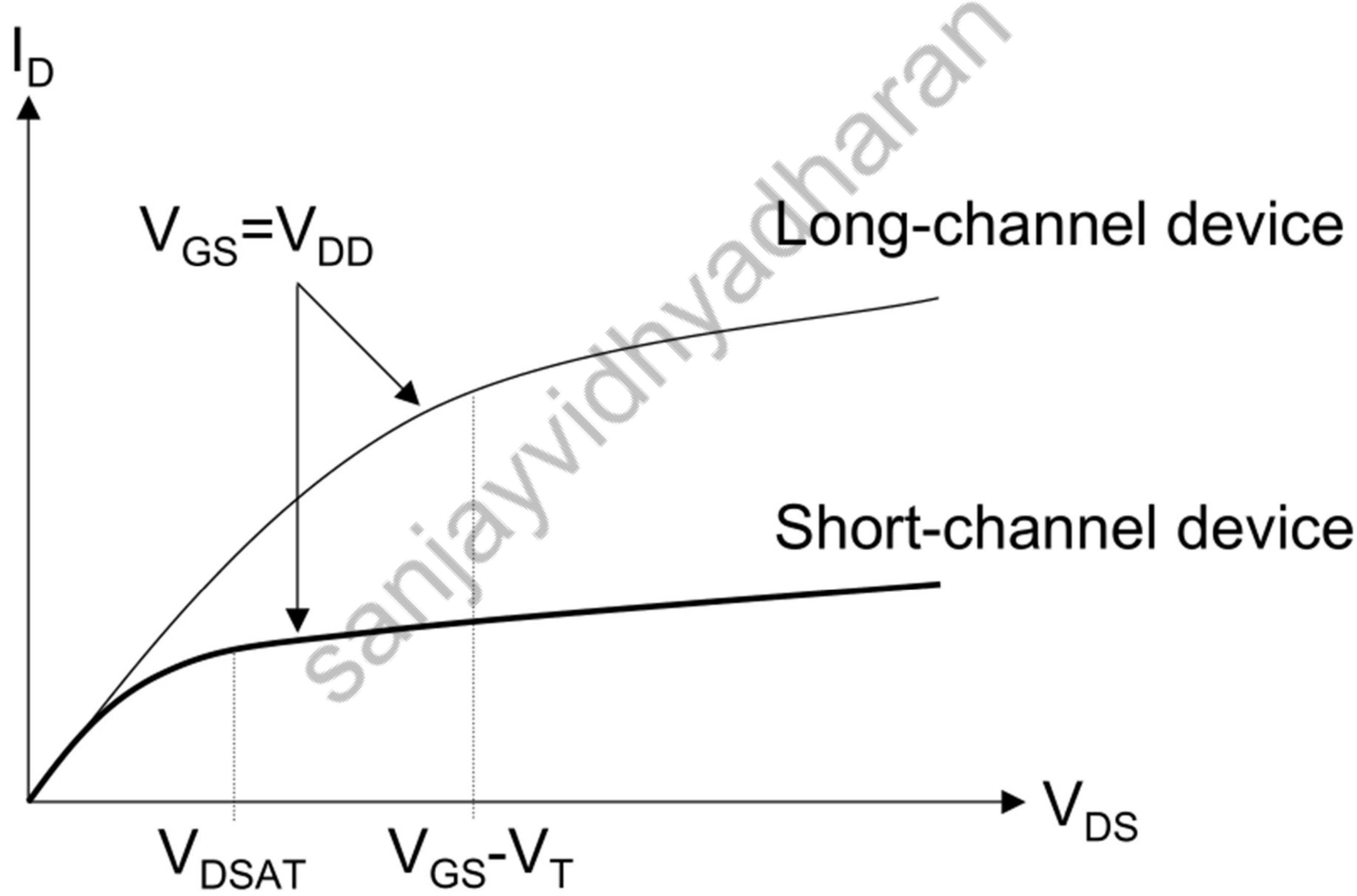
- **Saturation region:**

$$I_{DS} = I_{DSsat} = \frac{\frac{W}{2mL} C_{oxe} \mu_{eff,n} \left(V_{GS} - V_T \right)^2}{1 + \frac{V_{GS} - V_T}{\mathcal{E}_{sat} L}} \qquad \mathcal{E}_{sat} = \frac{2 v_{sat}}{\mu}$$

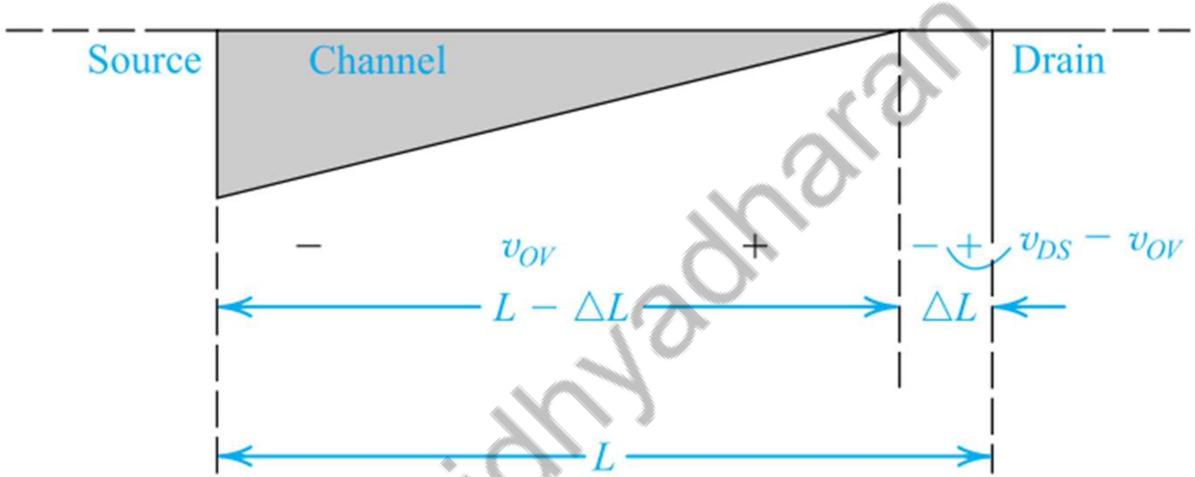
$v_{sat} = 8 \times 10^6$ cm/s

for electrons in Si

Velocity Saturation Effect

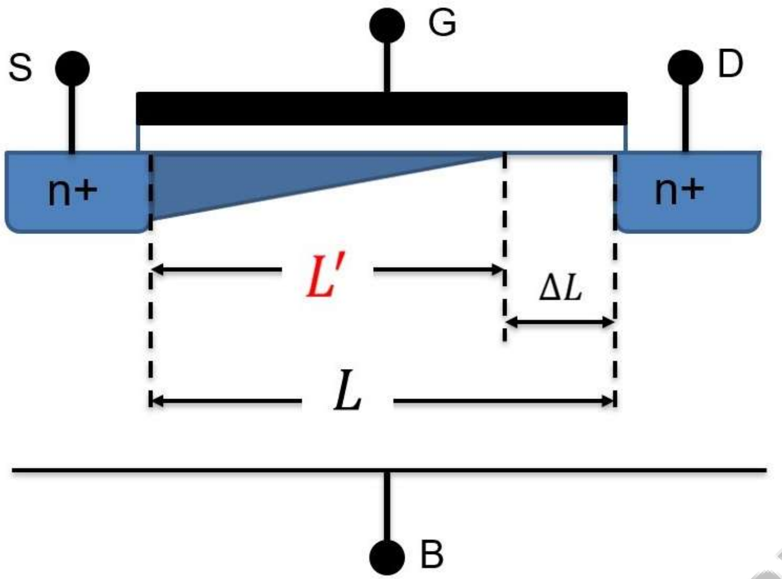


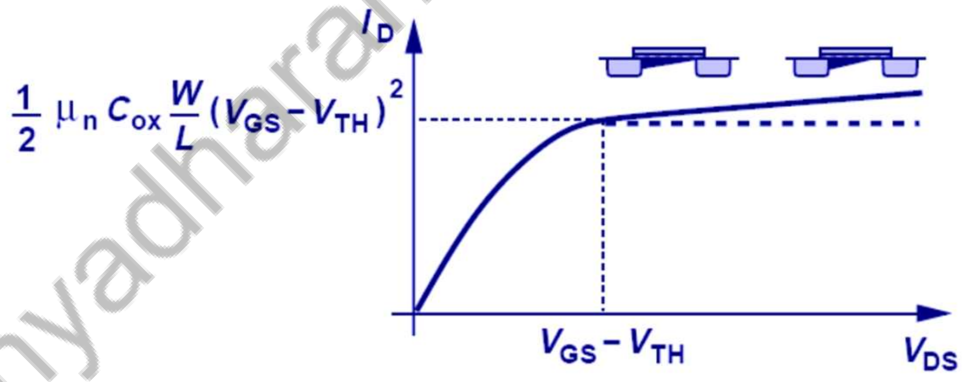
Channel Length Modulation



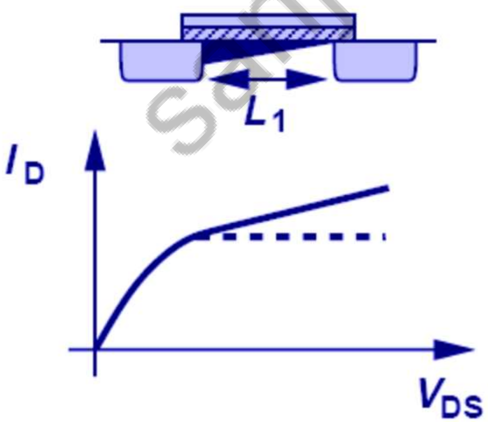
When the V_{DS} is increased beyond V_{OV} , the pinch-off point is moved slightly away from the drain, toward the source. The additional voltage applied to the drain appears as a voltage drop across the narrow depletion region between the end of the channel and the drain region. This voltage accelerates the electrons that reach the drain end of the channel and sweeps them across the depletion region into the drain.

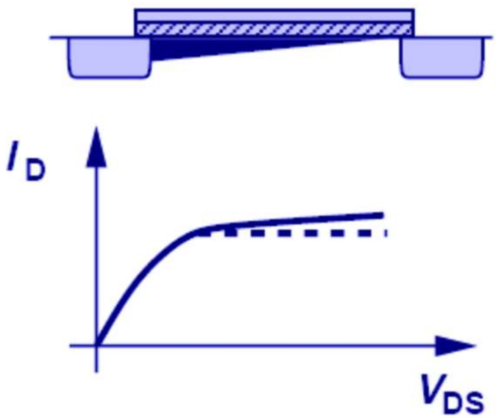
Channel Length Modulation



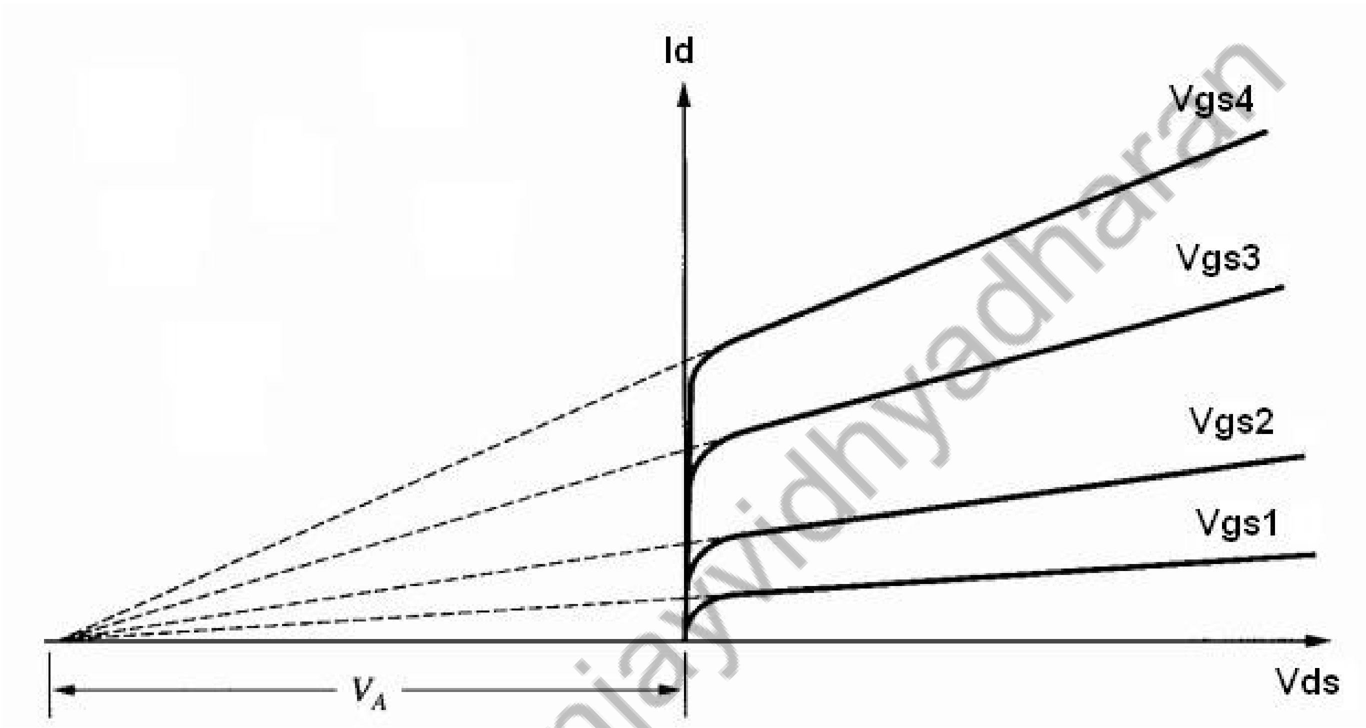


$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2(1+\lambda V_{DS})$$





Channel Length Modulation



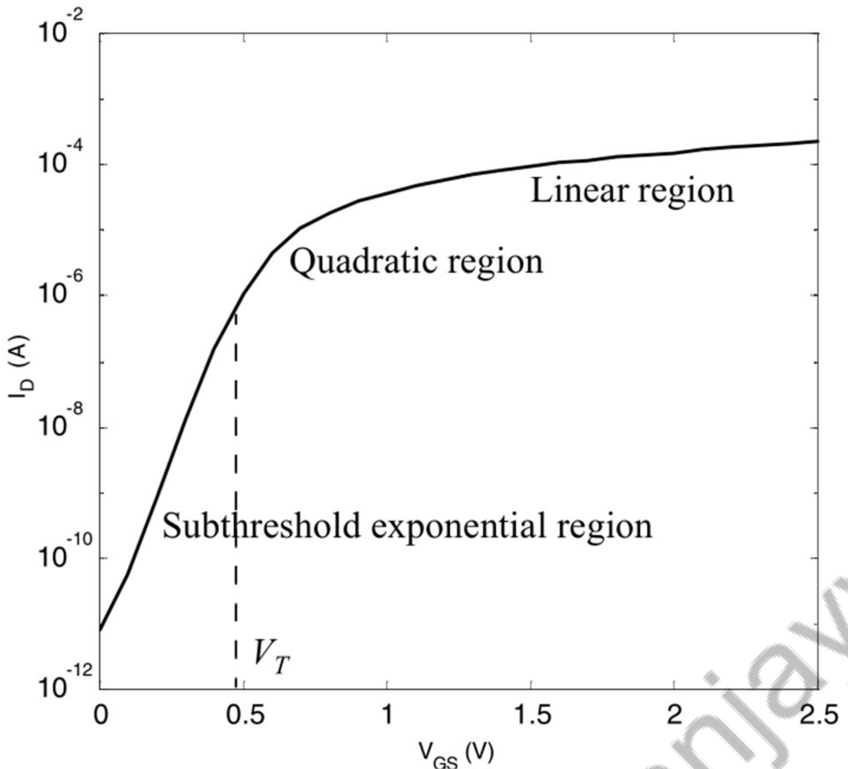
V_A *Early Voltage*

$$\lambda = \frac{1}{V_A}$$

$$r_o \approx \frac{1}{\lambda I_D}$$

$$\lambda \propto 1/L$$

Subthreshold Conduction



$$I_D = I_S e^{\frac{V_{GS}}{nkT/q}}\left(1 - e^{-\frac{V_{DS}}{kT/q}}\right)$$

where I_S and n are empirical parameters, with $n \geq 1$ and typically ranging around 1.5.

Subthreshold current has some important repercussions. In general, we want the current through the transistor to be as close as possible to zero at $V_{GS} = 0$. This is especially important in the so-called dynamic circuits, which rely on the storage of charge on a capacitor and whose operation can be severely degraded by subthreshold leakage.

Hot Carrier Effects

Increase in the electric field strength causes an increasing energy of the electrons.

- Some electrons are able to leave the silicon and tunnel into the gate oxide.
- Such electrons are called "Hot carriers".
- Electrons trapped in the oxide change the V_T of the transistors.
- This leads to a long term reliability problem.
- For an electron to become hot an electric field of 10^4 V/cm is necessary.
- This condition is easily met with channel lengths below 1µm.

Thank you