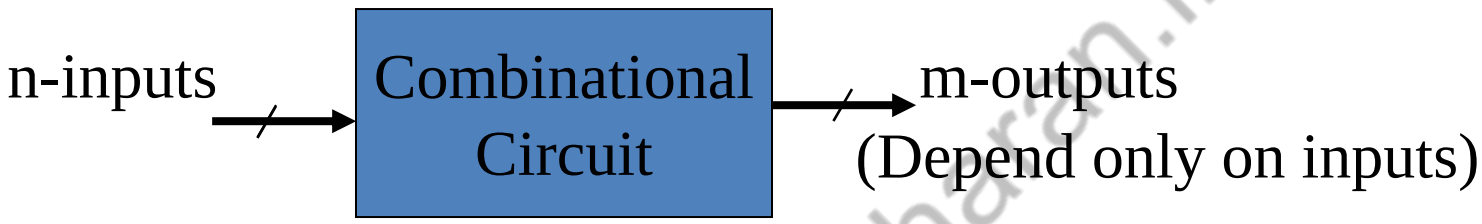
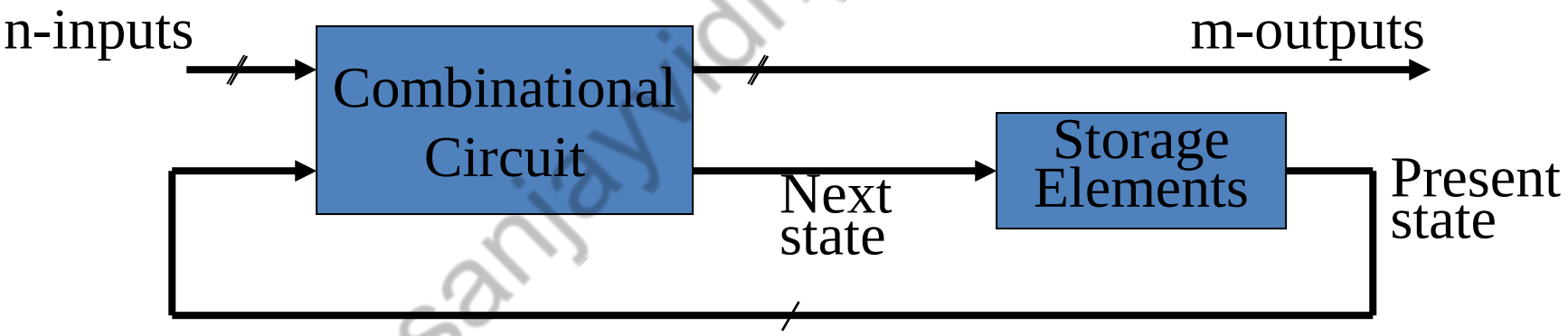
Advanced VLSI Design: 2021-22
Lecture 2
Sequential Circuits: Latch and Flip-flops

By Dr. Sanjay Vidhyadharan

Combinational vs. Sequential Circuits



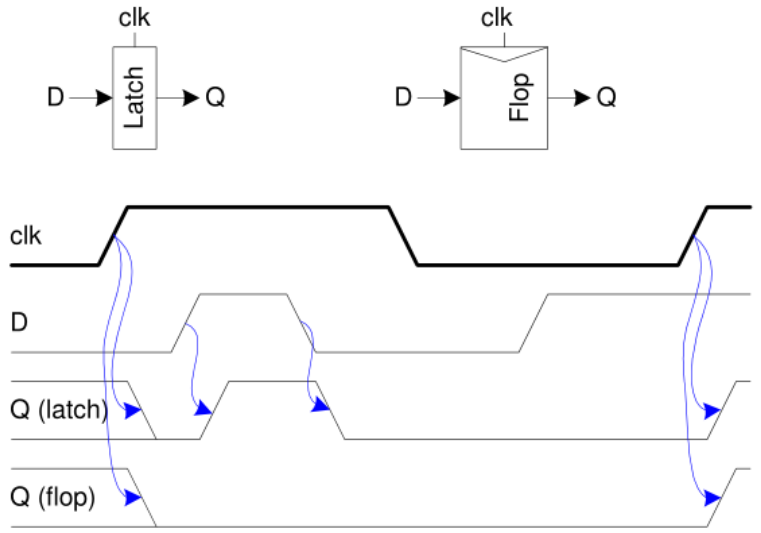
Combinational Circuit



Sequential Circuit

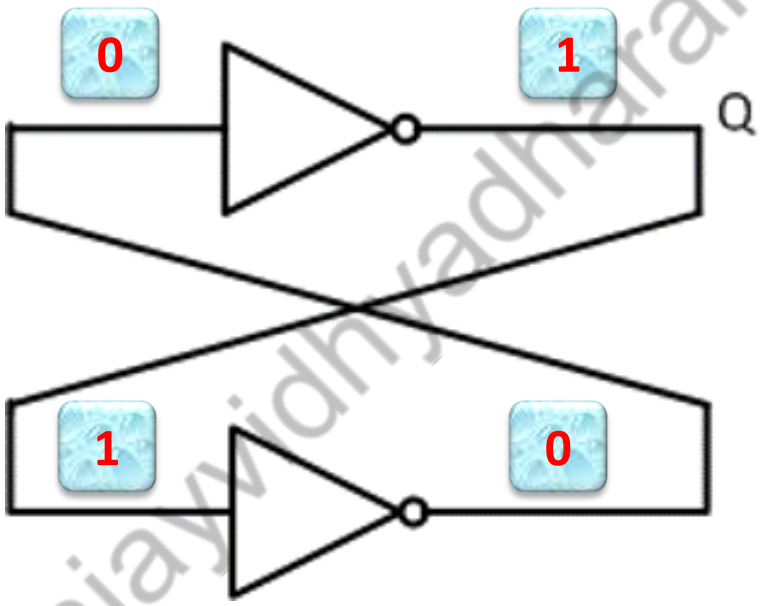
Latch vs. Flip-flop

- **Latch**: Level sensitive
  - a.k.a. transparent latch, D latch
- **Flip-flop**: edge triggered
  - A.k.a. master-slave flip-flop, D flip-flop, D register
- Timing Diagrams
  - Transparent
  - Opaque
  - Edge-trigger



Latch

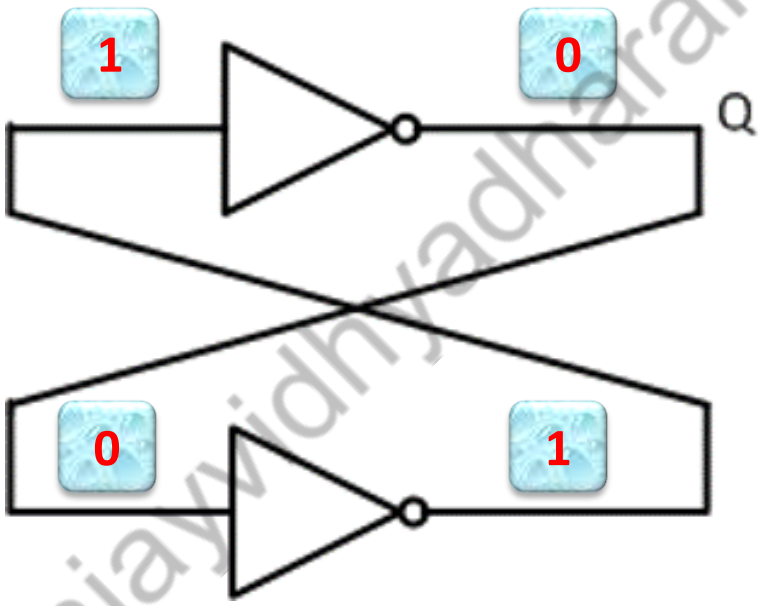
Storing 1



Stores 1 as Long as Power Supply is Provided

Latch

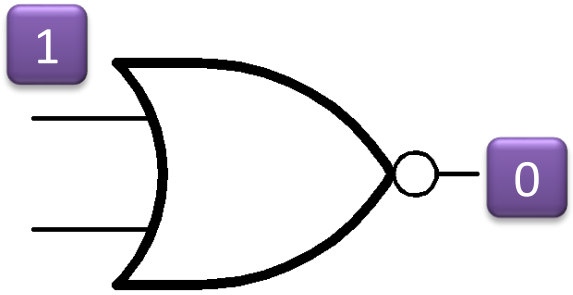
Storing 0

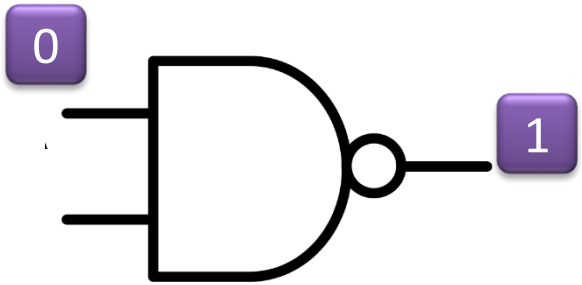


Stores 0 as Long as Power Supply is Provided

Latch

How to Write Data into a Latch?

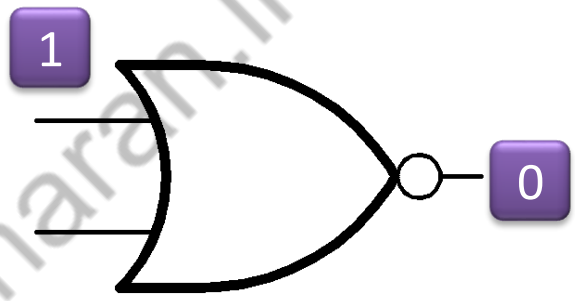


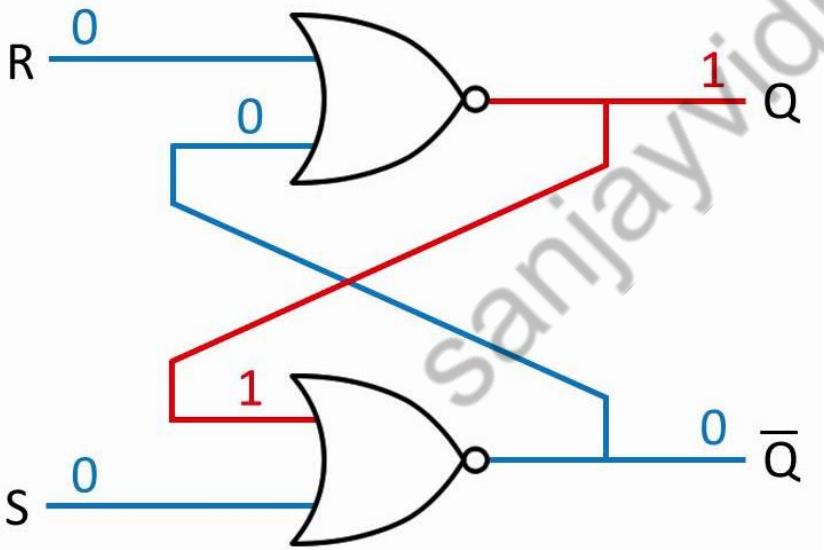


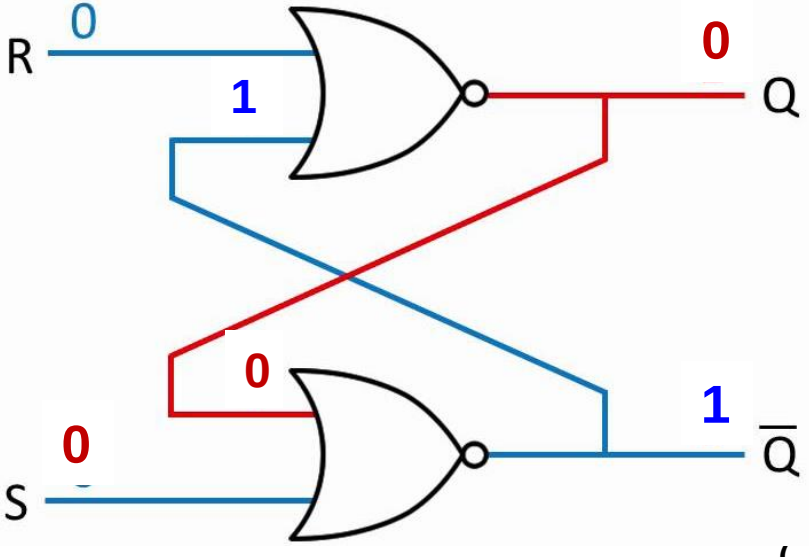
We are going to use this property of NOR and NAND to write data into the latch

SR Latch

S	R	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
0	1	0	1
1	0	1	0
1	1	0	0

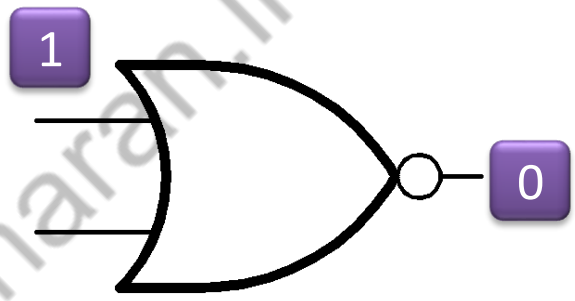


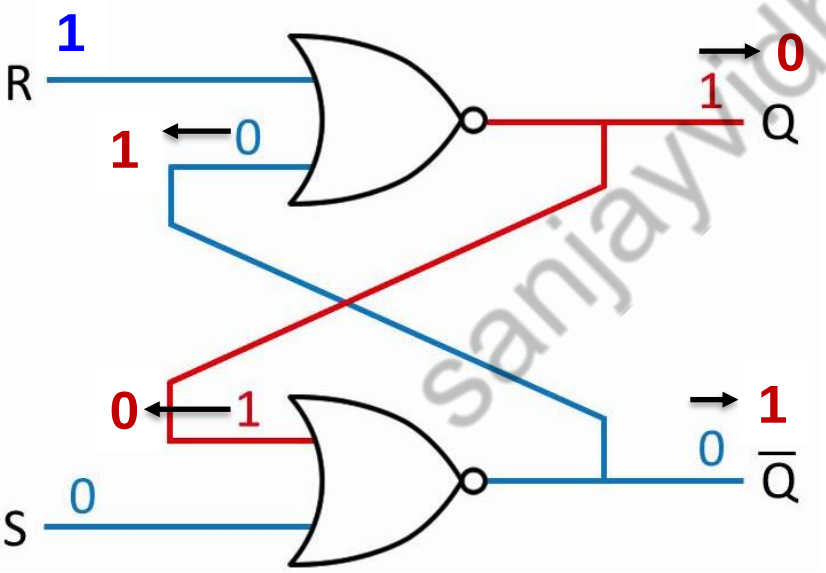


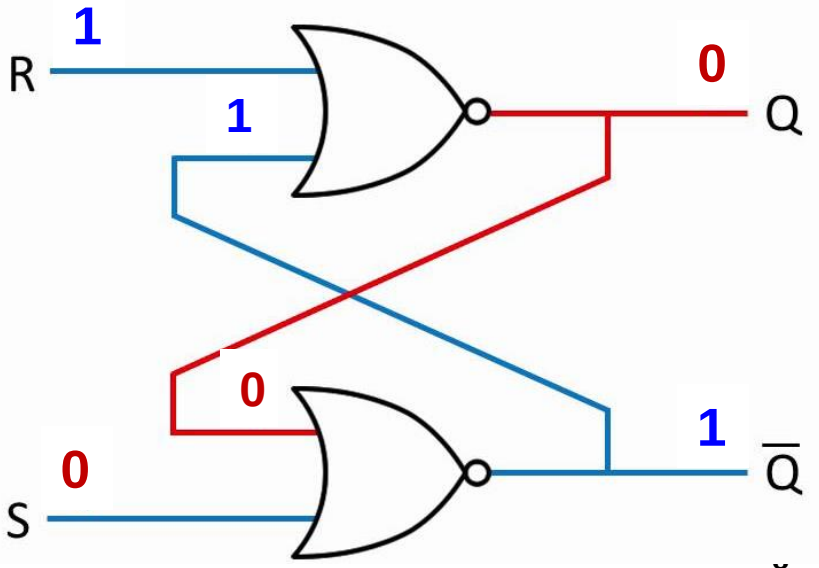


SR Latch

S	R	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
0	1	0	1
1	0	1	0
1	1	0	0

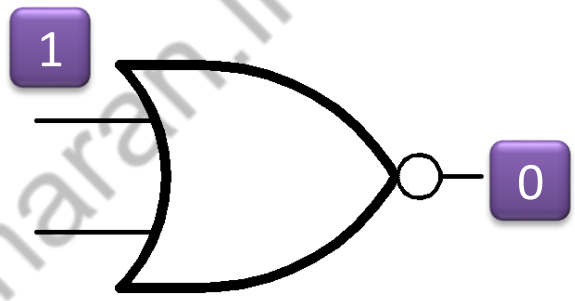


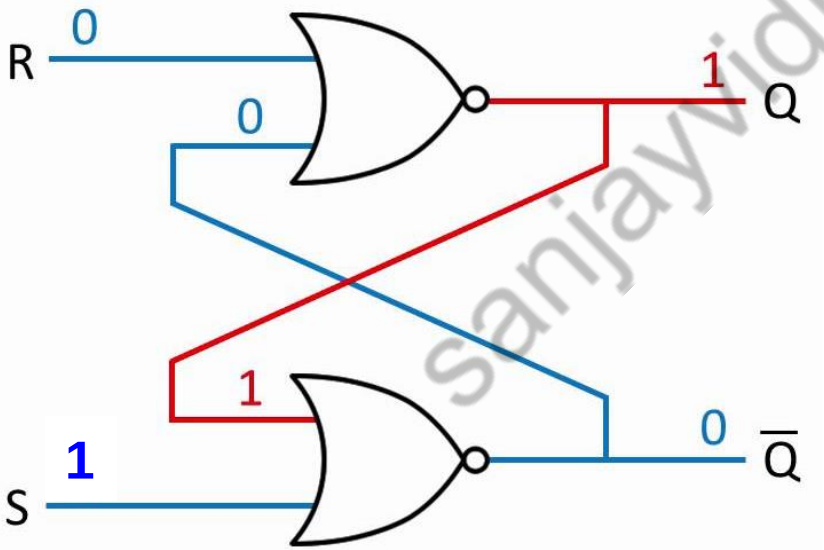


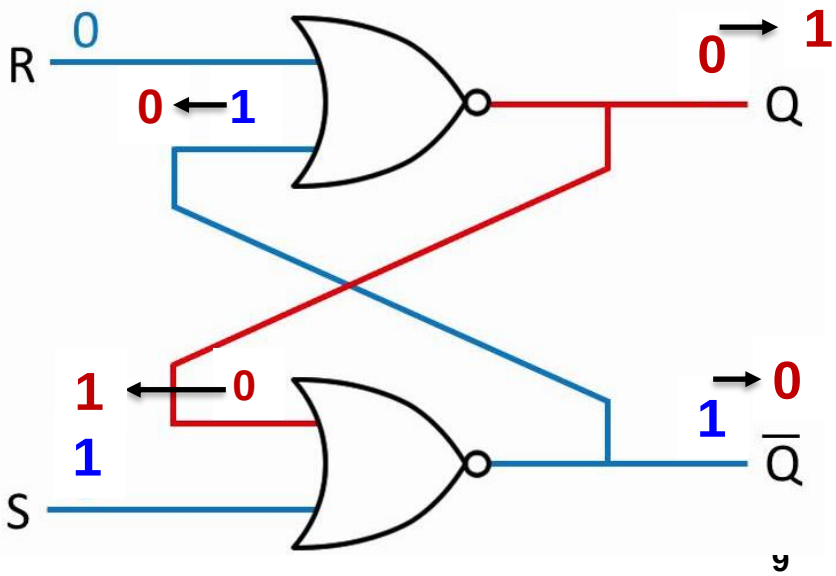


SR Latch

S	R	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
0	1	0	1
1	0	1	0
1	1	0	0





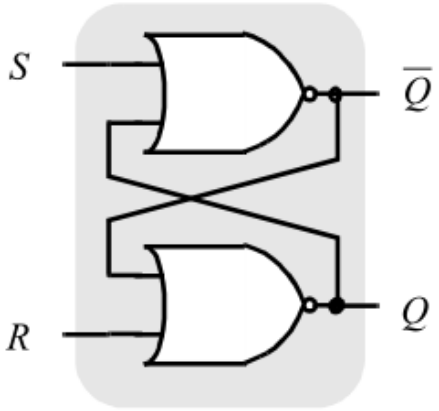


SR Latch

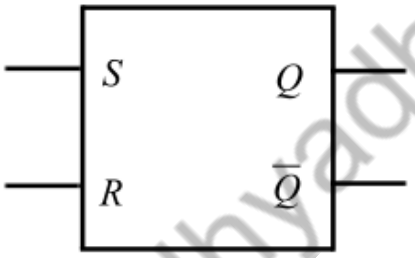
S	R	Q	$\overline{Q}$	
0	0	Q	$\overline{Q}$	No change
0	1	0	1	Reset Q = 0
1	0	1	0	Set Q = 1
1	1	0	0	Forbidden

SR Latch

SR Latch with NOR Gates



(a) Schematic diagram



(b) Logic symbol

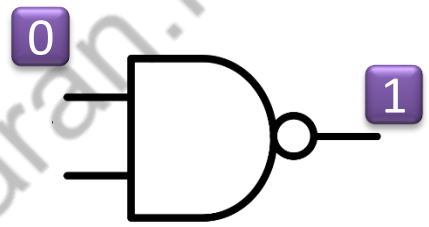
S	R	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
1	0	1	0
0	1	0	1
1	1	0	0

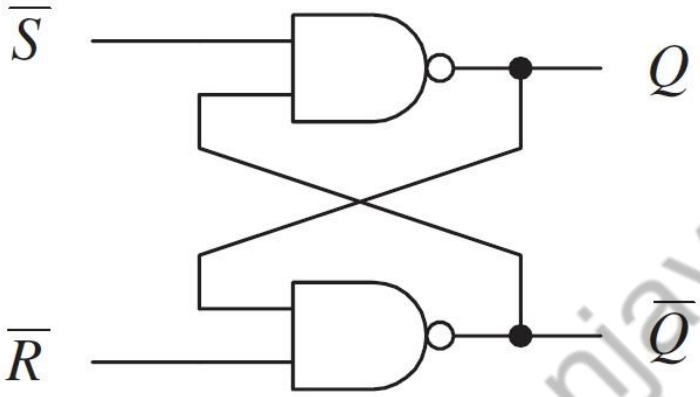
Forbidden State

(c) Characteristic table

SR Latch

SR Latch with NAND Gates

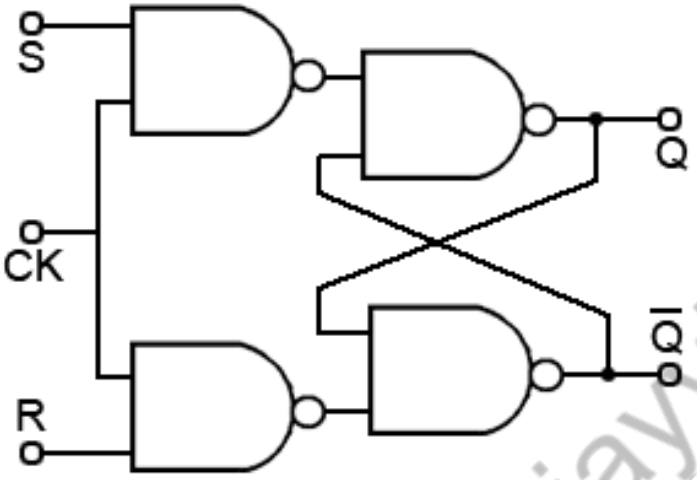




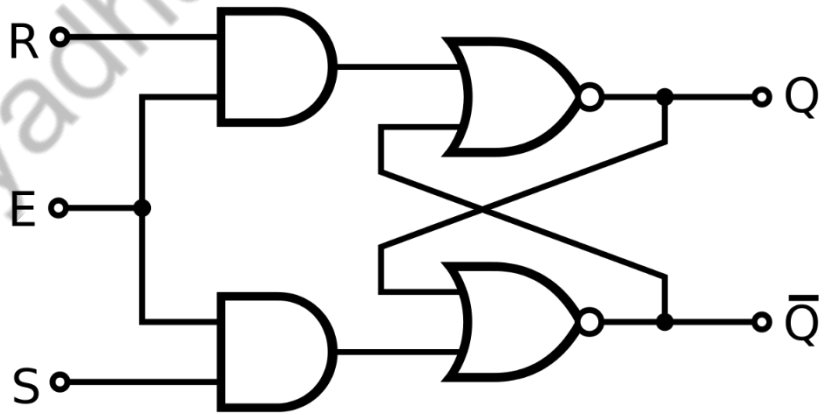
S'	R'	Q	Q'	
0	0	1	1	Forbidden
0	1	1	0	Set
1	0	0	1	Reset
1	1	Q	Q'	No change

SR Latch

Clocked SR Latch



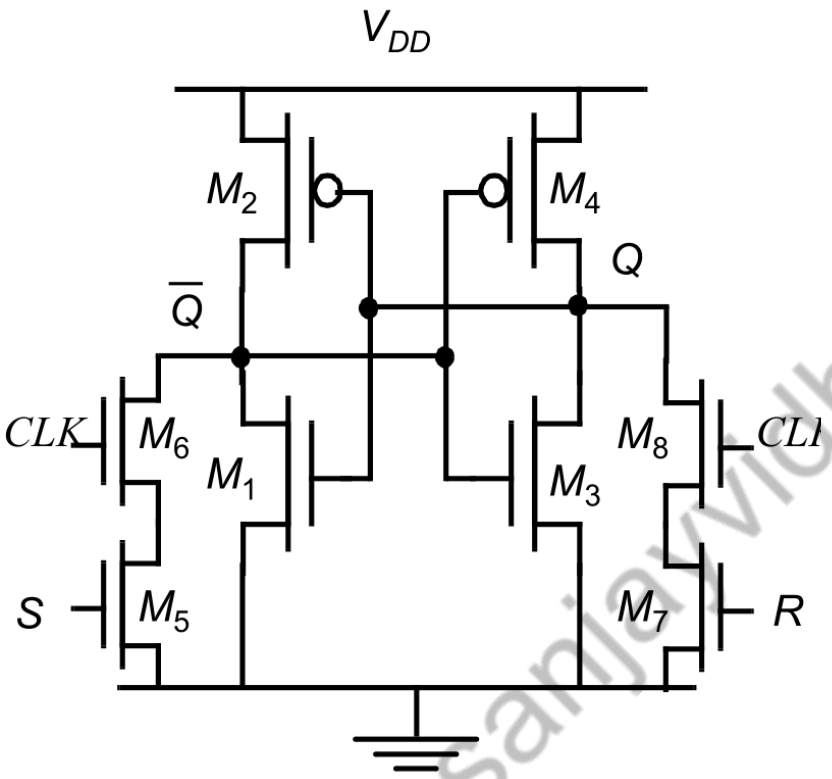
NAND Implementation

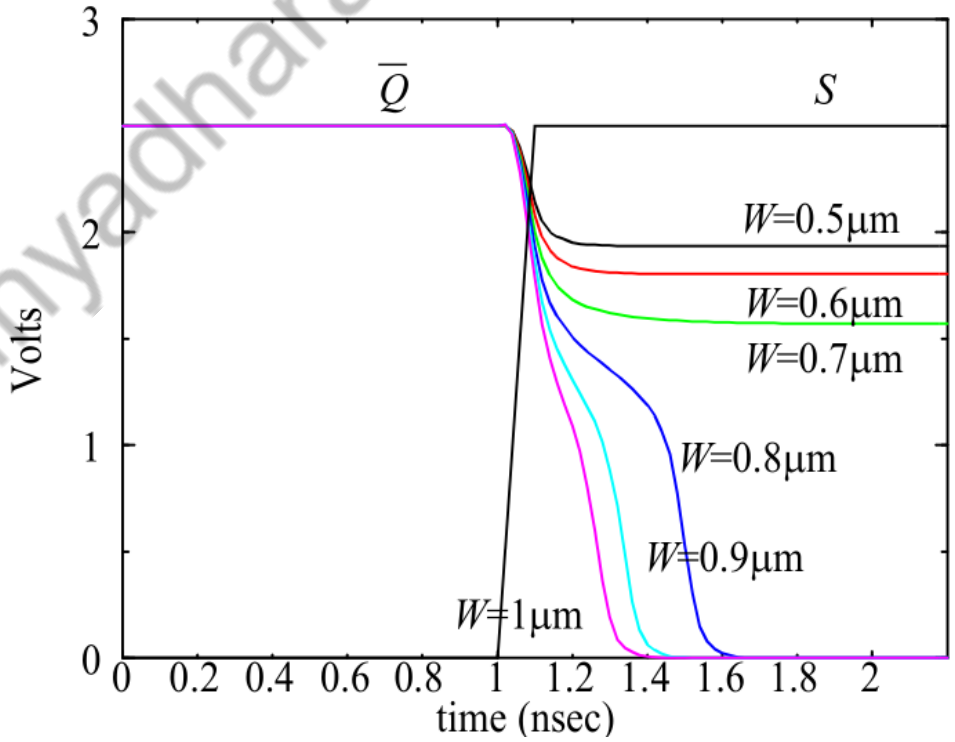


AND-NOR Implementation

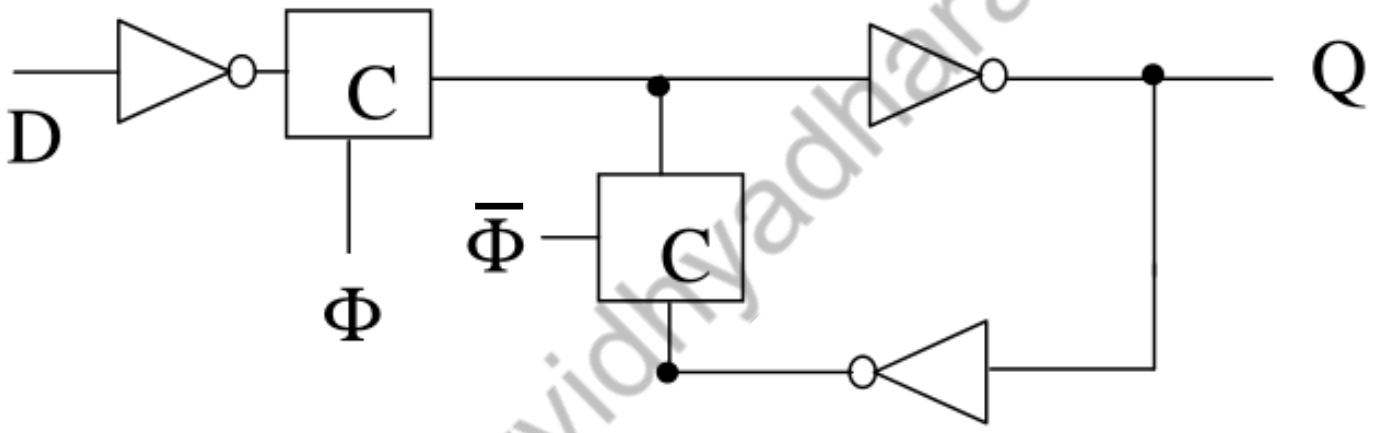
SR Latch

Clocked SR Latch



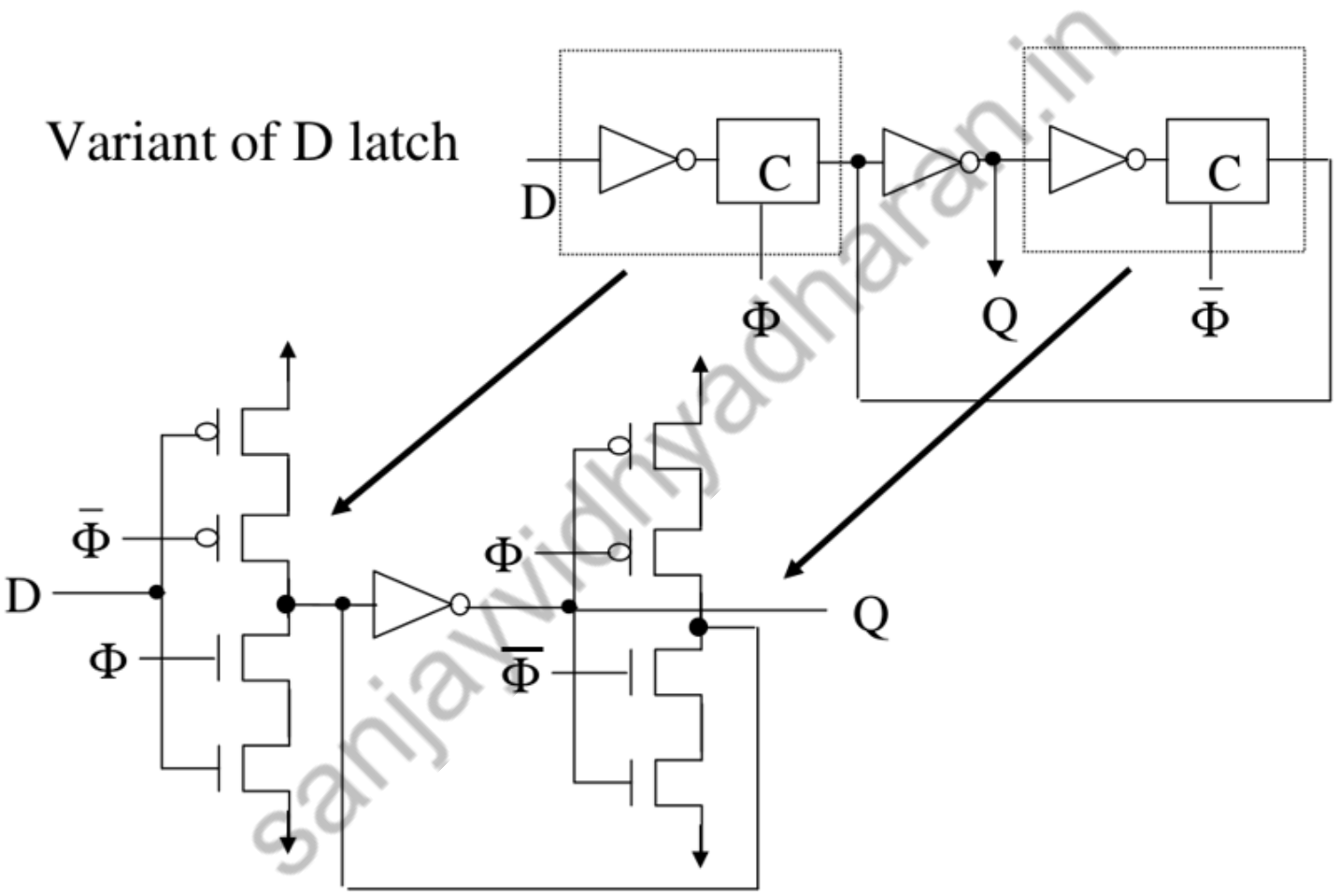


D Latch



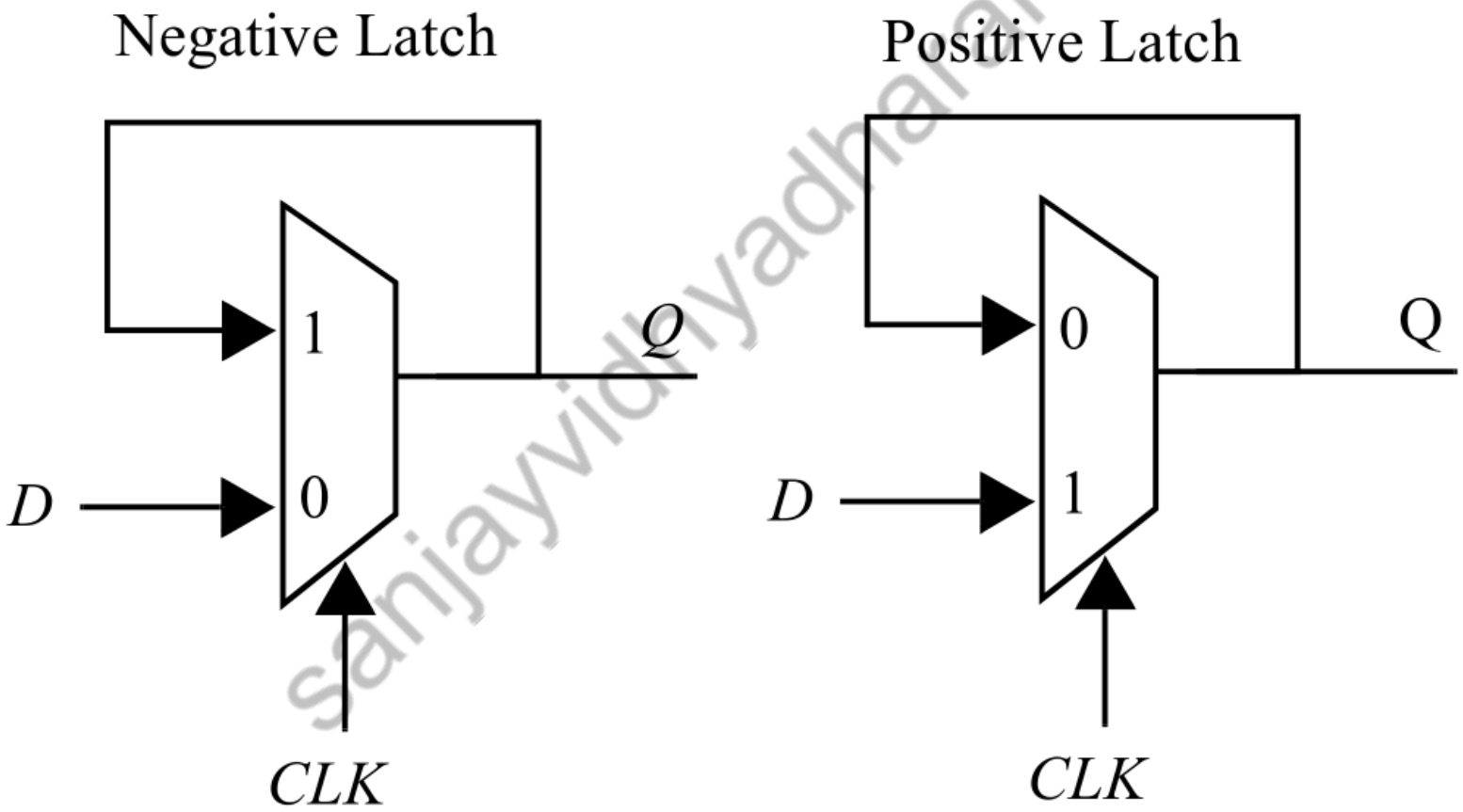
Static D latch

D Latch



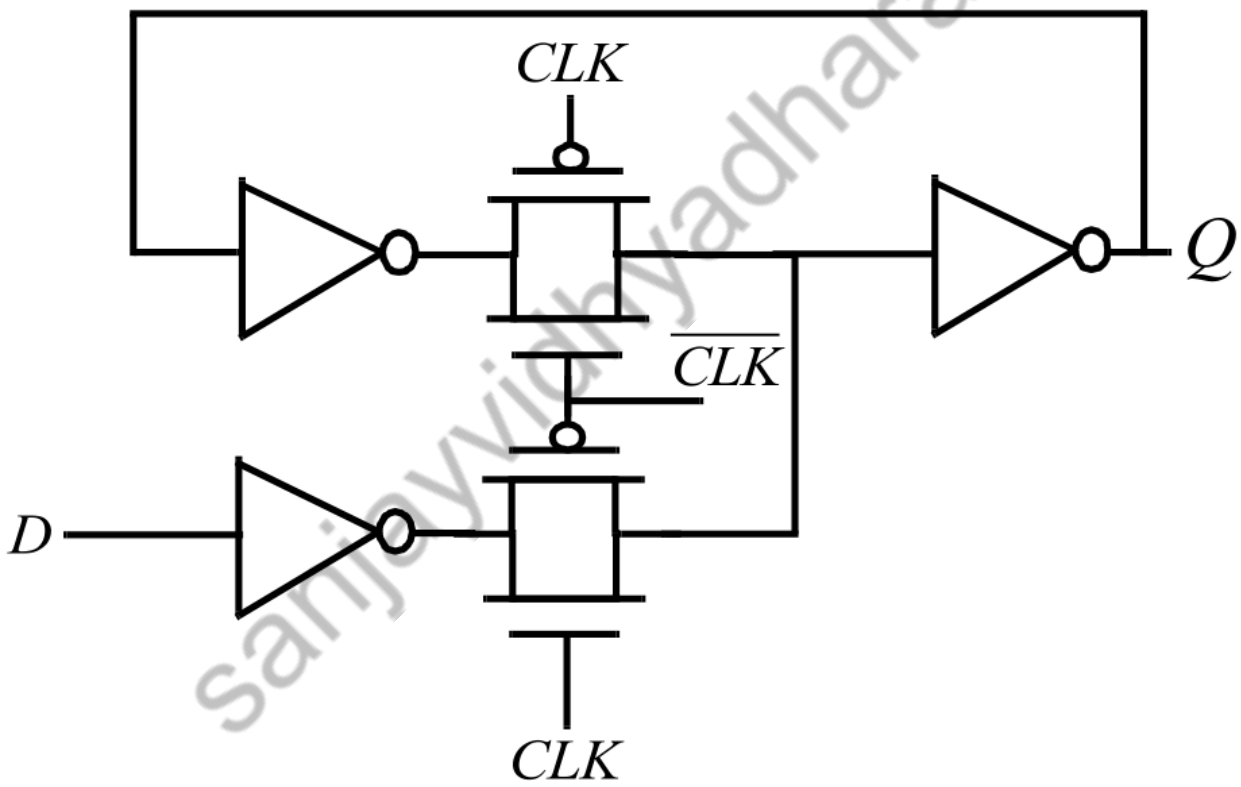
D Latch

Mux Based Latch



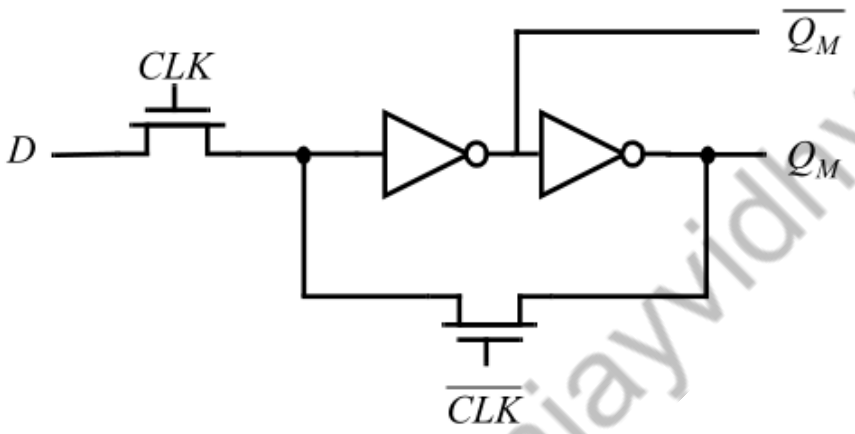
D Latch

Mux Based Latch

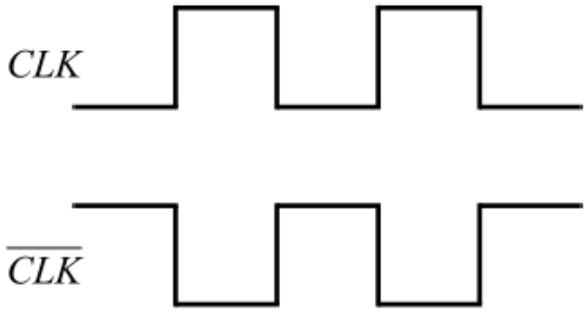


D Latch

Multiplexer-based NMOS latch using NMOS-only pass transistors.

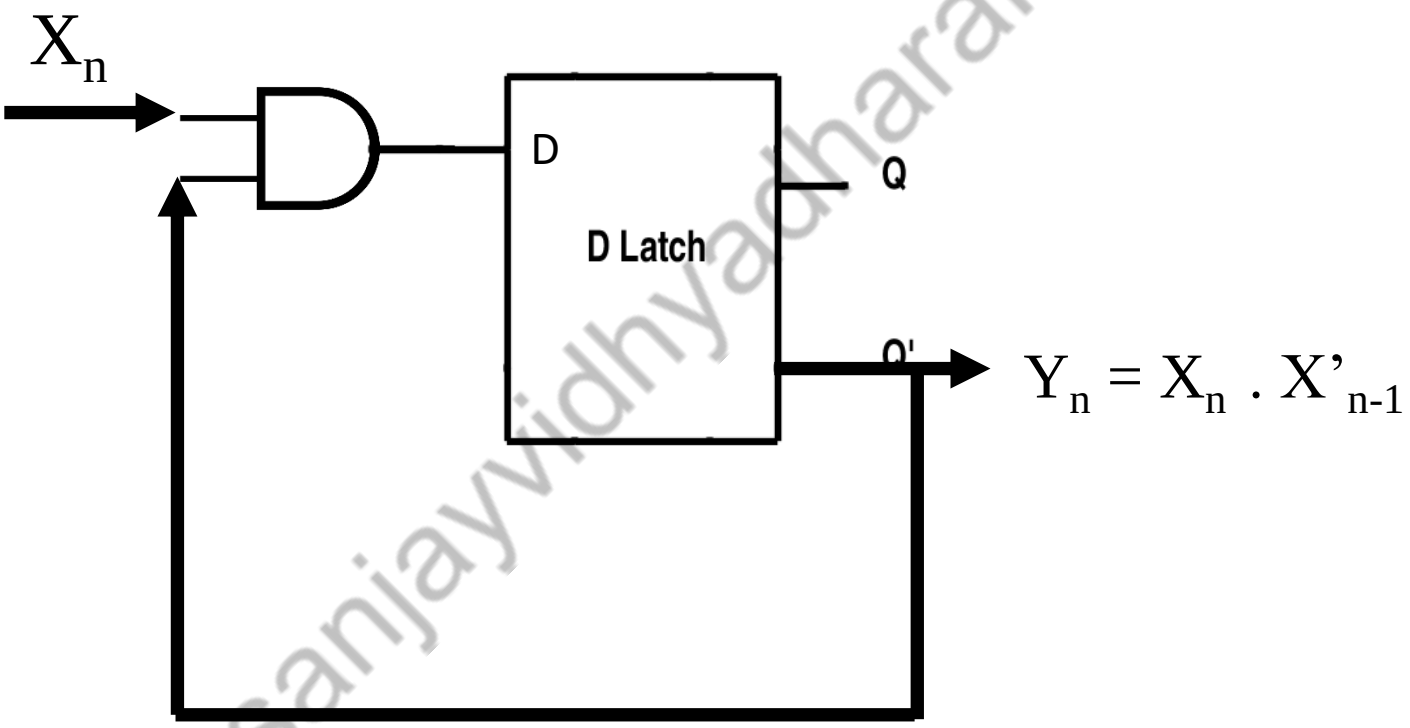


(a) Schematic diagram



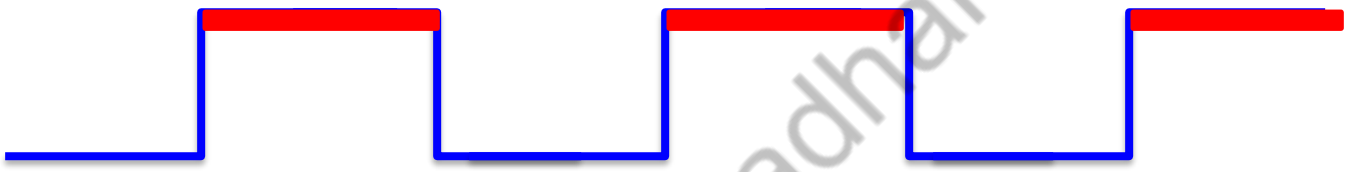
(b) Non-overlapping clocks

Race around in Latches

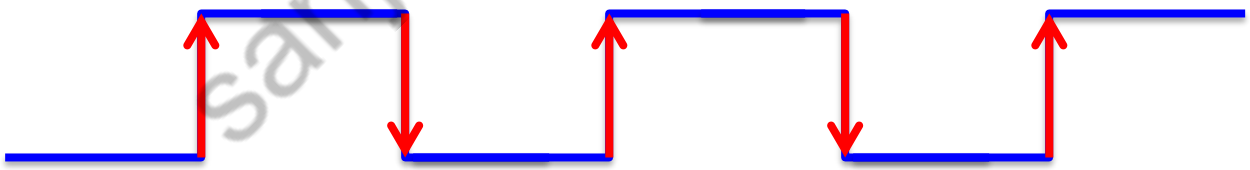


Latch vs. Flip-flop

Latch – Responds to change in level of clock pulse

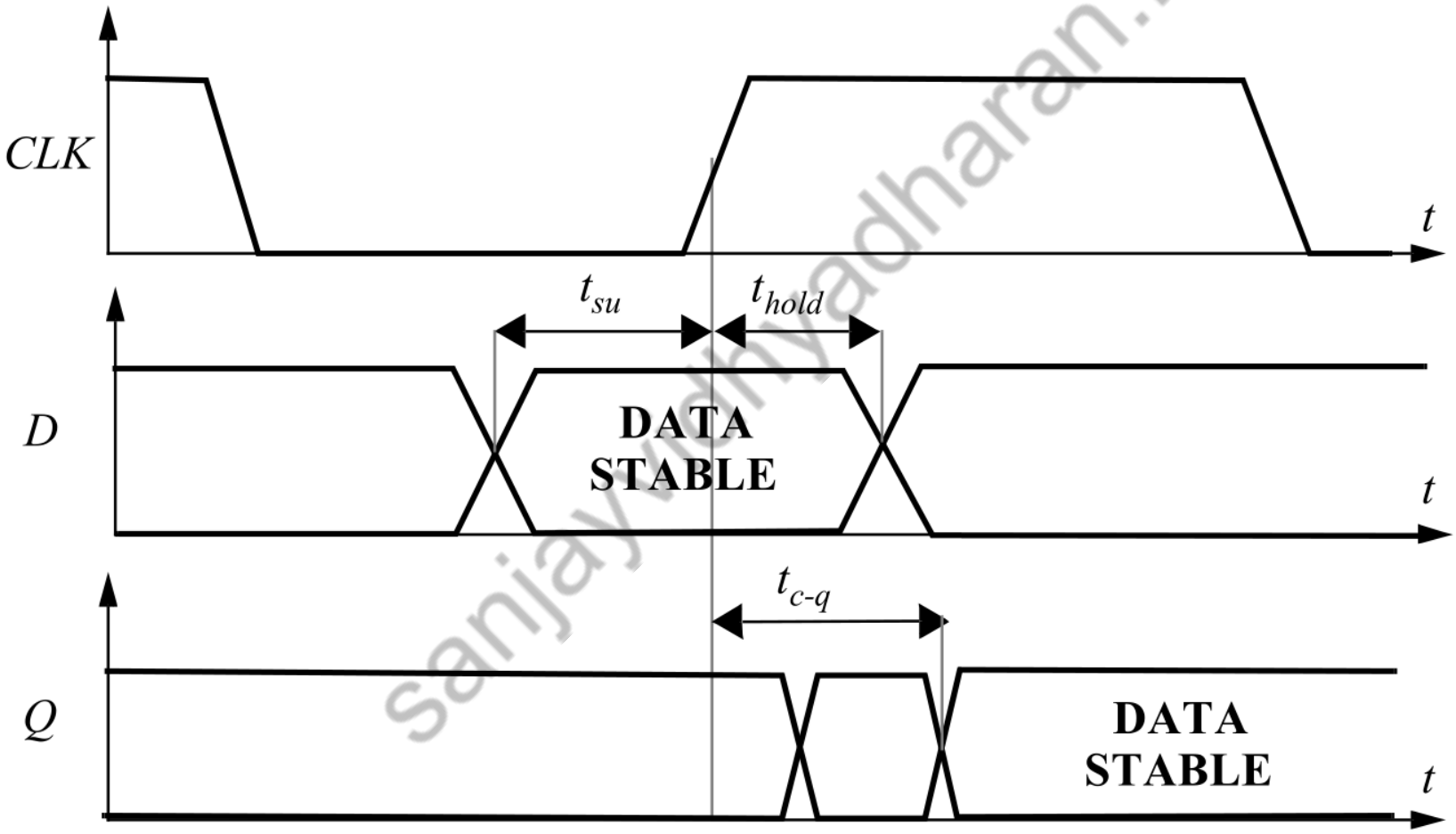


The key to the proper operation of a flip-flop is to trigger it only during signal transition.



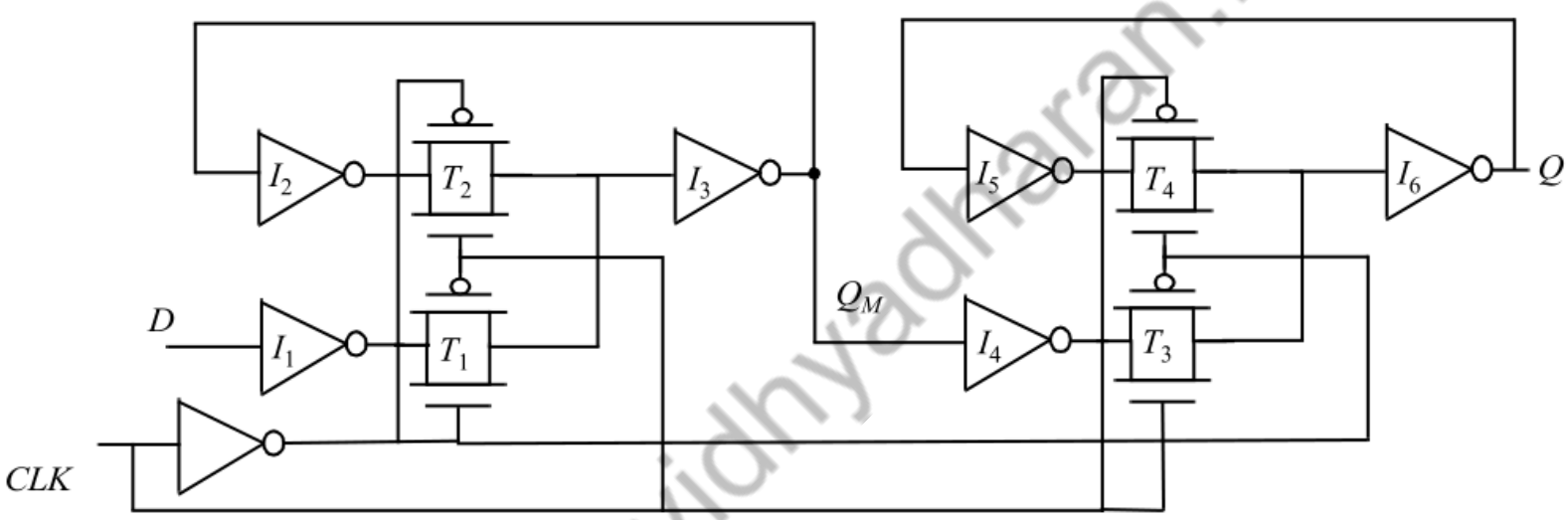
Timing Constraints of a Flip-flop

- Setup Time
- Hold Time



Flip-Flop

Master-slave positive edge-triggered register using multiplexers.



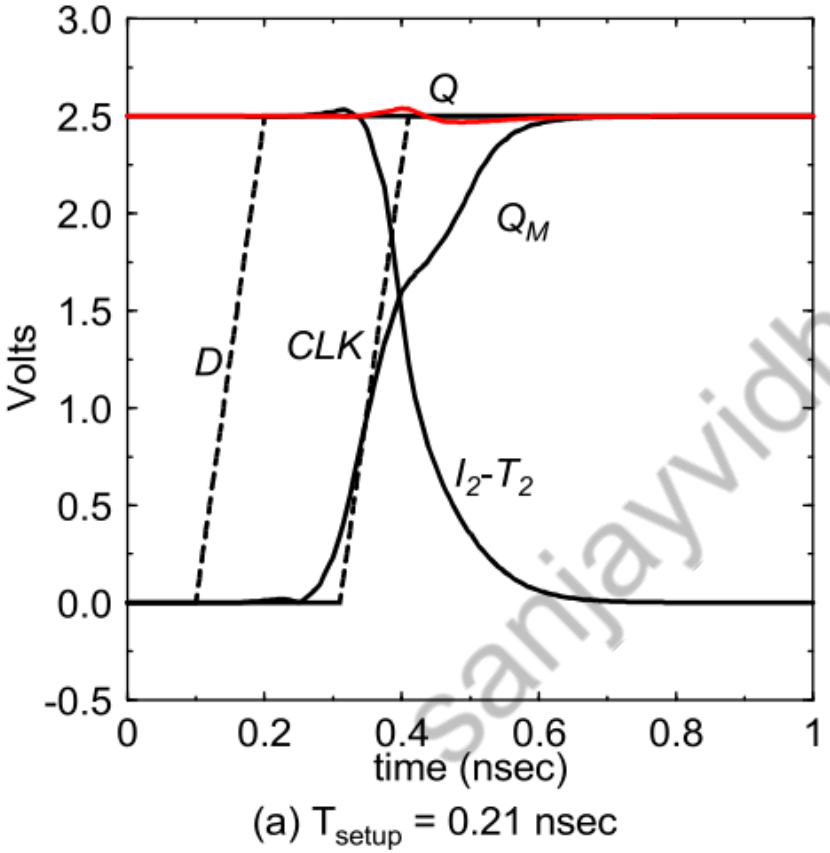
The set-up time is equal to $3*t_{pd\_inv} + t_{pd\_tx}$

Hold time is Nil

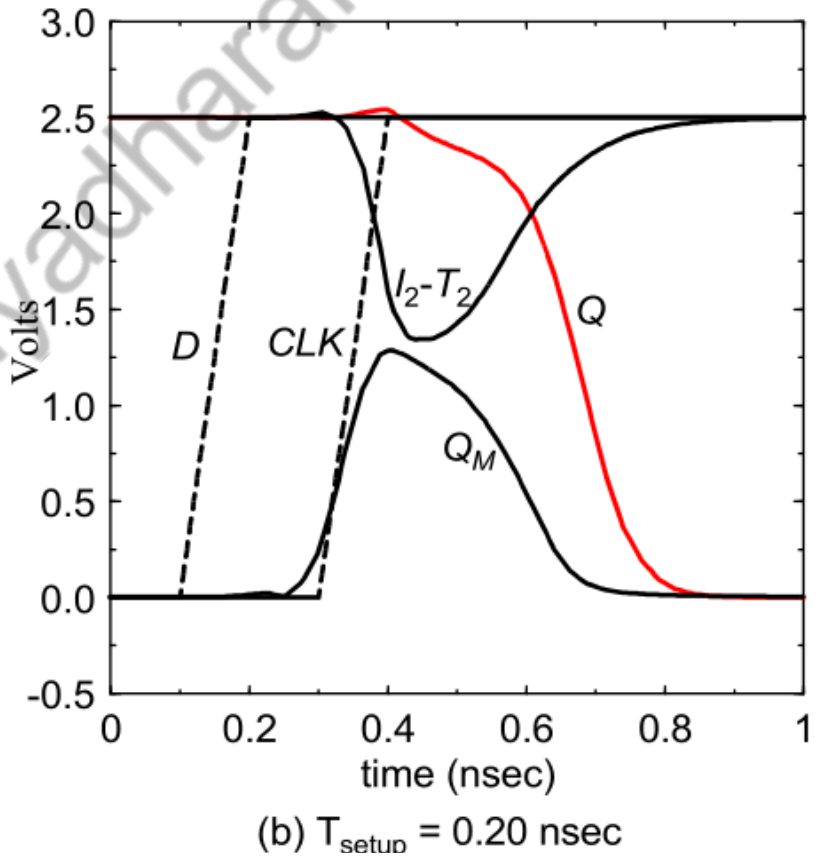
Propagation delay = $t_{pd\_tx} + t_{pd\_inv}$

Flip-Flop

Set-up time simulation



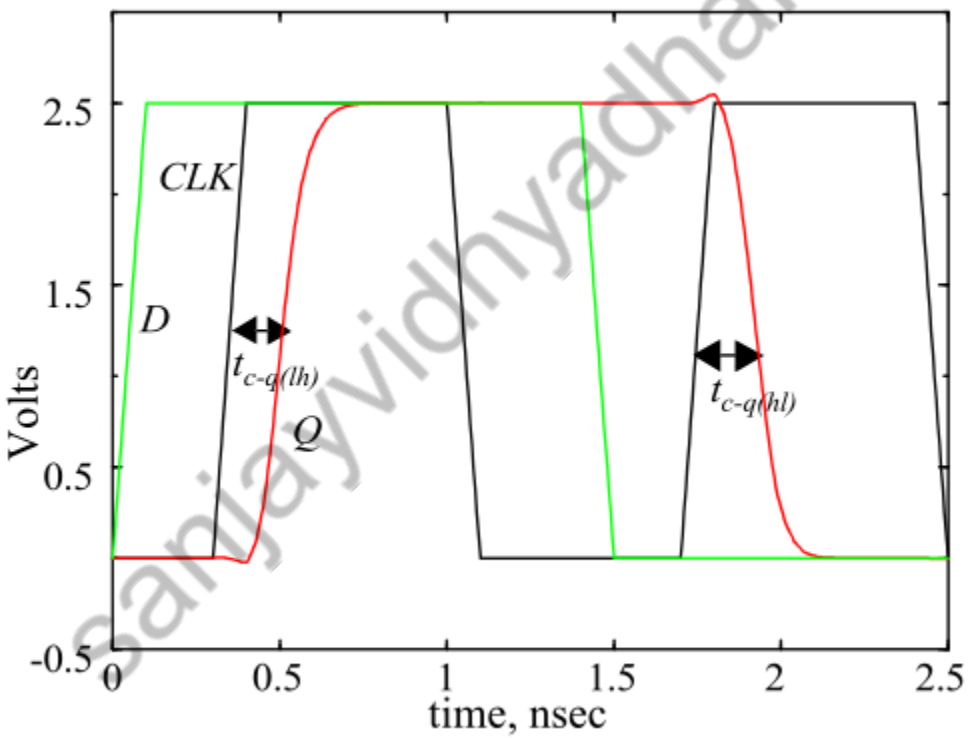
(a) T_{setup} = 0.21 nsec



(b) T_{setup} = 0.20 nsec

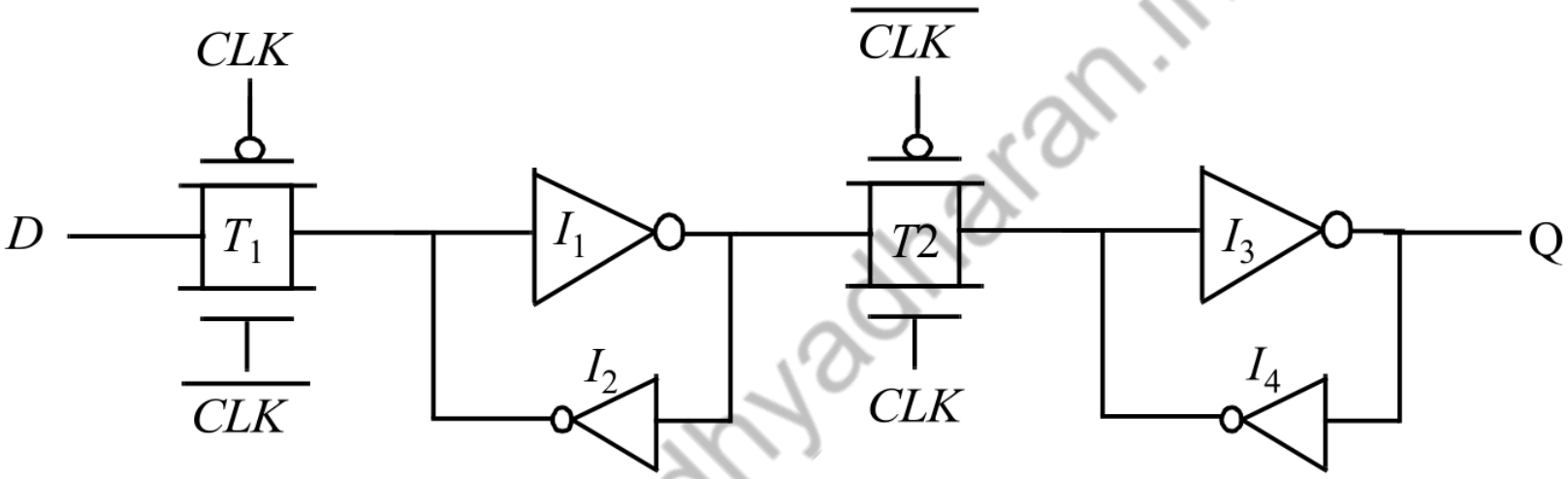
Flip-Flop

Simulation of propagation delay



Flip-Flop

Reduced load clock load static master-slave register.

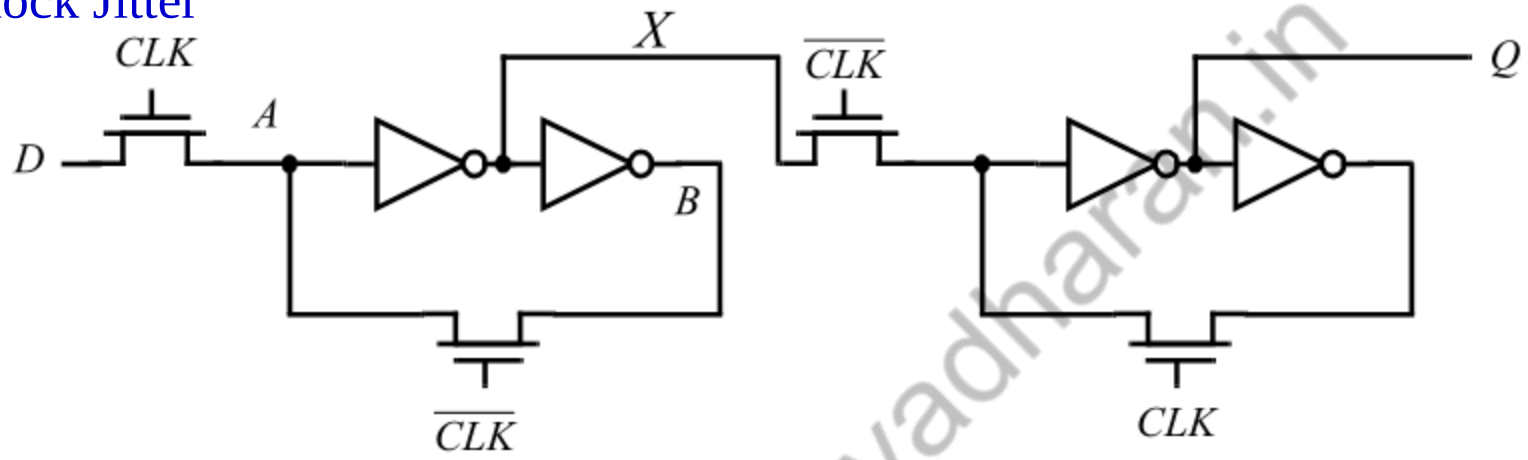


The penalty for the reduced clock load is increased design complexity. The transmission gate (T_1) and its source driver must overpower the feedback inverter (I_2) to switch the state of the cross-coupled inverter.

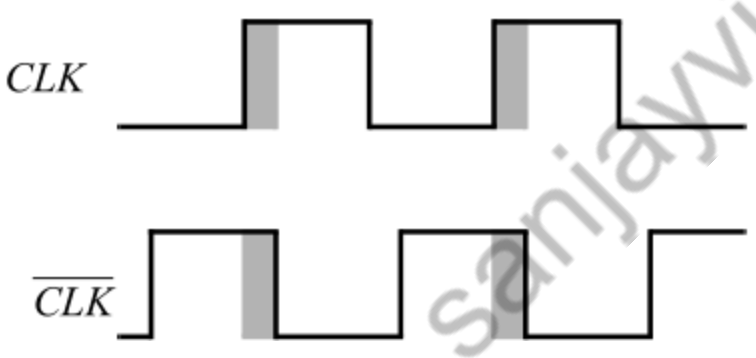
The transistors of inverter I_2 should be made weaker. This can be accomplished by making their channel-lengths larger than minimum.

Flip-Flop

Clock Jitter



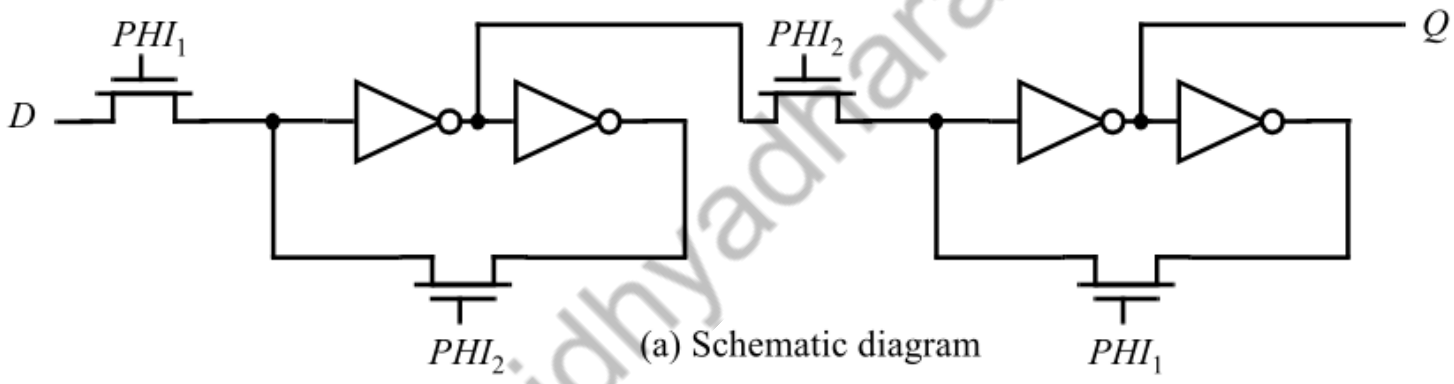
(a) Schematic diagram



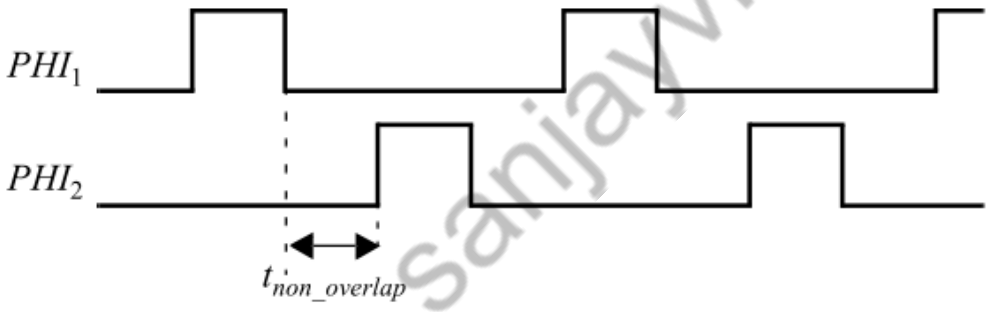
When the clock goes high, the slave stage should stop sampling the master stage output and go into a hold mode. However, since CLK and CLK are both high for a short period of time (the overlap period), both sampling pass transistors conduct and there is a direct path from the D input to the Q output. As a result, data at the output can change on the rising edge of the clock, which is undesired for a negative edge- triggered register.

Flip-Flop

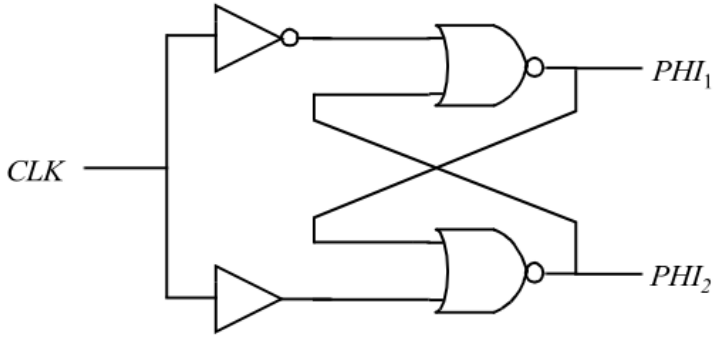
Two-phase non-overlapping clocks



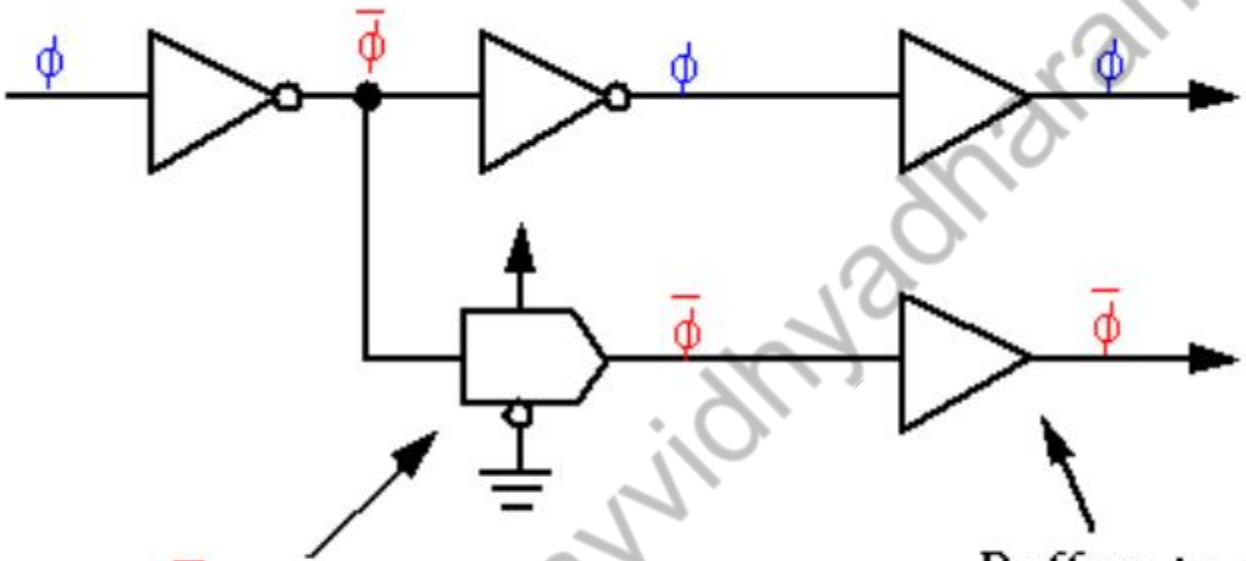
(a) Schematic diagram



(b) Two-phase non-overlapping clocks



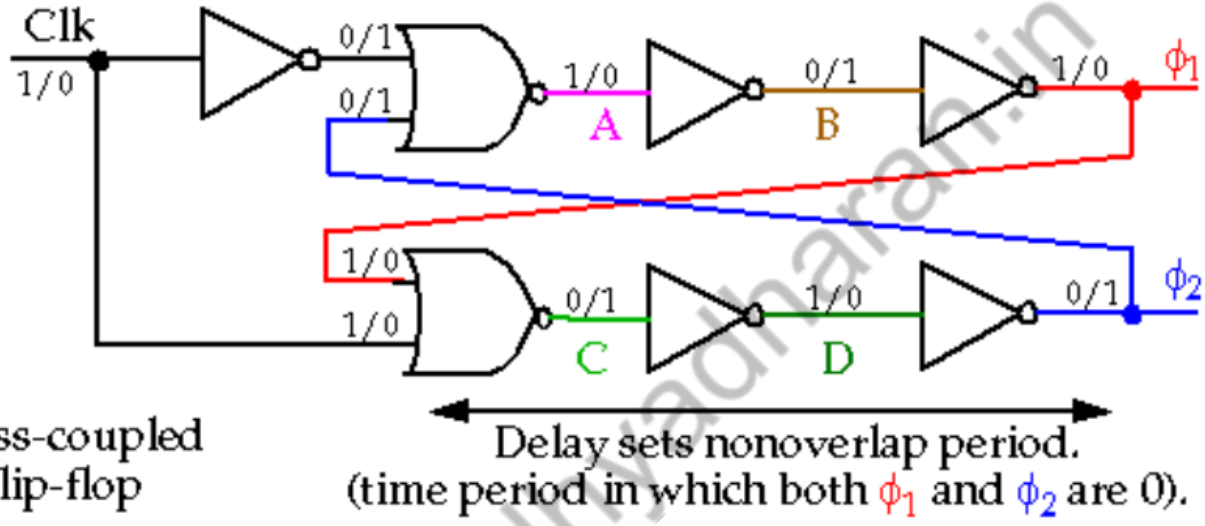
Single Phase Global Clock Generation



Pass $\bar{\phi}$ through a transmission gate as a means of calibrating for ϕ's inverter delay.

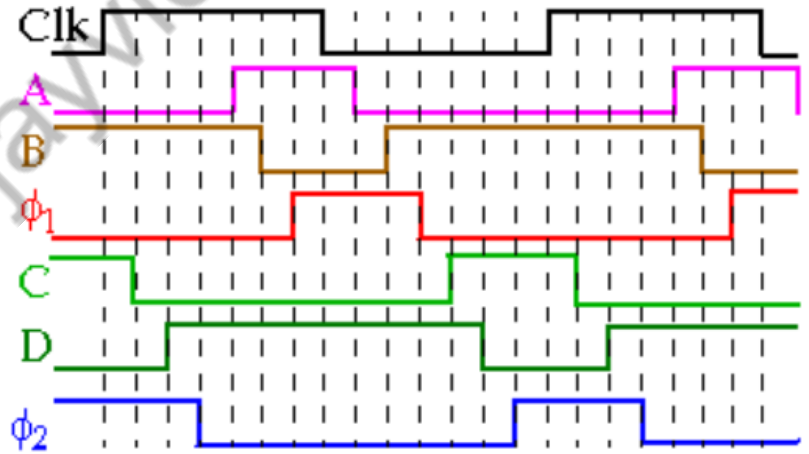
Buffers to drive large loads.

Non-overlapping Clock Generation



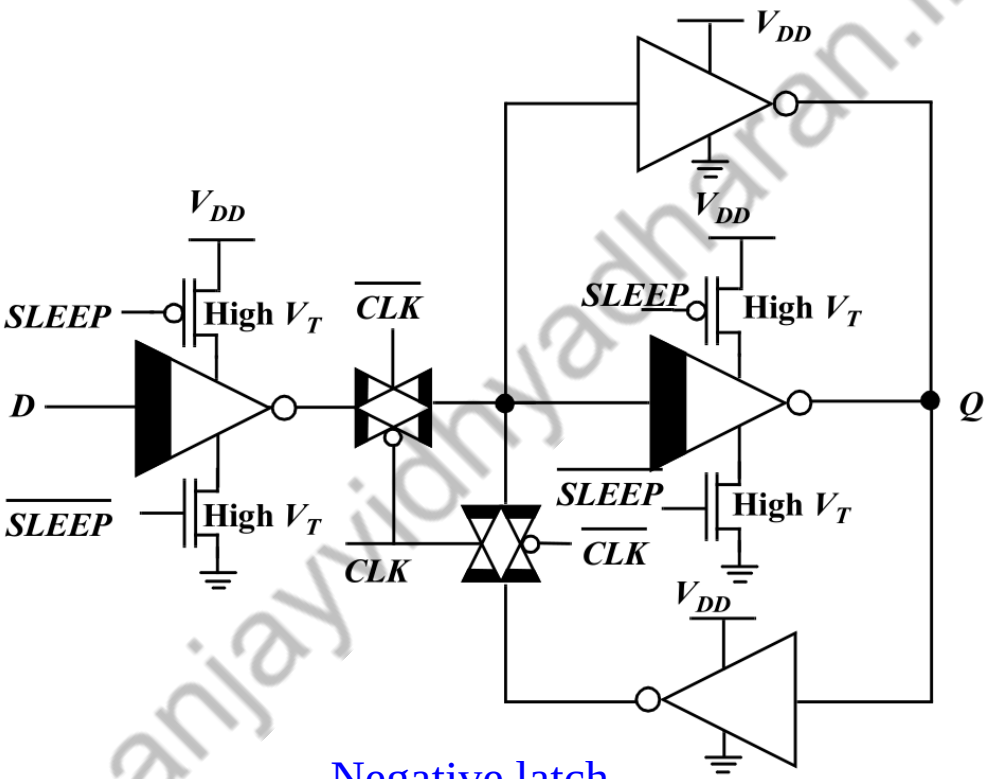
Cross-coupled RS flip-flop

Delay sets nonoverlap period. (time period in which both ϕ_1 and ϕ_2 are 0).



Flip-Flop

Solving the leakage problem using multiple-threshold CMOS.



Negative latch

- During normal mode of operation, the sleep devices are tuned on.
- The shaded inverters and transmission gates are implemented in low-threshold devices.

Thank you