VLSI Design : 2021-22
Lecture 2
Review of MOSFET Operation

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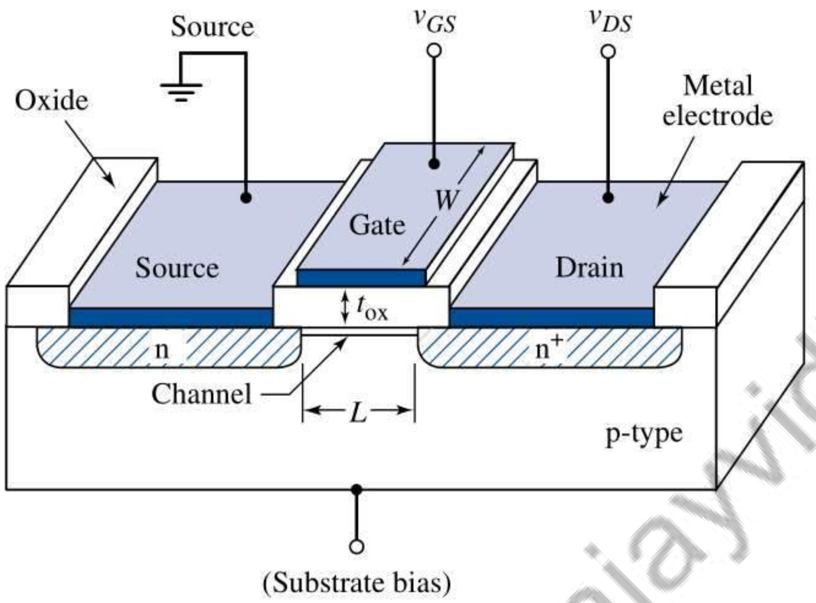
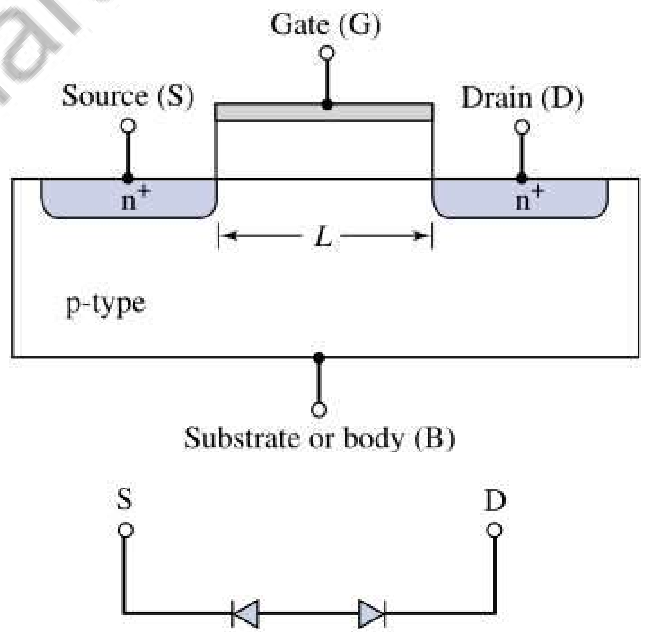
MOSFET Operation

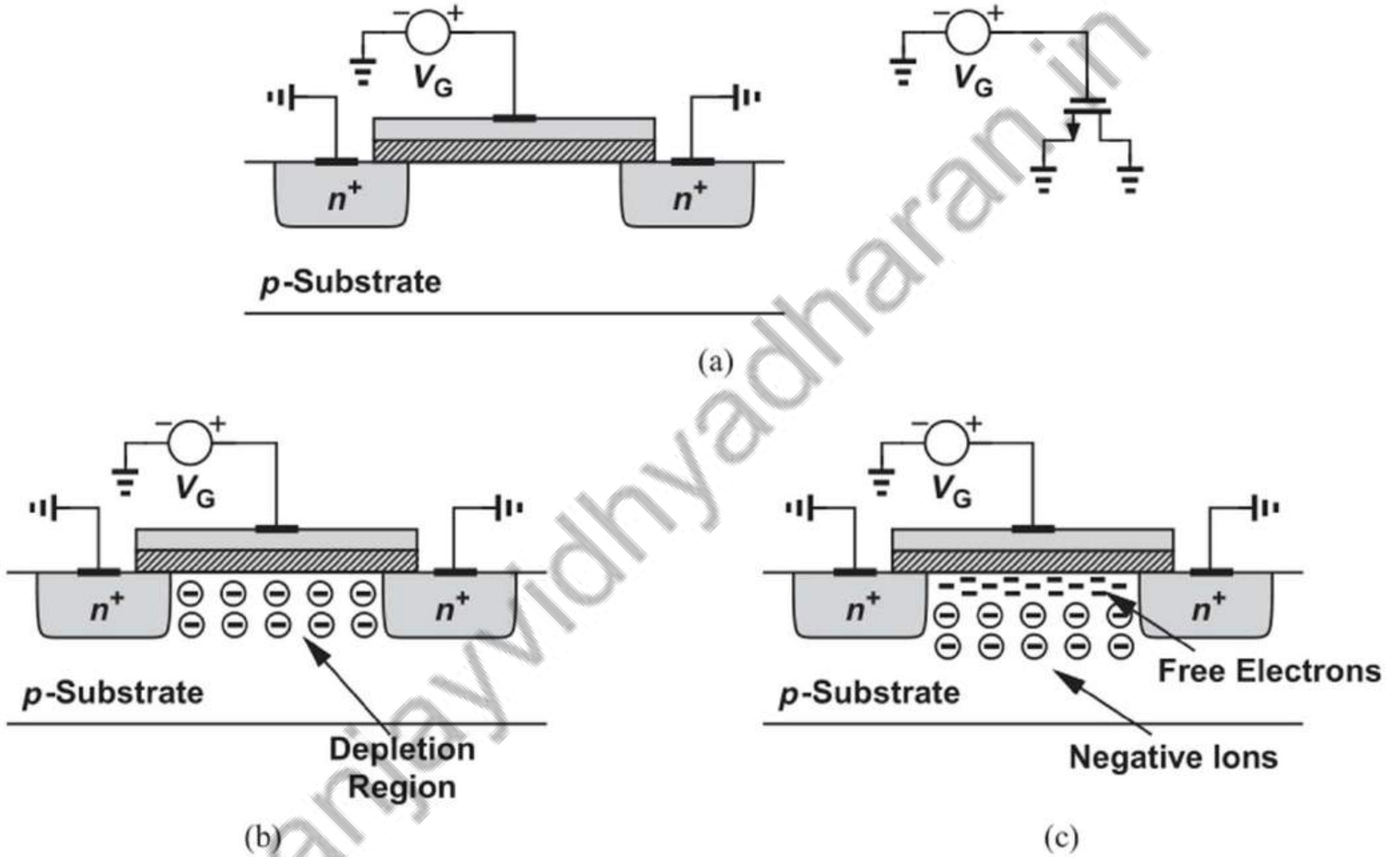
Cut-off Region





$$For\ V_{GS} < V_T \qquad I_D = 0$$

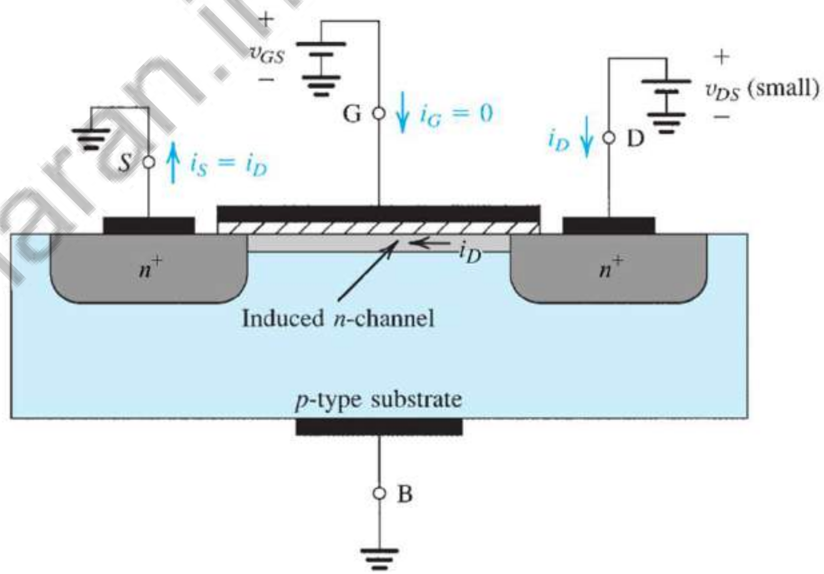
The Threshold Voltage



As a practical definition, The threshold Voltage V_T is that gate voltage when the surface is said to be inverted, i.e. the density of mobile electrons on the surface becomes equal to the density of holes in the bulk (p-type) substrate.

The Threshold Voltage

$$V_{T0} = \Phi_{GC} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}$$



1. The work function difference TGC between the gate and the channel reflects the built-in potential of the MOS system, which consists of the p-type substrate, the thin silicon dioxide layer, and the gate electrode. Depending on the gate material, the work function difference is

$$\emptyset_{GC} = \emptyset_{F\_Substrate} - \emptyset_{F_{metal}} \quad \textit{For Matral Gate}$$

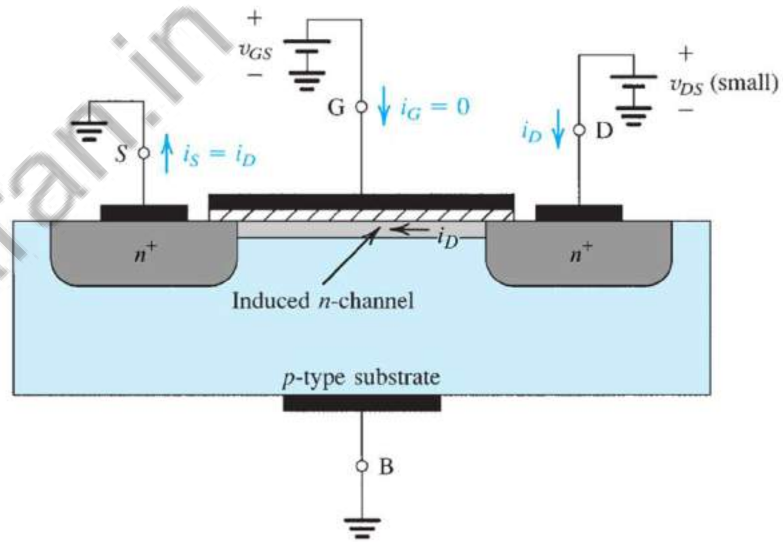
$$\emptyset_{GC} = \emptyset_{F\_Substrate} - \emptyset_{F_{Polysilicon}} \quad \textit{ForPolysilicon Gate}$$

2. The externally applied gate voltage must be changed to achieve surface inversion, i.e., to change the surface potential by - 2 $\emptyset_F$. This will be the second component of the threshold voltage.

$$\phi_{Fp} = \frac{kT}{q} \ln \frac{n_i}{N_A}$$

The Threshold Voltage

$$V_{T0} = \Phi_{GC} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}$$

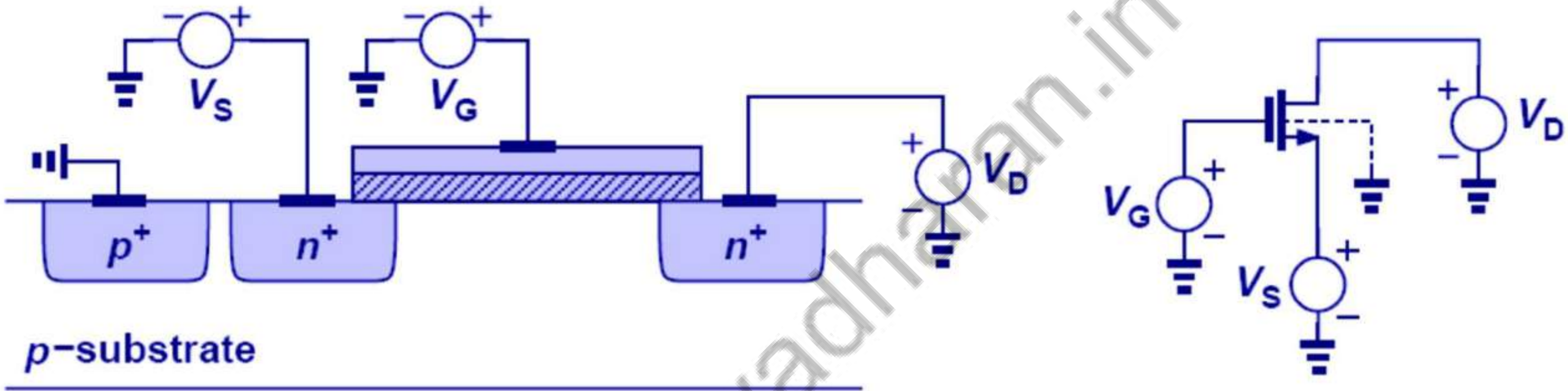


3. Another component of the applied gate voltage is necessary to offset the depletion region charge, which is due to the fixed acceptor ions located in the depletion region near the surface.

$$Q_{B0} = -\sqrt{2q \cdot N_A \cdot \varepsilon_{Si} \cdot |-2\phi_F|}$$

4. There always exists a fixed positive charge density Q_{ox} at the interface between the gate oxide and the silicon substrate, due to impurities and/or lattice imperfections at the interface. The gate voltage component that is necessary to offset this positive charge at the interface is - Q_{OX}/C_{ox}.

The Threshold Voltage

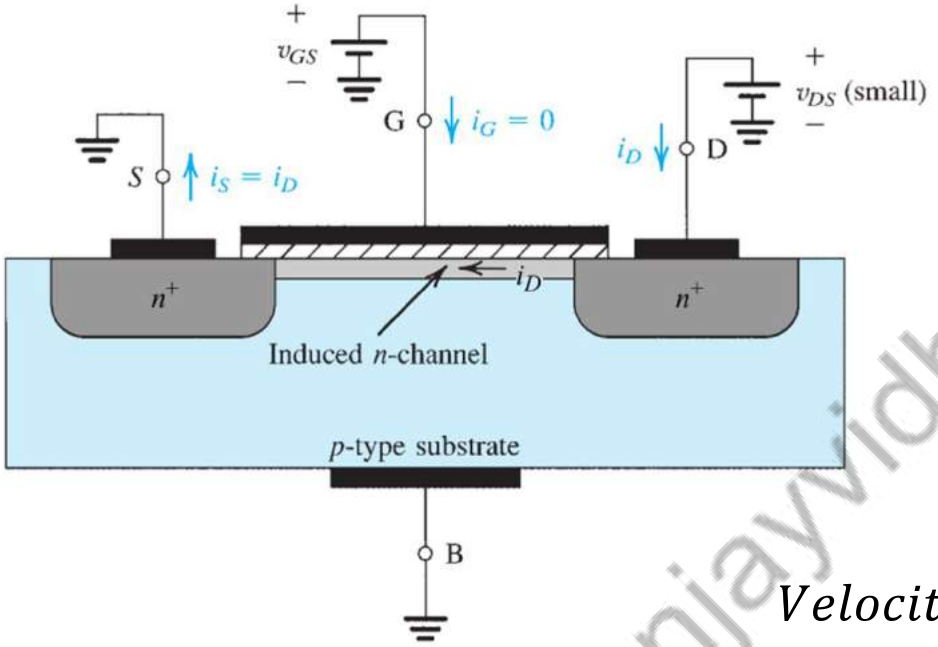


$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{|2\phi_F| + V_{SB}} - \sqrt{|2\phi_F|}\right)$$

The **body effect** occurs in a MOSFET when the source is not tied to the substrate (which is always connected to the most negative power supply in the integrated circuit for n-channel devices and to the most positive for p-channel devices). The substrate then acts as a "second gate" or a back-gate for the MOSFET

MOSFET Current

Linear Region- Small V_{DS}



$$V_{ov} = V_{GS} - V_T$$

$$C_{ox}WL = \frac{Q}{V_{ov}}$$

$$Charge\ per\ unit\ Length = \frac{Q}{L} = C_{ox}WV_{ov}$$

$$Electric\ Field\ in\ Channel = \frac{V_{DS}}{L}$$

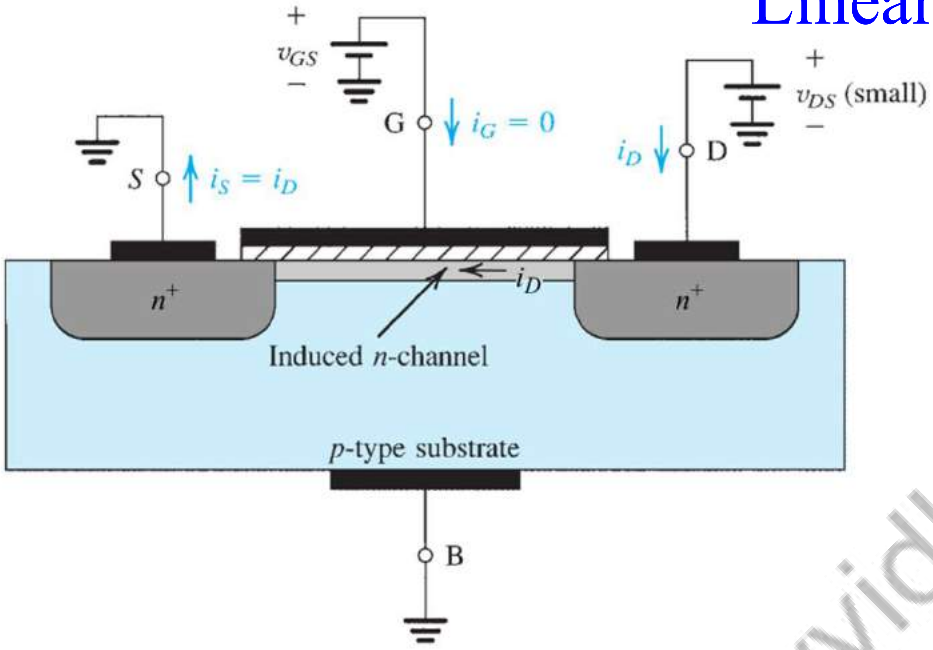
$$Velocity\ of\ Charge\ in\ Channel(v) = \mu_n E = \frac{V_{DS}\mu_n}{L}$$

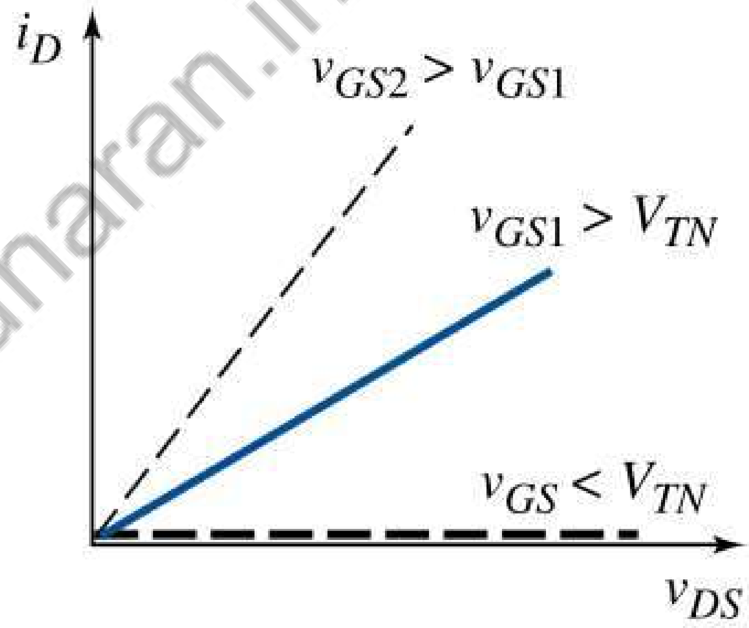
$$Current\ in\ Channel\ \ (I_D) = v * \frac{Q}{L} = \frac{V_{DS}\mu_n}{L} * C_{ox}WV_{ov}$$

$$I_D = \frac{\mu_n C_{ox} W (V_{GS} - V_T) V_{DS}}{L}$$

MOSFET Current

Linear Region- Small V_{DS}





V_{ov}

$$I_D = \frac{\mu_n C_{ox} W (V_{GS} - V_T) V_{DS}}{L}$$

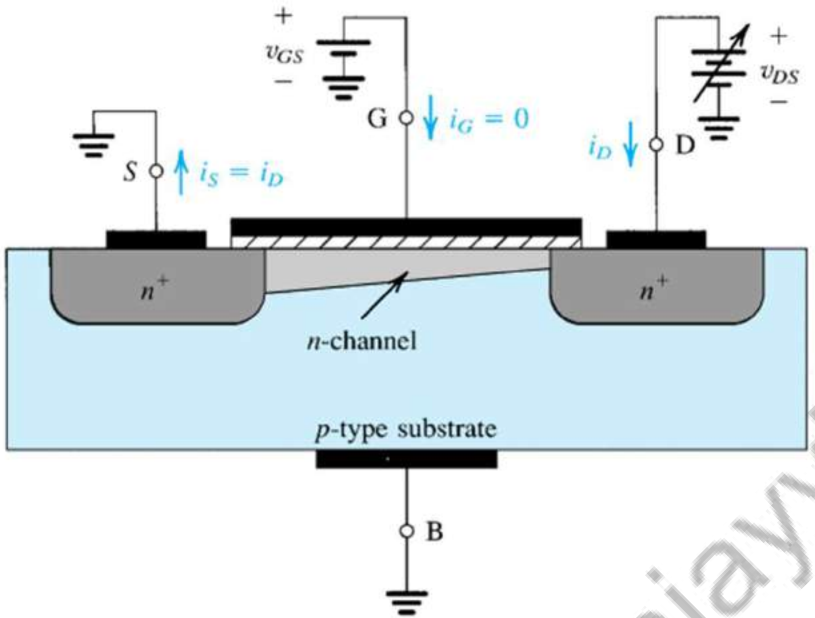
$$Transconductance\ of\ Channel\ g_{DS} = \frac{\mu_n C_{ox} W V_{ov}}{L}$$

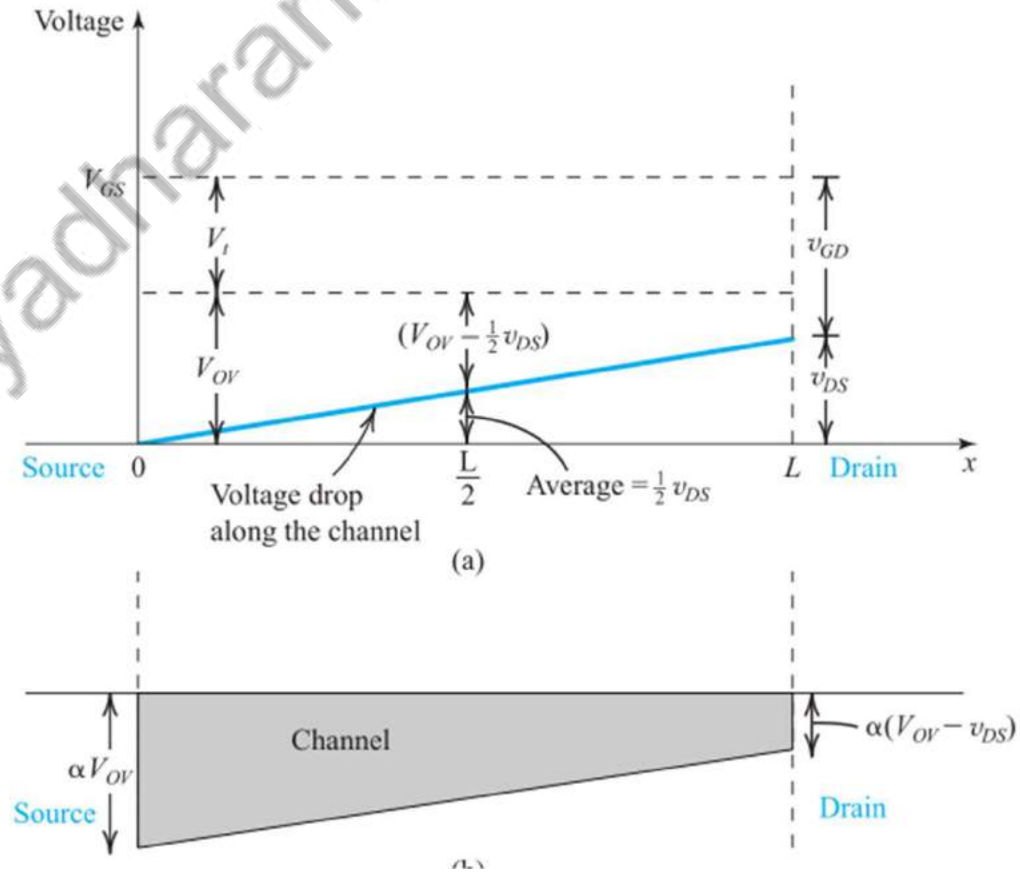
$$Process\ transconductance\ parameter\ k'_n = \mu_n C_{ox}$$

$$I_D = \frac{k'_n W V_{ov} V_{DS}}{L}$$

MOSFET Current

Linear Region as V_{DS} is Increased



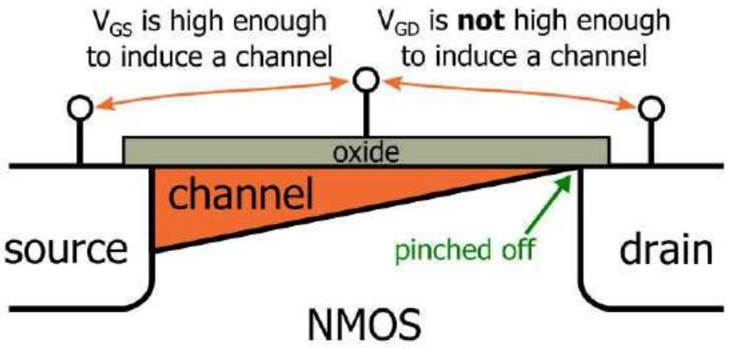


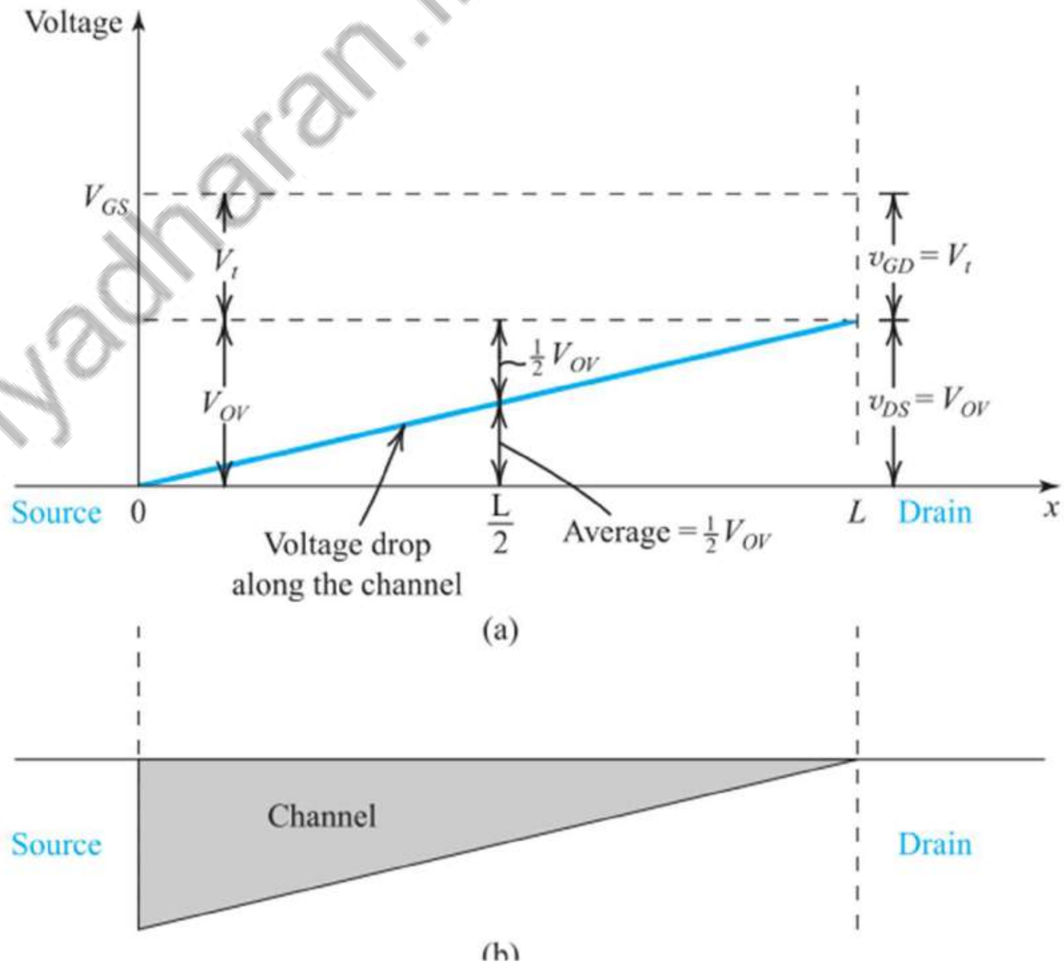
Charge in the tapered channel is proportional to the channel cross-sectional area

$$I_D = \frac{k_n' W (V_{ov} - \frac{V_{DS}}{2}) V_{DS}}{L}$$

MOSFET Current

Saturation Region



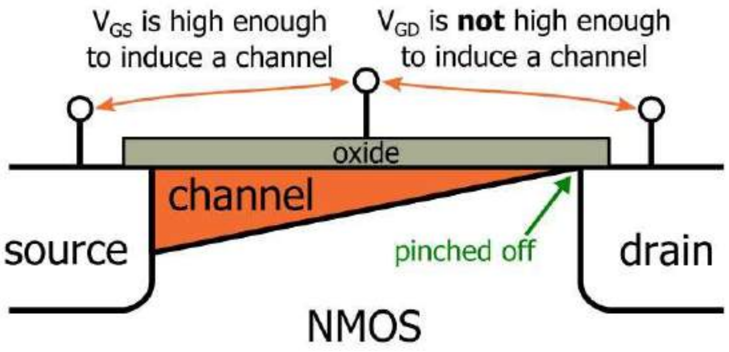


$$V_{DS} = V_{ov} = V_{GS} - V_T$$

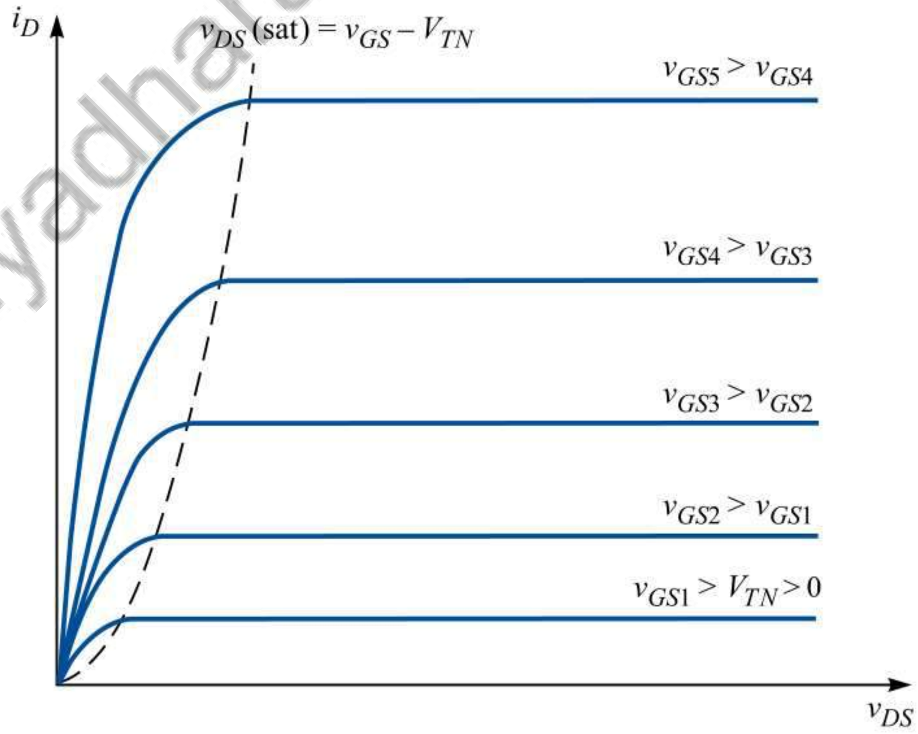
$$I_D = \frac{k_n' W (V_{ov} - \frac{V_{DS}}{2}) V_{DS}}{L}$$

$$I_D = \frac{k_n' W (V_{GS} - V_T)^2}{2L}$$

MOSFET Current



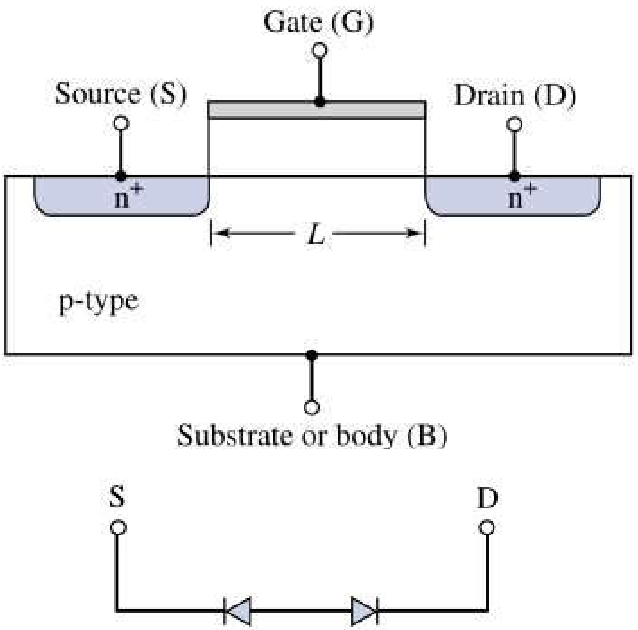
$$I_D = \frac{k_n' W (V_{GS} - V_T)^2}{2L}$$



MOSFET OPERATION AS SWITCH

NMOSFET

Switch OFF



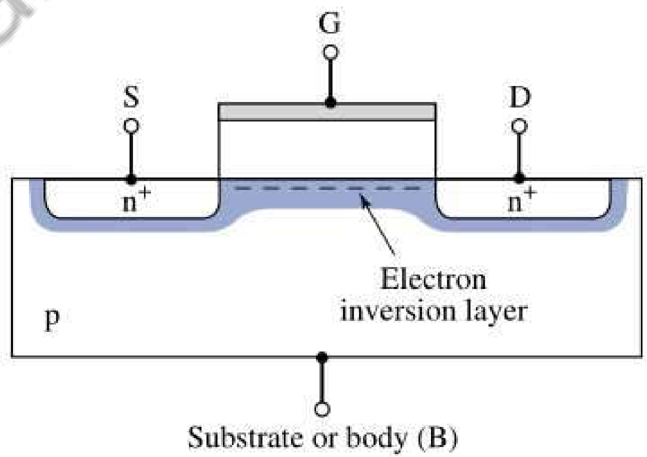
I_{OFF}

Ideal = 0 Practically in pico amperes

R_{OFF}

Ideal = ∞ Practically in Mega/Giga Ohms

Switch ON



I_{ON}

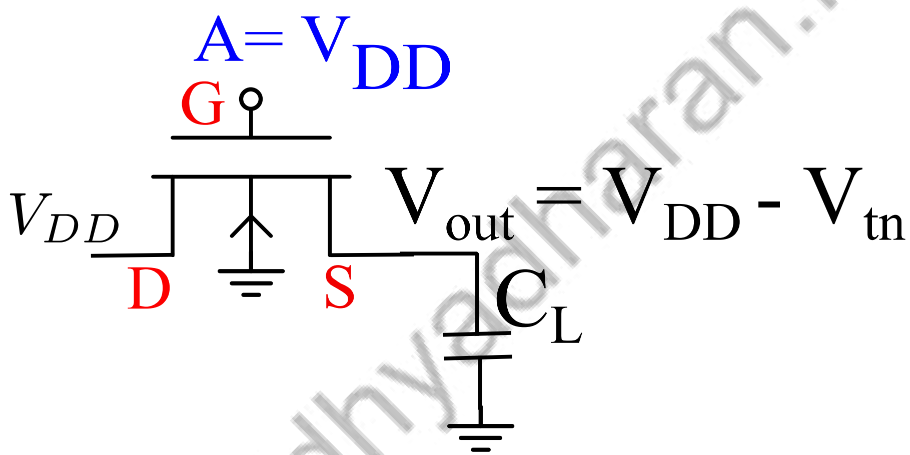
Ideal = ∞ Practically in micro amperes

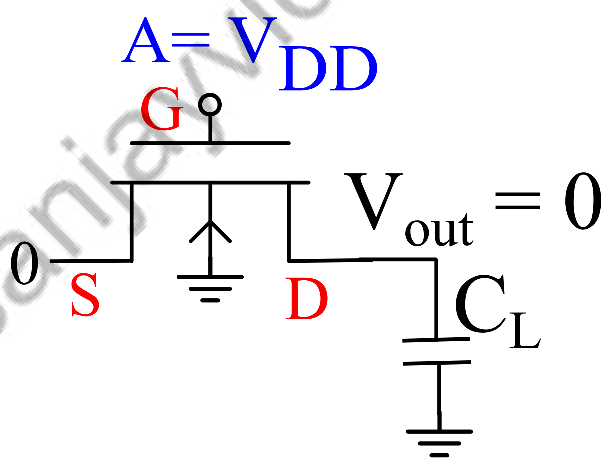
R_{ON}

Ideal = 0 Practically in few Ohms

MOSFET OPERATION AS SWITCH

NMOSFET AS SWITCH



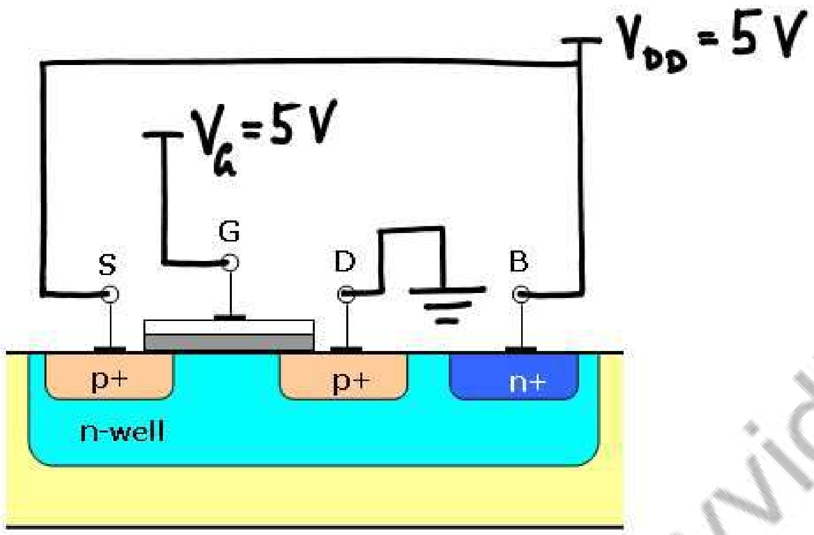


- NMOS can pass perfect 0 but not 1

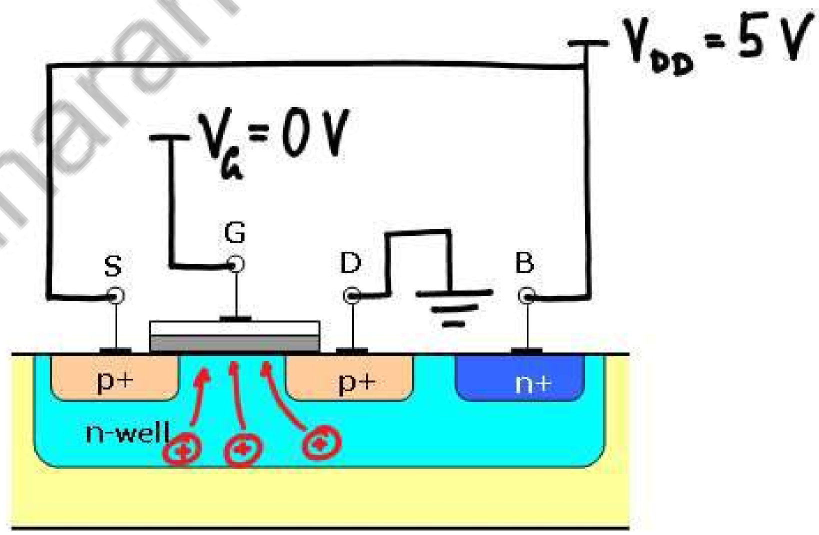
MOSFET OPERATION AS SWITCH

PMOSFET

Switch OFF



Switch ON



I_{OFF}

Ideal = 0 Practically in pico amperes

R_{OFF}

Ideal = ∞ Practically in Mega Ohms

I_{ON}

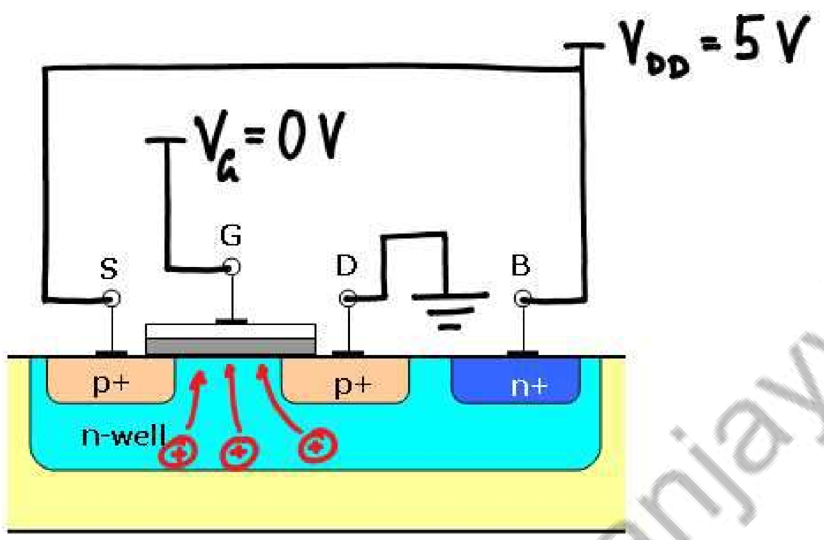
Ideal = ∞ Practically in micro amperes

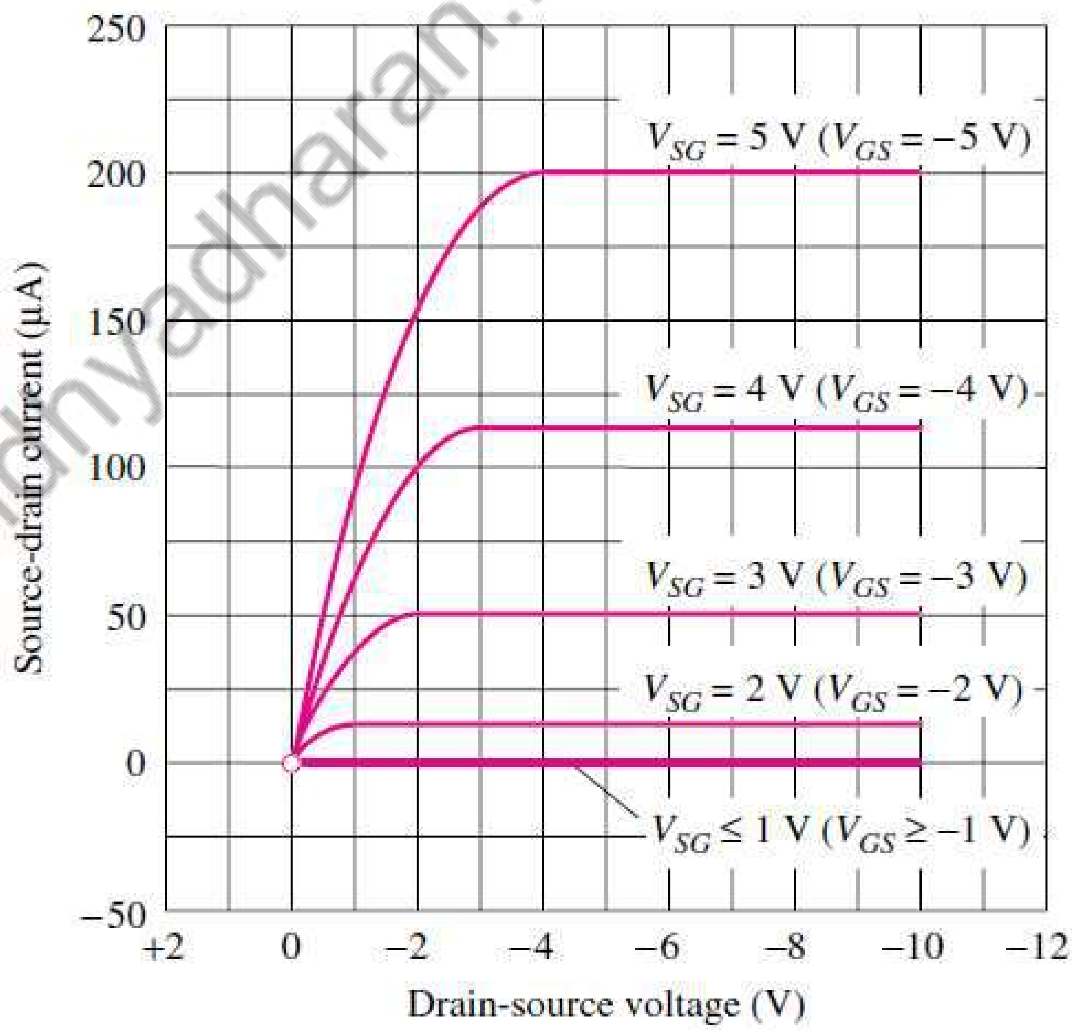
R_{ON}

Ideal = 0 Practically in few Ohms

MOSFET OPERATION

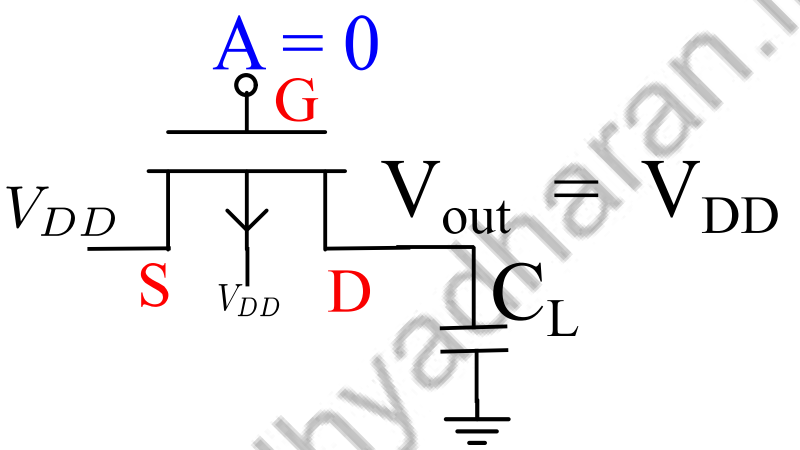
PMOSFET

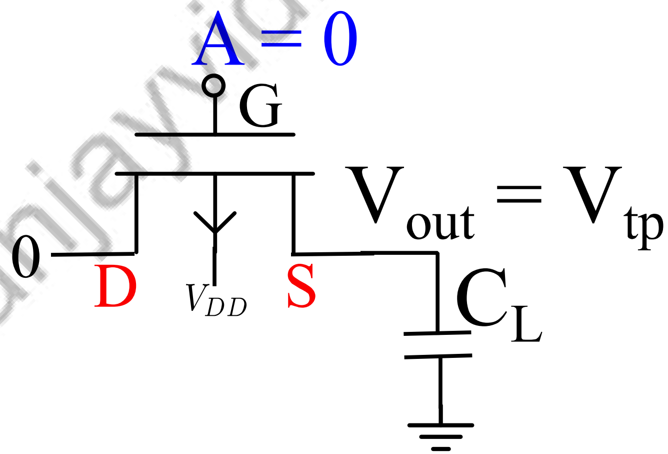




MOSFET OPERATION AS SWITCH

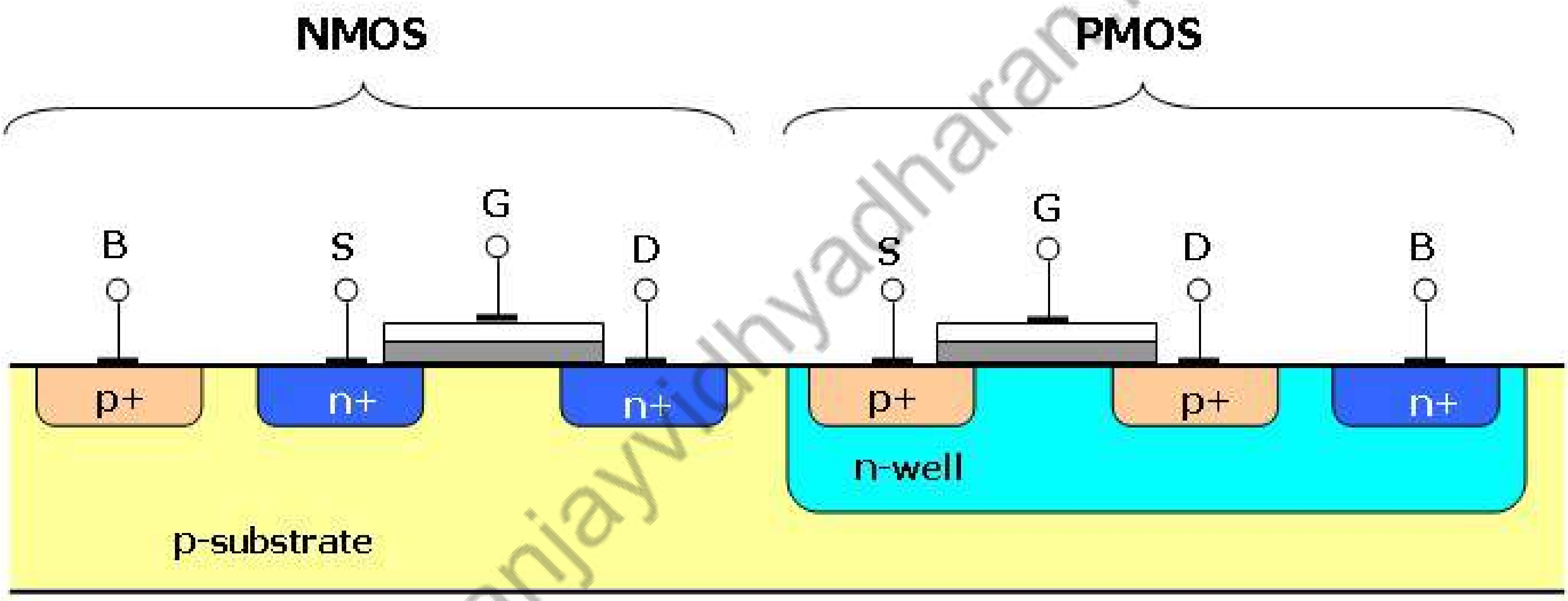
PMOSFET AS SWITCH



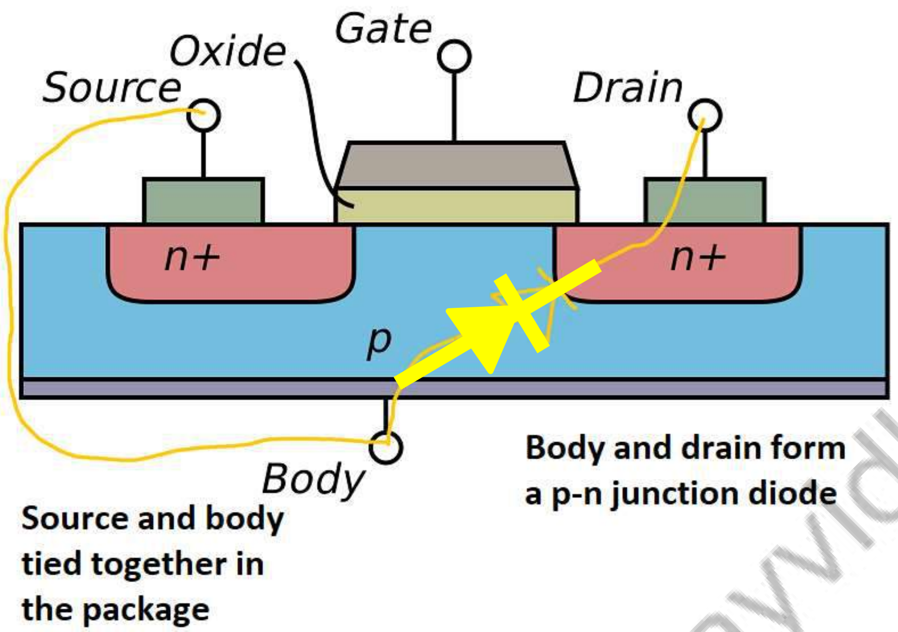


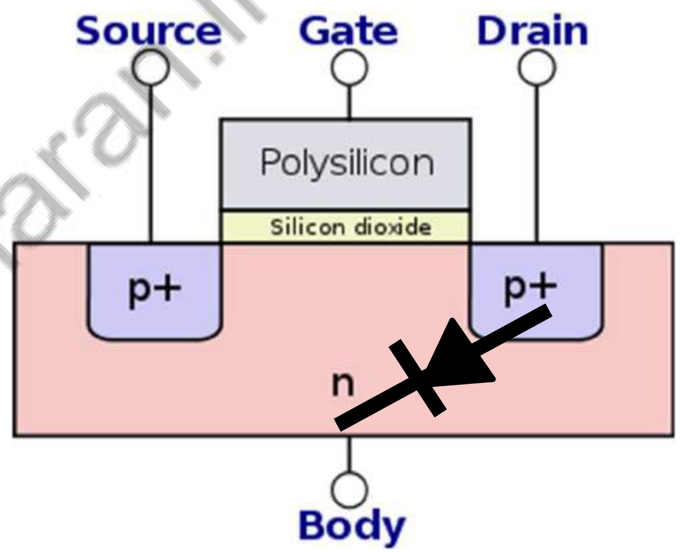
- PMOS pass perfect 1 but not 0

MOSFET OPERATION AS SWITCH



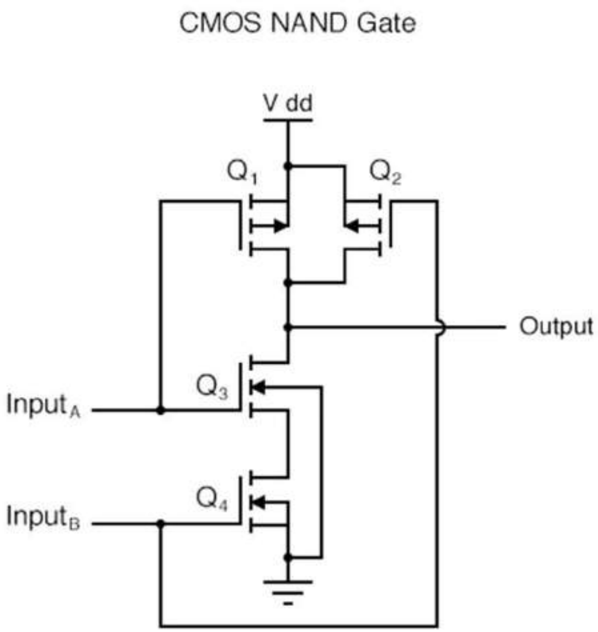
MOSFET BODY CONNECTION

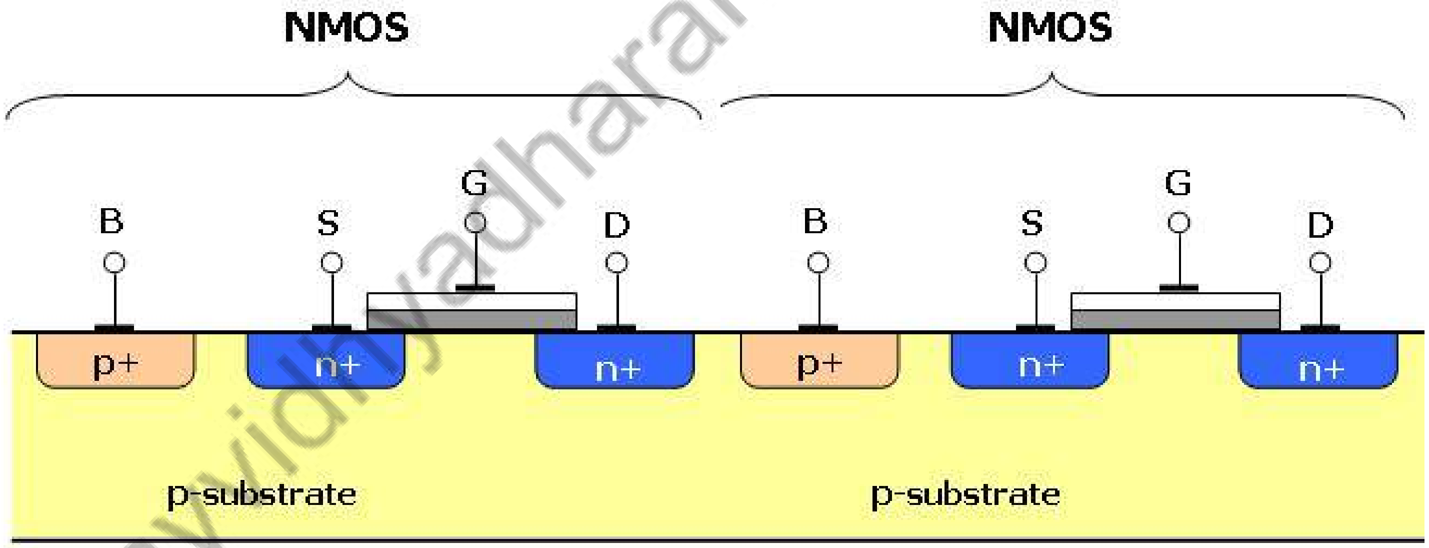




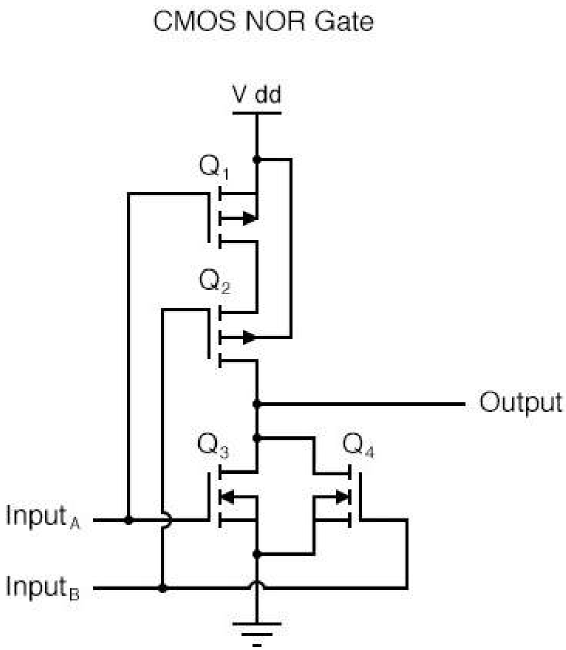
- NMOS Body to Lowest Possible Potential (Gnd)
- PMOS Body to Highest Possible Potential (V_{DD})

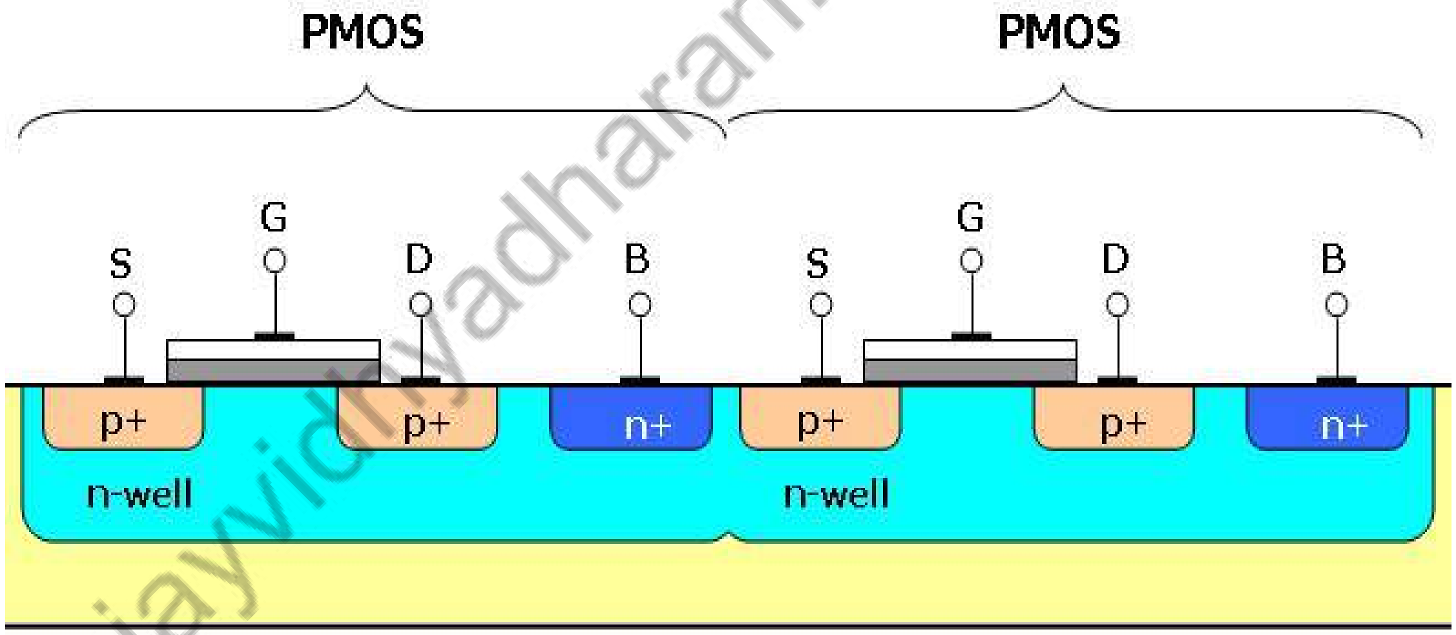
MOSFET BODY CONNECTION



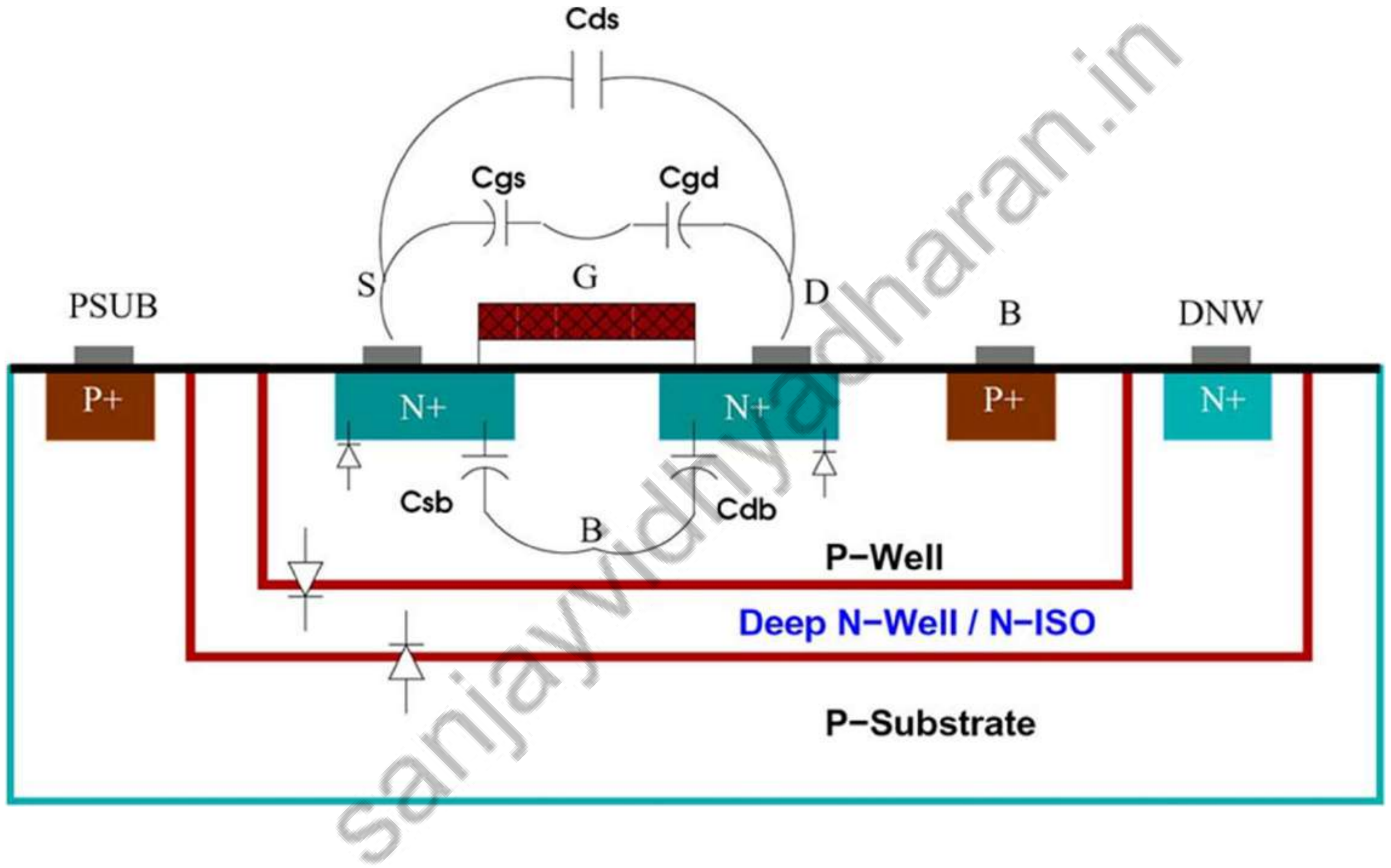


MOSFET BODY CONNECTION



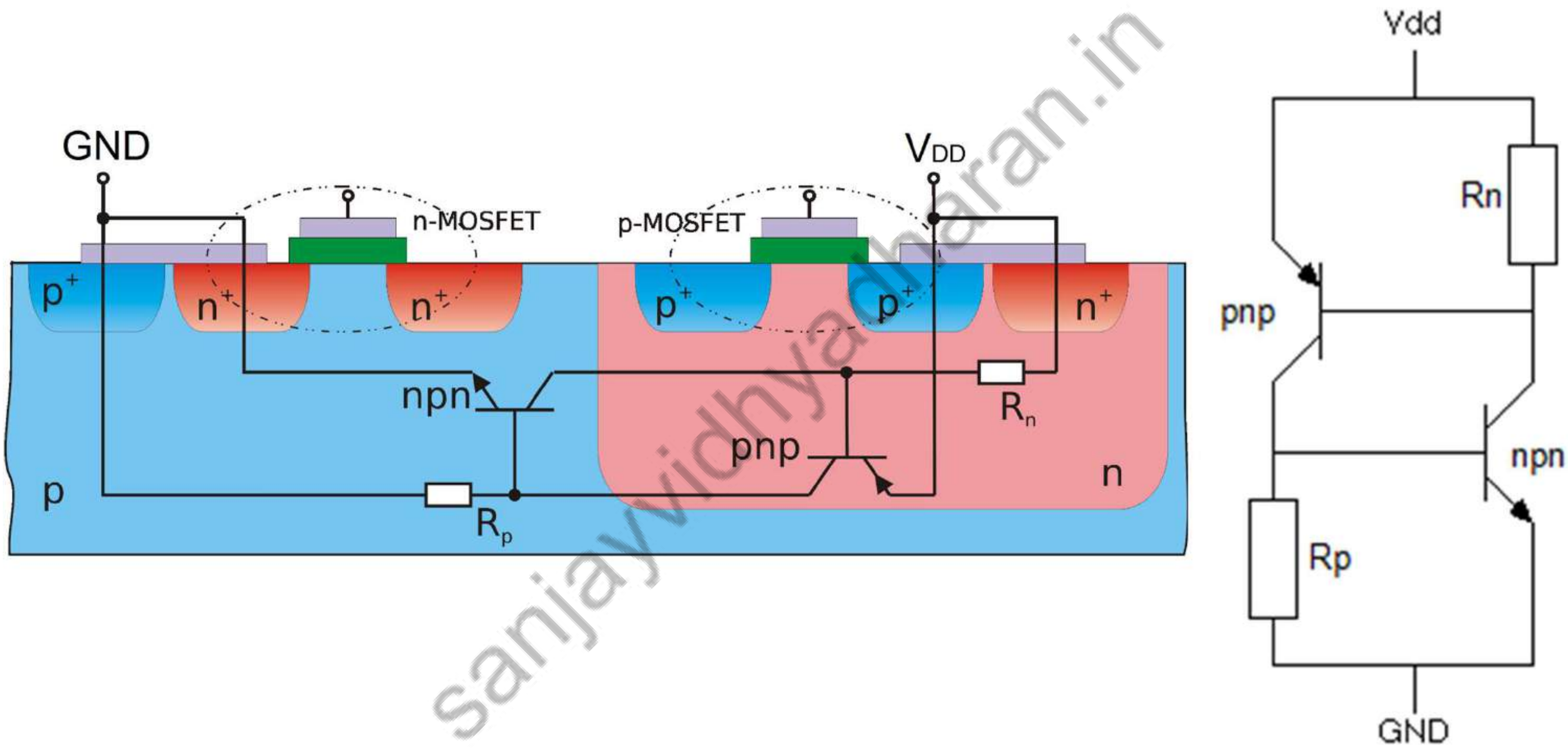


MOSFET BODY CONNECTION



- NMOS Double well : Body not same as Substrate

MOSFET LATCH



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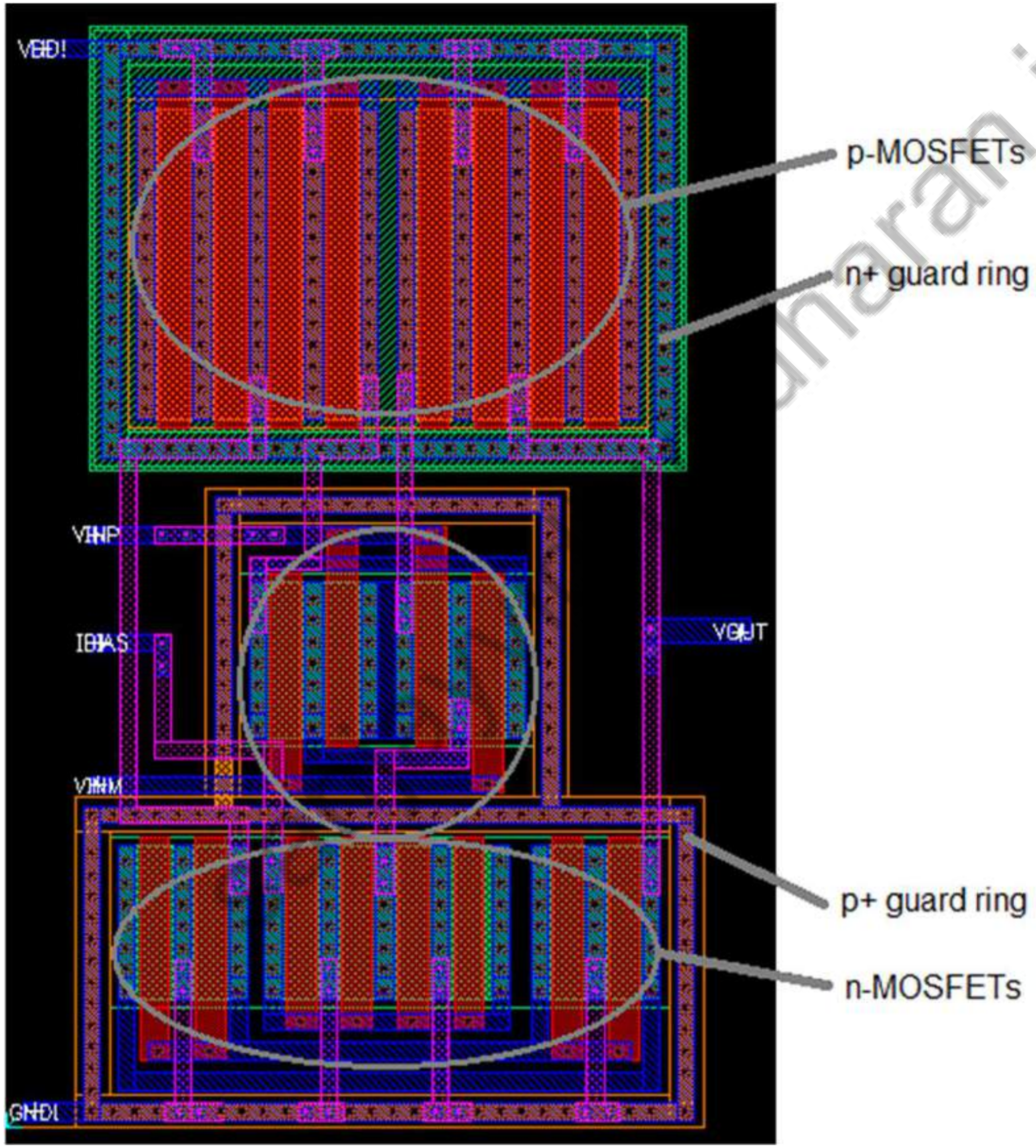

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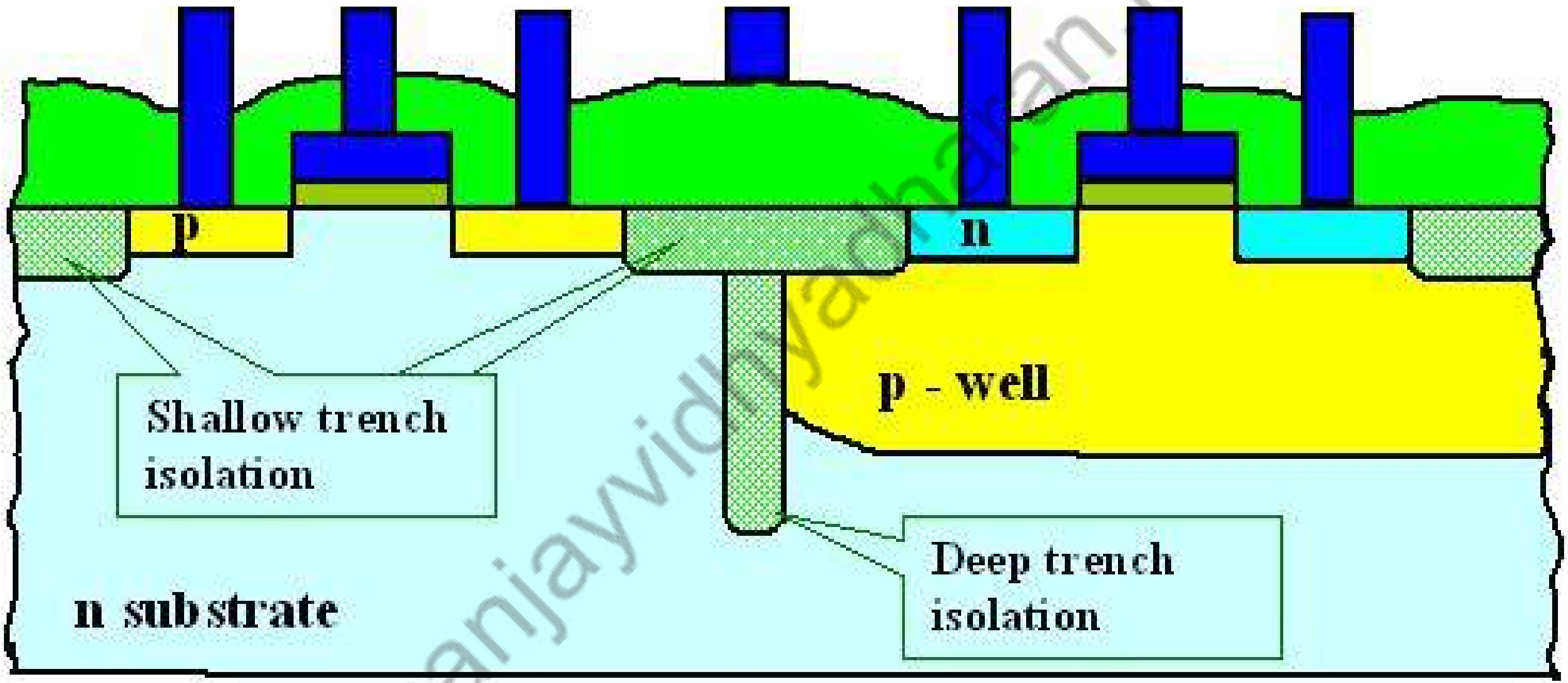

Thank you