VLSI Design / Advanced VLSI Design: 2021-22
Lecture 1
Introduction to VLSI Design

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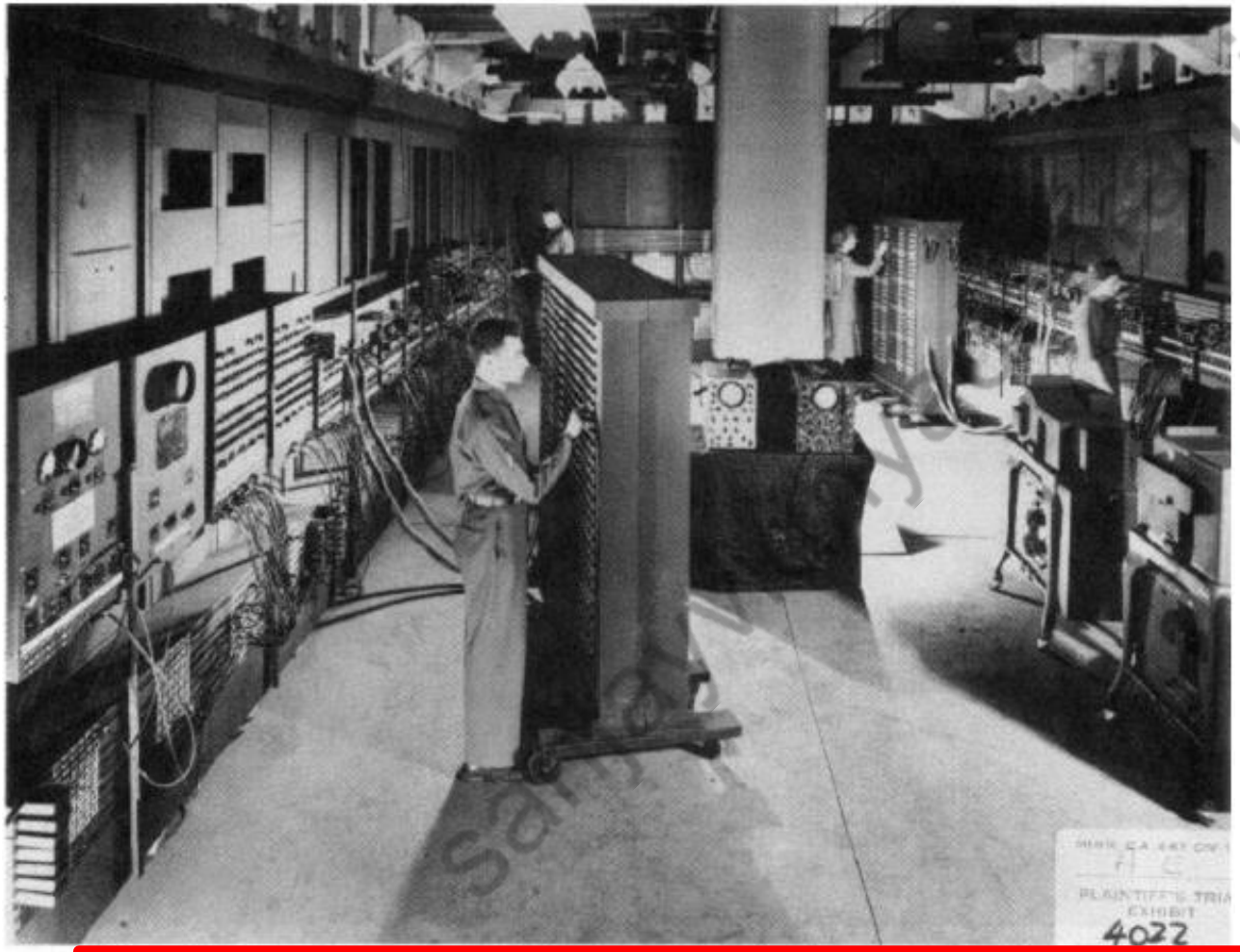
VLSI Design

Integrated circuits are also categorized according to the number of transistors or other active circuit devices they contain.

- An IC is said to use small-scale integration (SSI) if it contains fewer than 10 transistors.
- An IC that contains from 10 to 100 transistors is said to use medium-scale integration.
- A large-scale integration (LSI) IC contains from 100 to 1,000 transistors
- **And one that uses Very-Large-Scale Integration (VLSI) contains more than 1,000 transistors.**

ENAIC - The First Electronic Computer



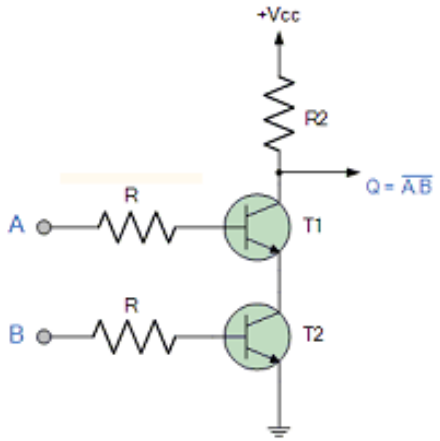
1945

17,468 vacuum tubes and consumed 160 kW

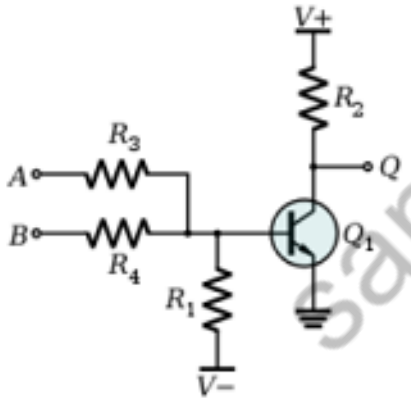
Evolution of Digital Technology

- Resistor Transistor Logic : 1961
- Diode Transistor Logic : 1962
- Transistor Transistor Logic : 1963 Discrete IC
- Emitter-coupled Logic : First Microprocessor 360
- CMOS :
  - 1974 Intel 4004 which had 2000 Transistors Channel Length of 10 µm.
  - 2021 AMD 7 nm has billions of Transistors Channel Length of 7 nm.

RTL Logic



RTL NAND gate



RTL NOR gate

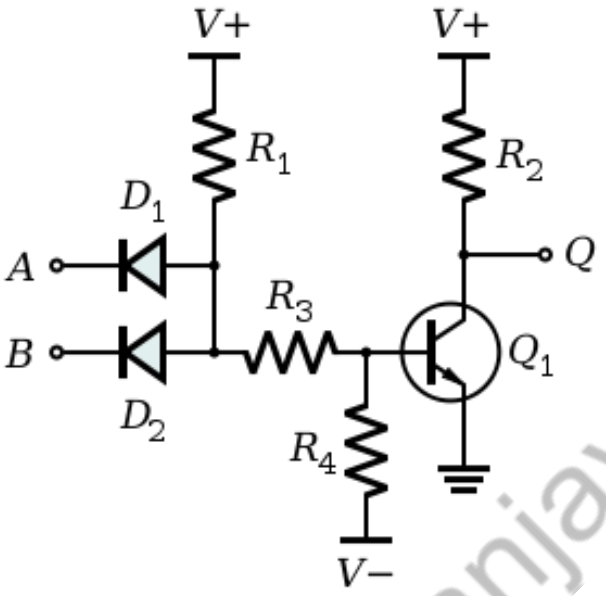
Advantages

- The primary advantage of RTL technology was that it involved a minimum number of transistors, which was an important consideration before integrated circuit technology

Disadvantages

- The obvious disadvantage of RTL is its high current dissipation when the transistor conducts to overdrive the output biasing resistor.
- Passive Pull up.
- Limited Fanout
- No Rail-to-Rail Output

DTL Logic



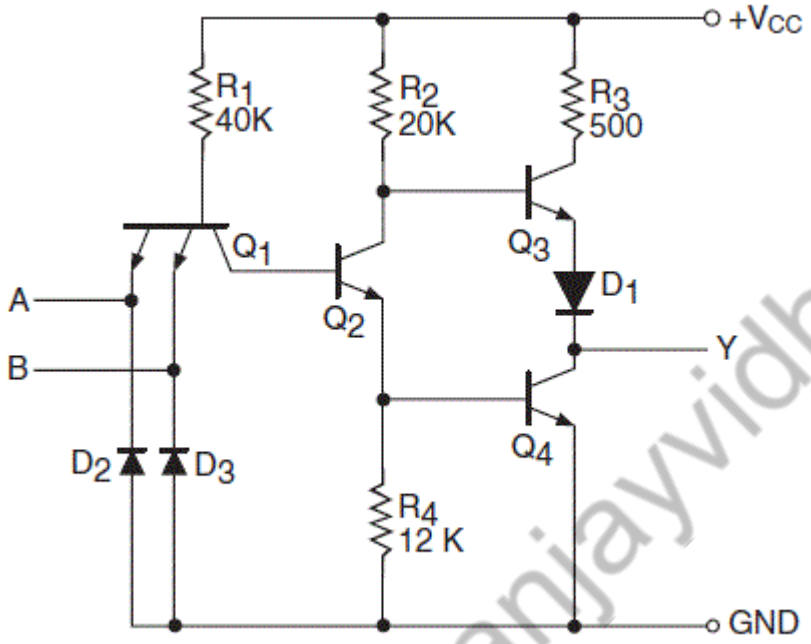
Advantages

- Diodes perform the logical function

Disadvantages

- The obvious disadvantage of DTL is its high current dissipation when the transistor conducts to overdrive the output biasing resistor.
- Passive Pull up.
- Limited Fanout
- No Rail-to-Rail Output

TTL Logic



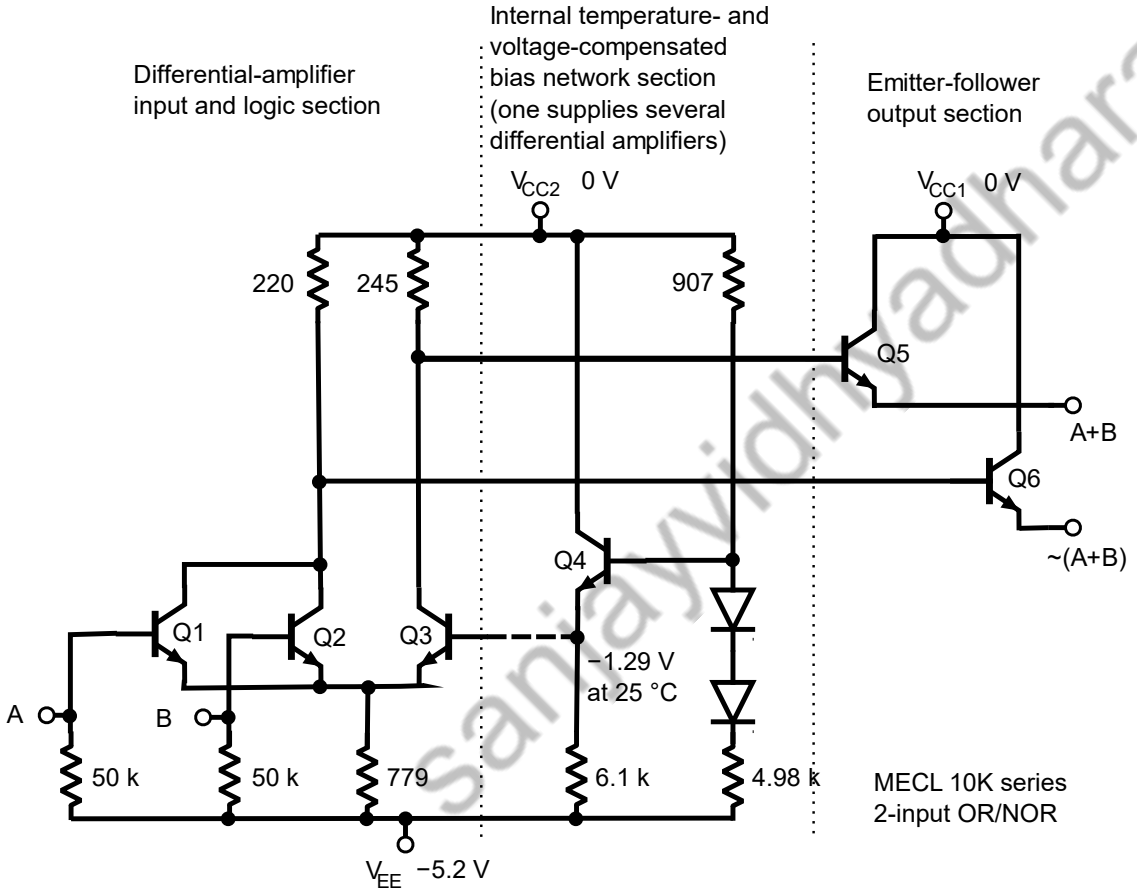
Advantages

- Multi-Emitter perform the logical function
- Active Pull-up and Active Pull down

Disadvantages

- The obvious disadvantage of TTL is its high current dissipation
- No Rail-to-Rail Output

ECL Logic



Advantages

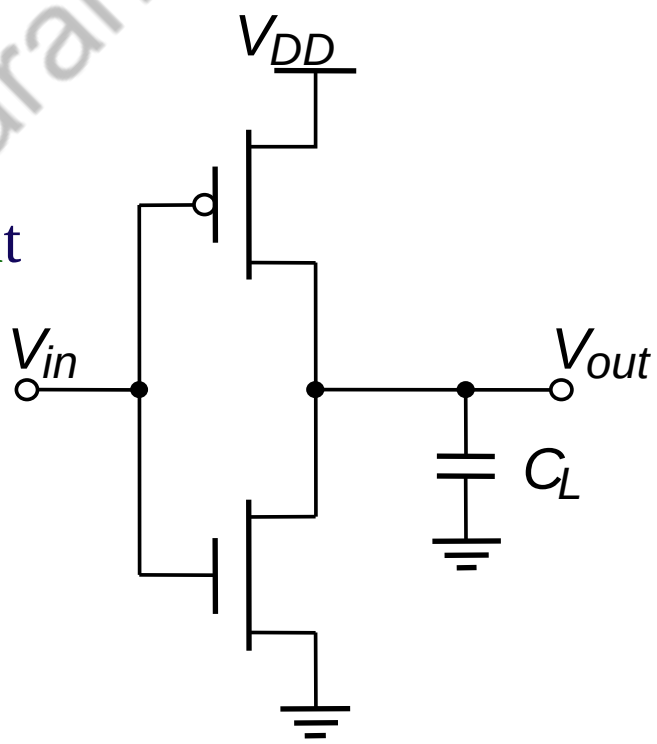
- Fast
- High Fan-out

Disadvantages

- High current dissipation

Advantages of CMOS Technology

- Low Static power consumption
- High input impedance
- Rail to Rail Output
- Active Pull-up and Pull-down of Output
- Simple Design
- High Packing Density
- High noise immunity
- Temperature Stability
- Scalability



Pentium

1993 : Technology : 0.8 μm (16.7 mm by 17.6 mm)

60–66 MHz

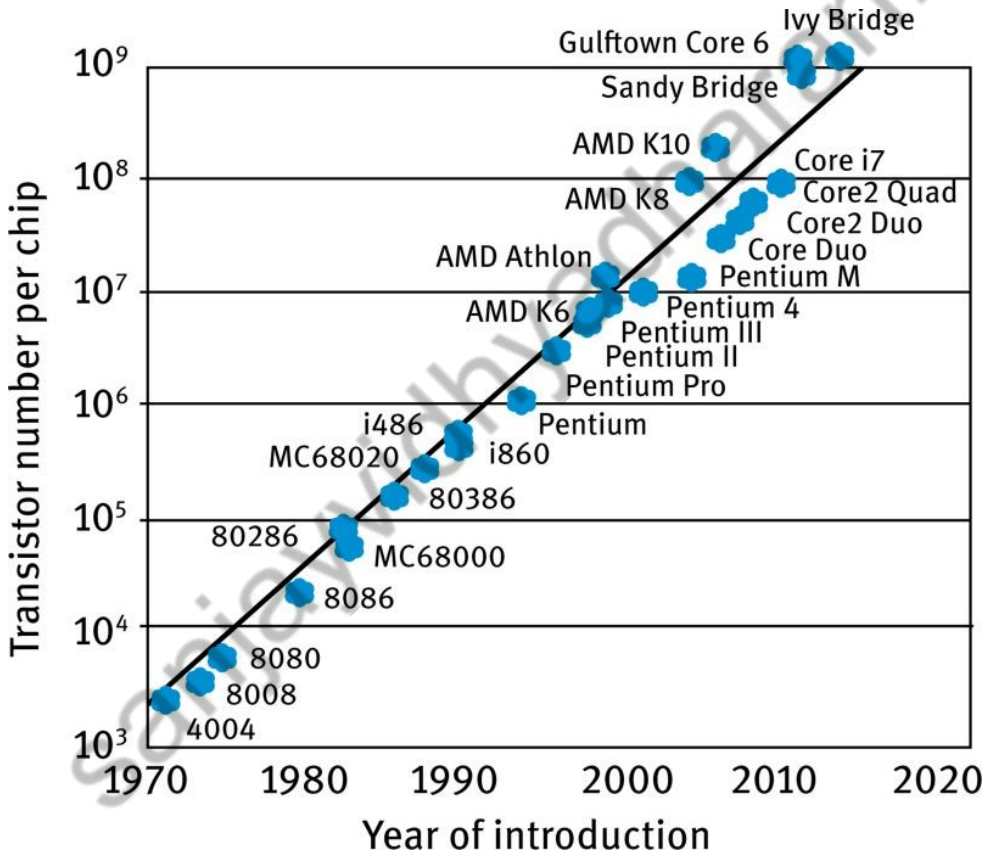
Latest CPUs and GPUs

Latest Trends :- Intel : 14 nm AMD : 7nm

- Billions of Transistors/ Chip
- Frequency of Operation in GHz
- Complex Computational Capability

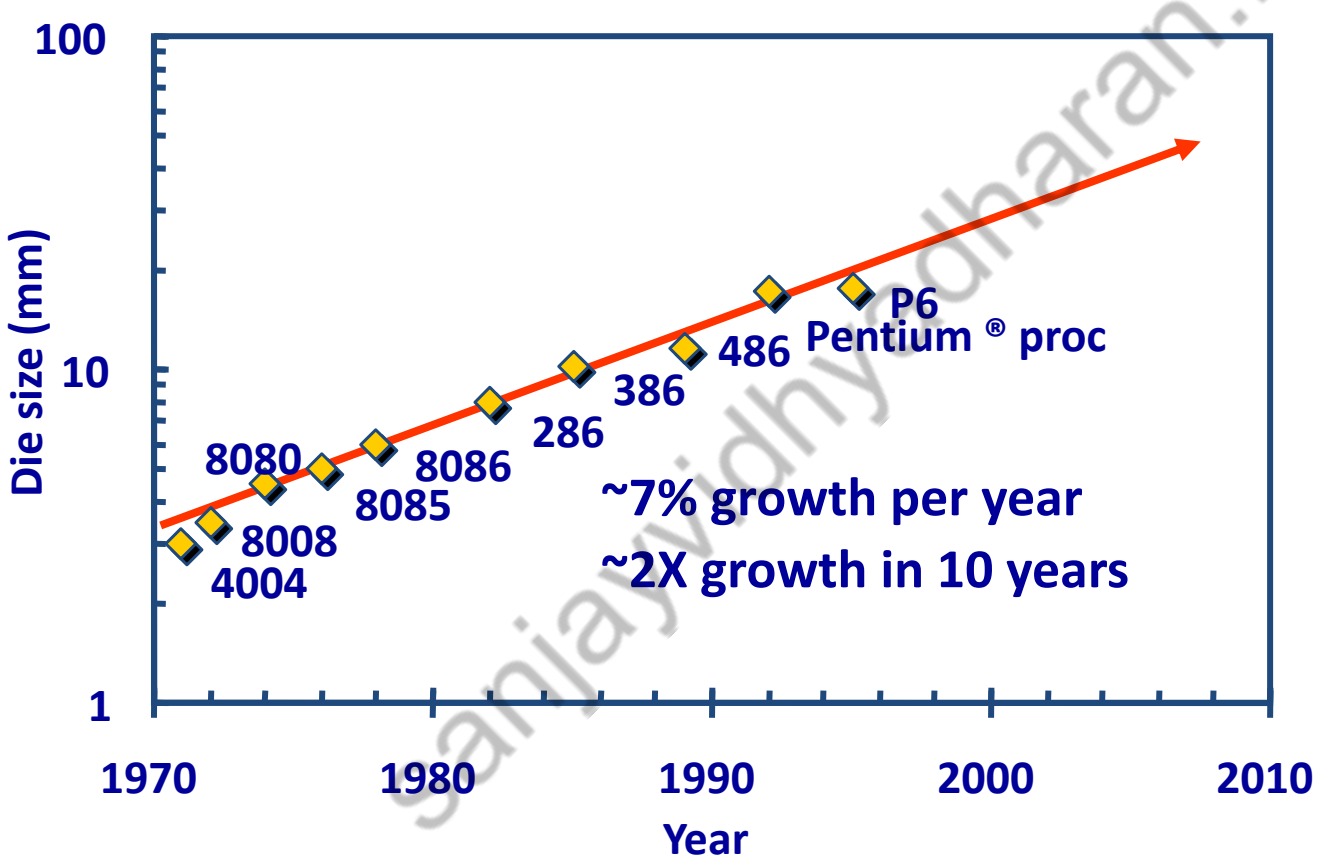
Moore's Law

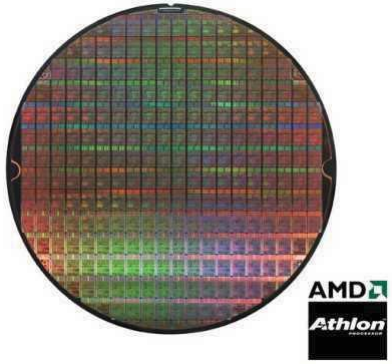
In 1965, Gordon E. **Moore**—co-founder of Intel (NASDAQ: INTC)—postulated that the number of **transistors** that can be packed into a given **unit of space will double about every two years.**



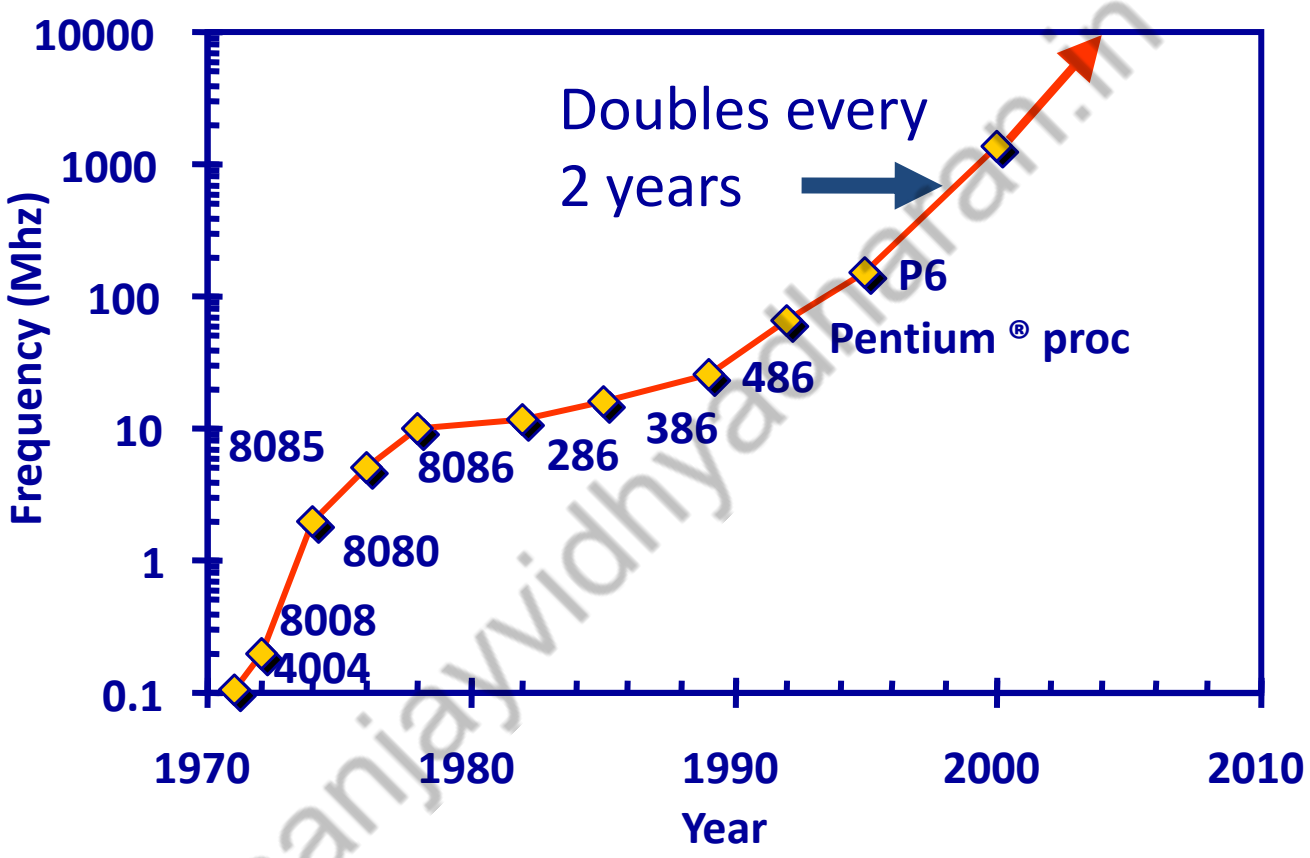
Million-transistor/chip barrier crossed in the late 1980s

Die Size Growth



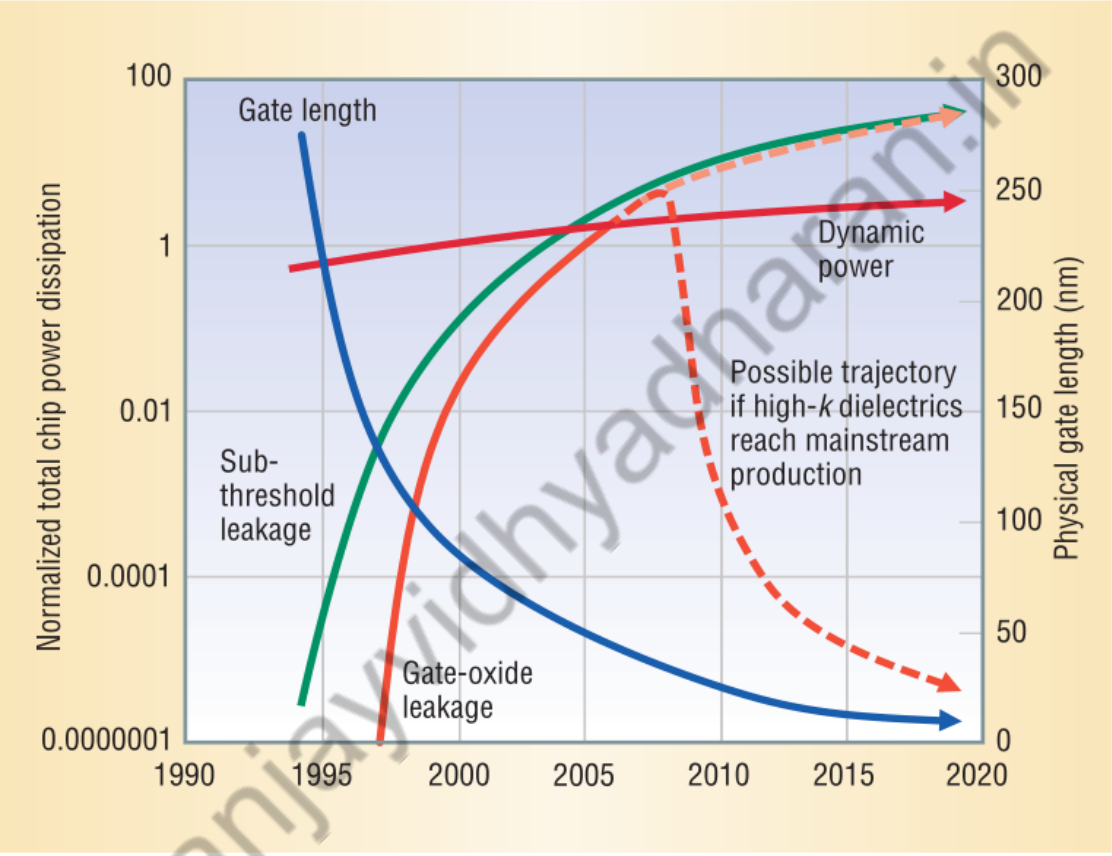


Frequency



Microprocessors frequency doubles every 2 years

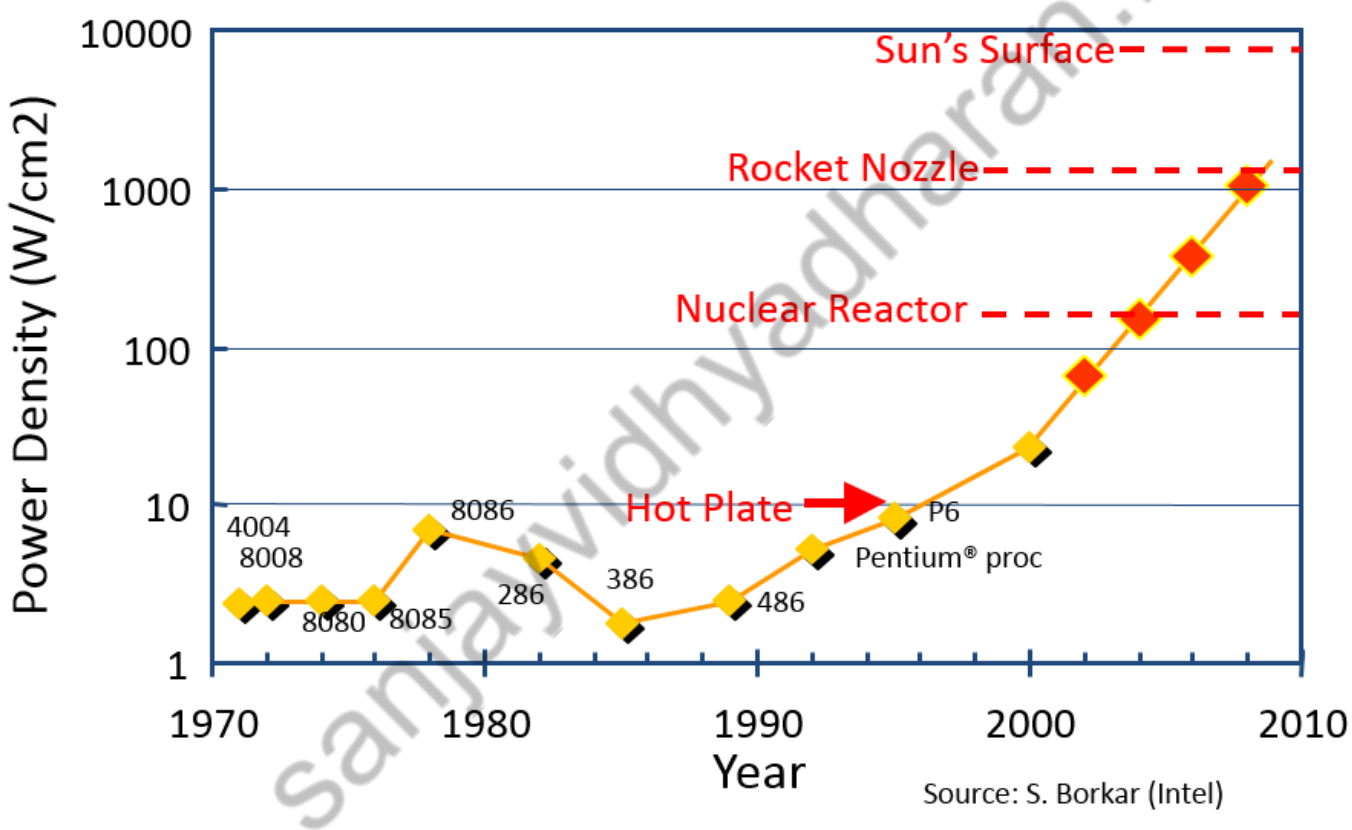
ITRS Prediction of Power Consumption



Semiconductor Industry Assoc., International Technology Roadmap for Semiconductors, 2002 Update; http://public.itrs.net.

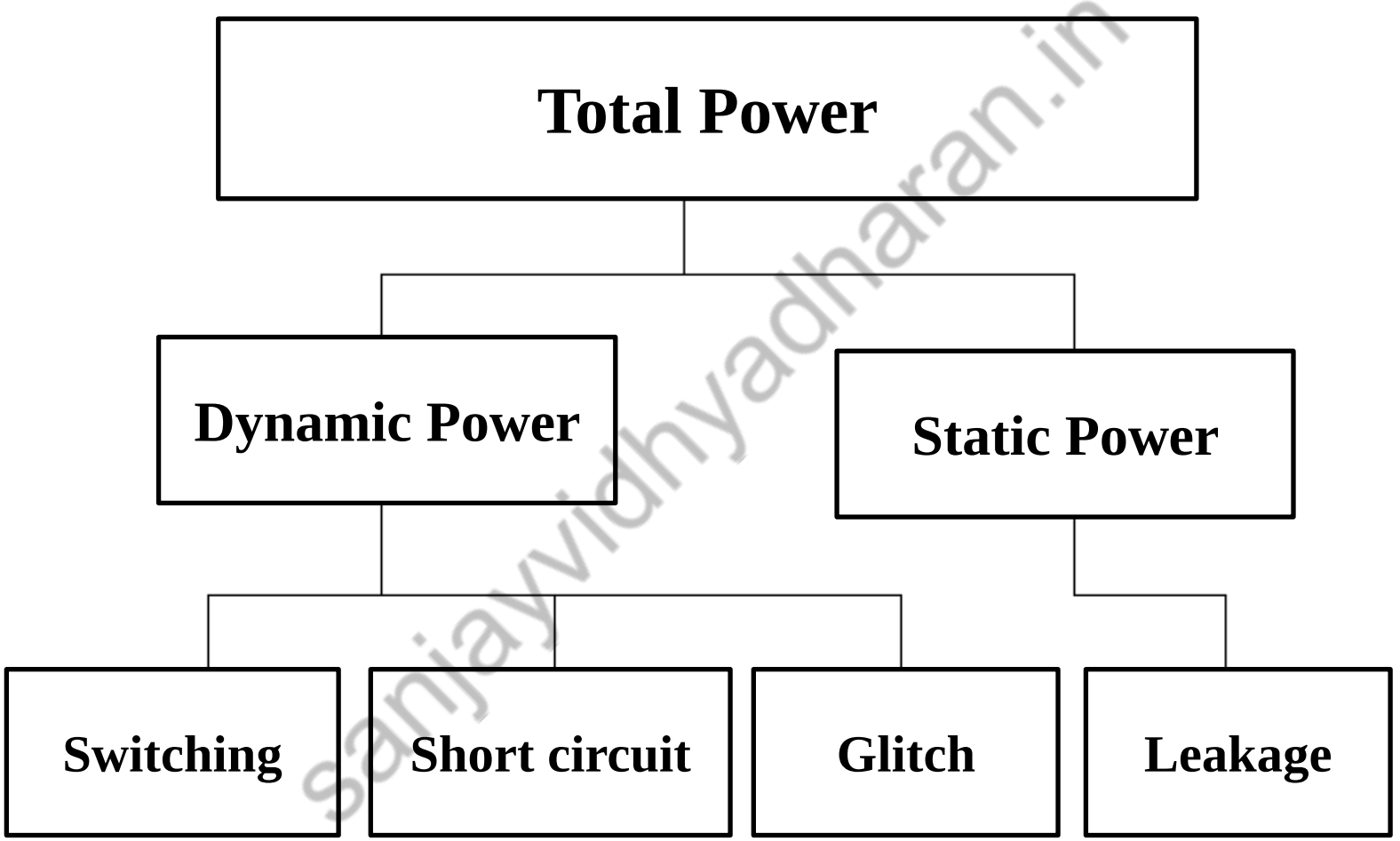
Limitations of Static CMOS

Intel's Prediction of Power Consumption

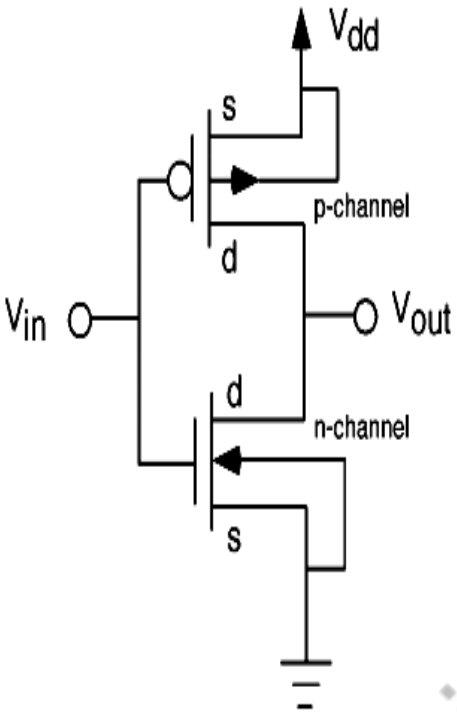


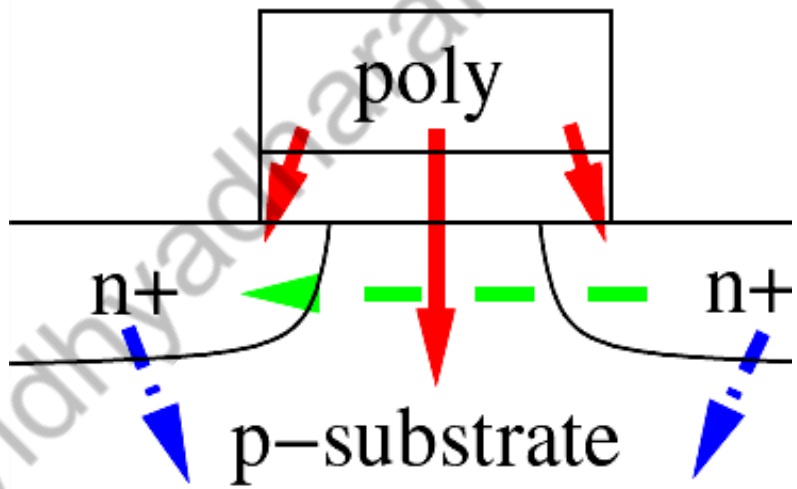
Online Available: http://computerscience.chemeketa.edu/cs160Reader/Parallel Processing/MooresLaw.html

Power Dissipation in CMOS Circuits



Static Loss





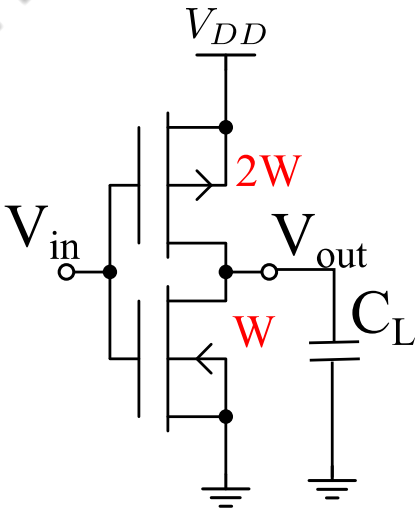
Static Power Dissipation in CMOS

Static Loss

➢ Causes for High Static Power Consumption

Effect of Decreasing V_{DD} on Delay

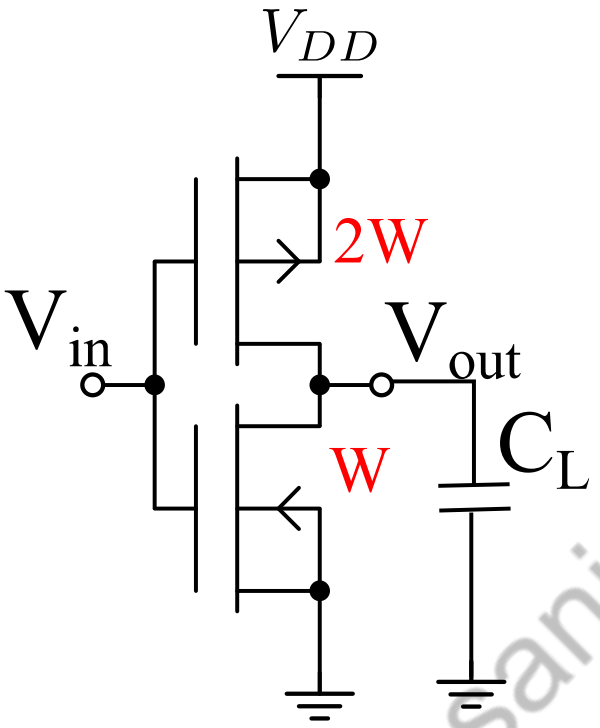
$$Propagation\ Delay\ (tpd) = \frac{K_1 C_L}{I_D} = \frac{K_2 C_L}{(V_{DD} - V_{th})^2}$$

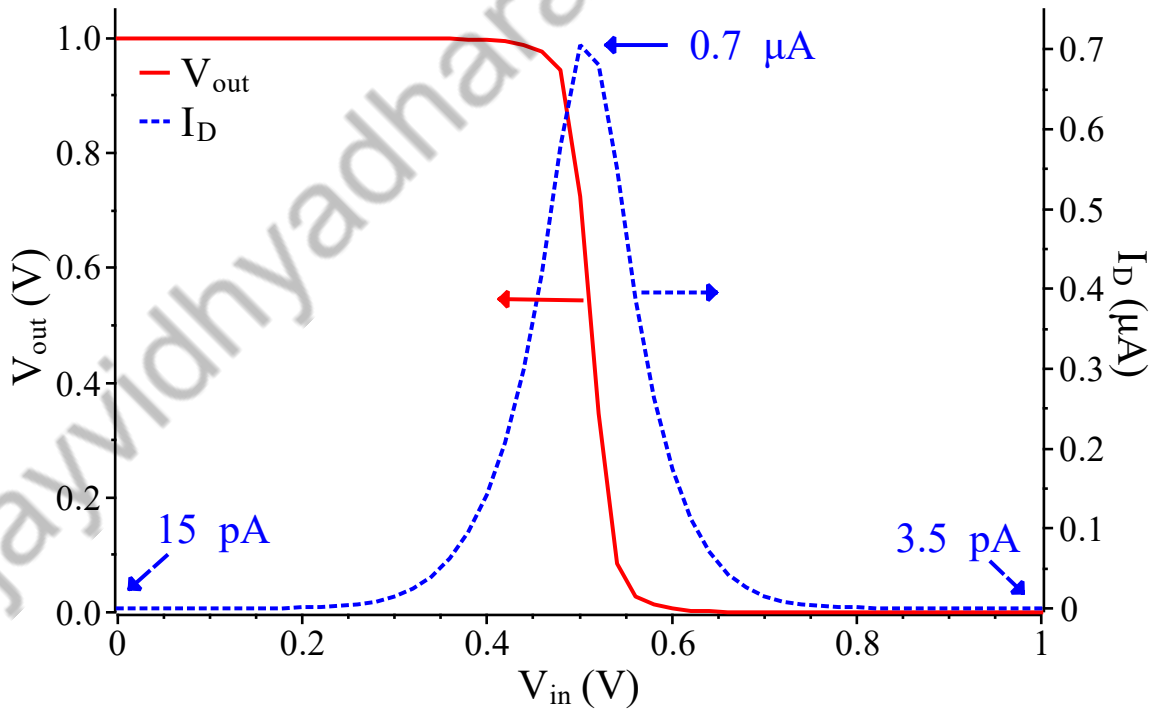


Effect of Decreasing V_{th} on Power

- Intel estimated leakage power consumption at more than 50W for a 100nm technology node.
- Leakage depends strongly on a Threshold voltage (V_{th}) of the transistor

Static Loss





Static Loss

➢ Reducing Static Loss

- Device Level Techniques
  - Tunnel Field Effect Transistors
  - CNFETs
- Circuit Level Techniques when using CMOS

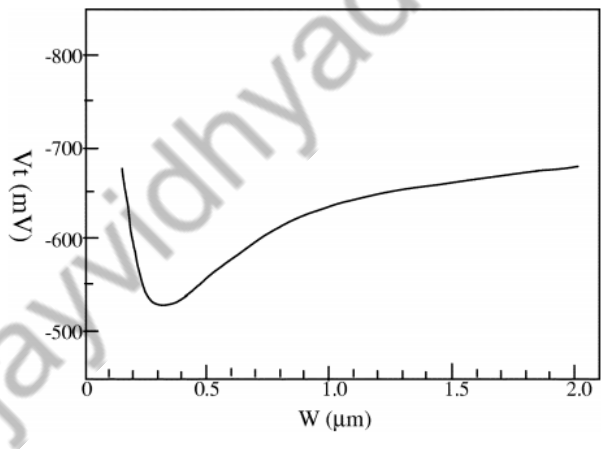
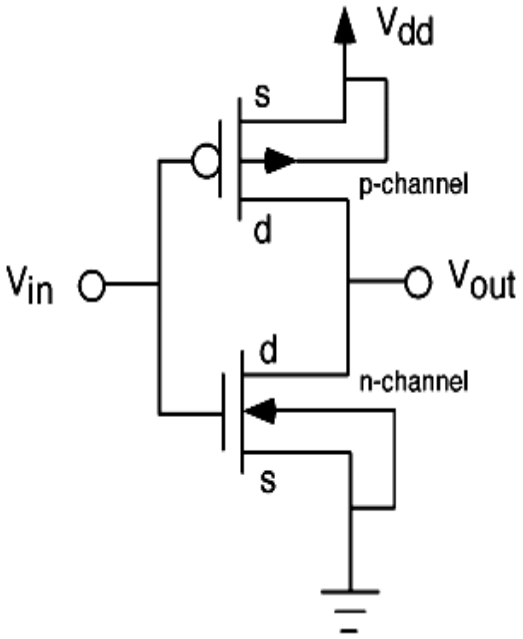
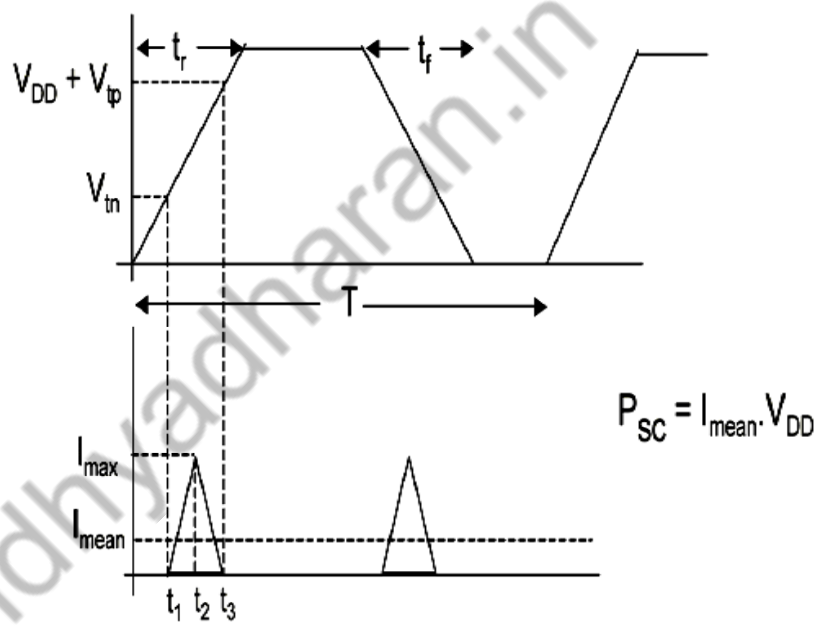


Fig. 12 Variation of threshold voltage with gate width in the case of trench isolated buried channel P-MOSFET showing the anomalous behavior [27].

[3] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," Proceedings of the IEEE, vol. 91, no. 2, pp. 305–327, Feb. 2003.

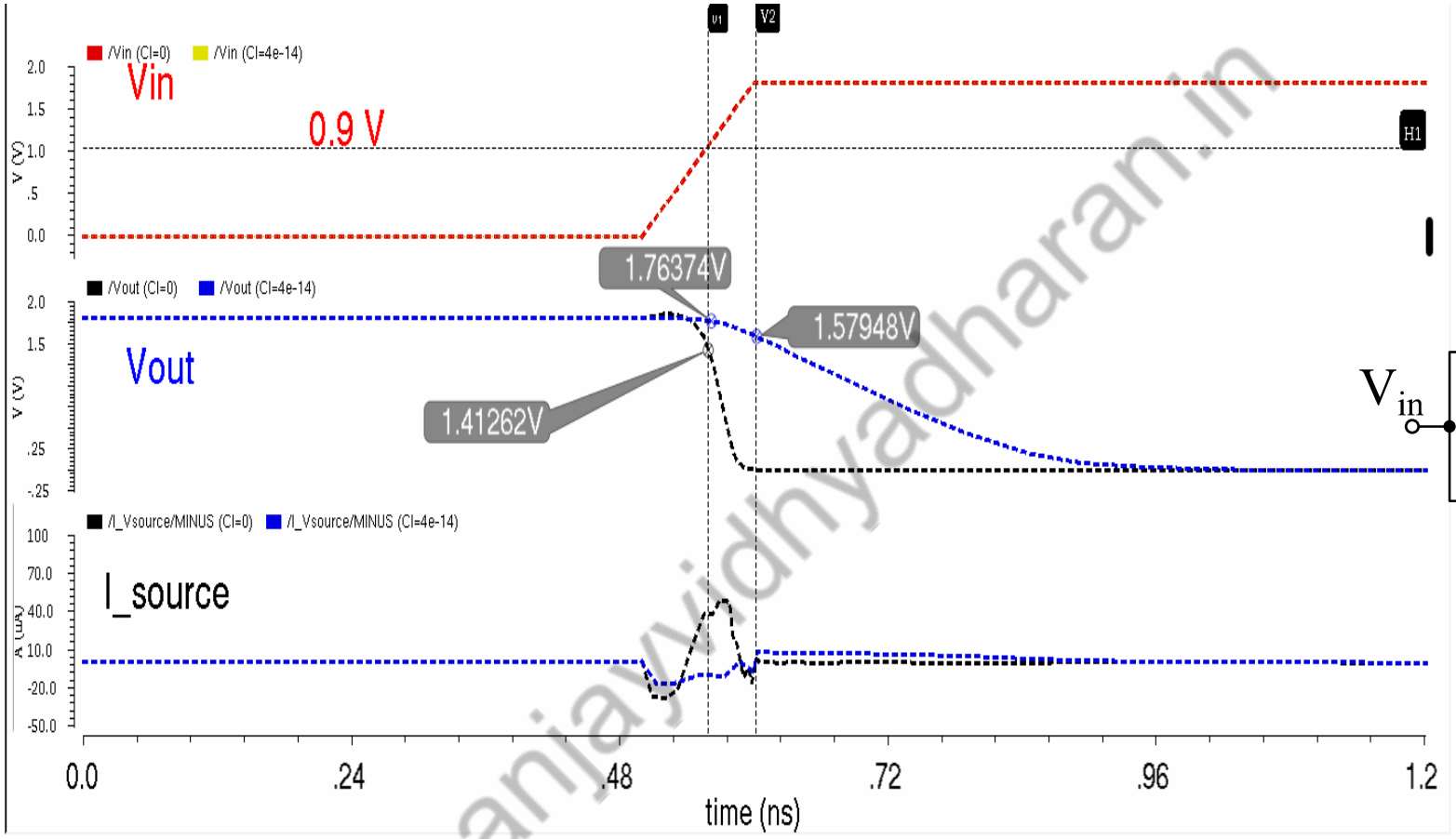
Short Circuit Loss

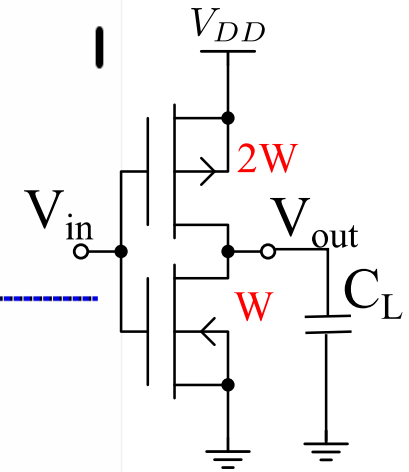




- Use devices with V_{th} close to $\frac{V_{DD}}{2}$ & steep switching characteristics
- Short Circuit loss reduces with C_{load}

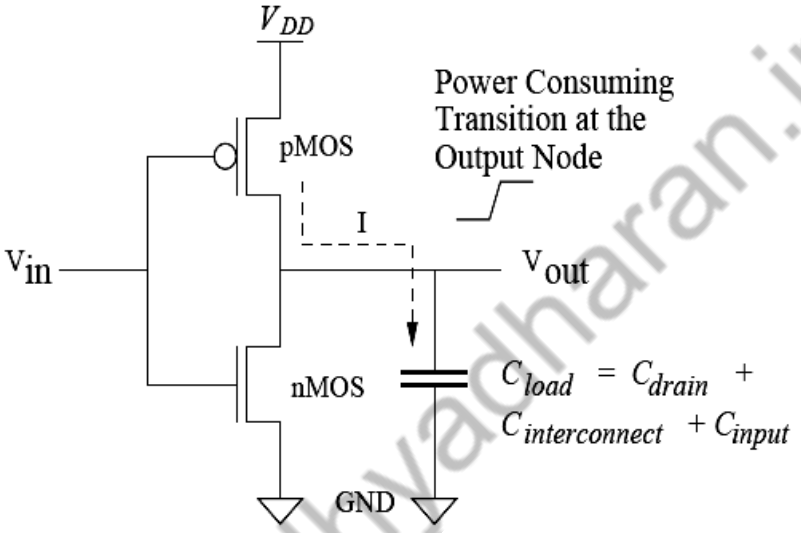
Short Circuit Loss





- Short Circuit loss reduces with C_{load}

Switching Loss



Energy stored in C_{Load} $(C_L) = \int_0^{V_{DD}} V_C \, C_L dV_c = \frac{1}{2}.V_{DD}^2 * C_L$

Energy consumed from power supply= $V_{DD} \int_0^T i(t)dt = V_{DD}.Q_{CL} = V_{DD}^2.C_L$

Energy dissipated in pMOSFET during charging = $\frac{1}{2}.V_{DD}^2.C_L$

Energy dissipated in nMOSFET during discharging = $\frac{1}{2}.V_{DD}^2.C_L$

Power Consumption = Frquency.$V_{DD}^2.C_L$

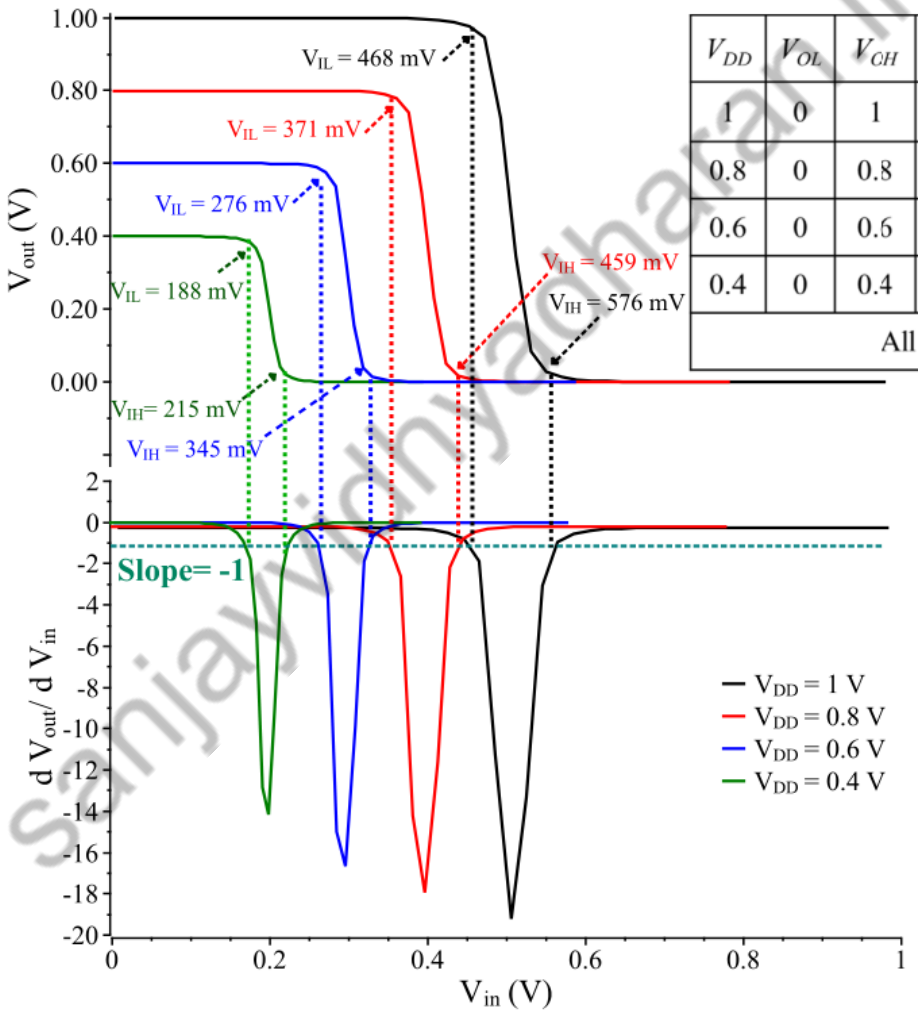
High Dynamic Power Consumption

$$P_{Dynamic} = Freq * V_{DD}^2 * C_L$$

- V_{DD} & C_L : Reduced by 30 % each generation
- Frequency : 43 % Increase
  - Architectural optimizations
  - Consumer requirements
- Transistors per chip : Increased exponentially
  - Advancement in lithography
  - Multilayer metallization
  - Efficient partitioning and routing techniques

Figure of Merits of a Digital Circuit

1. Noise Margin



V_{DD}	V_{OL}	V_{OH}	V_{IL}	V_{IH}	NM_L	NM_H
1	0	1	0.468	0.576	0.468	0.424
0.8	0	0.8	0.371	0.459	0.371	0.341
0.6	0	0.6	0.276	0.345	0.276	0.255
0.4	0	0.4	0.188	0.215	0.188	0.185
All values are in Volts						

Figure of Merits of a Digital Circuit

2. Propagation Delay (Eg. Inverter)

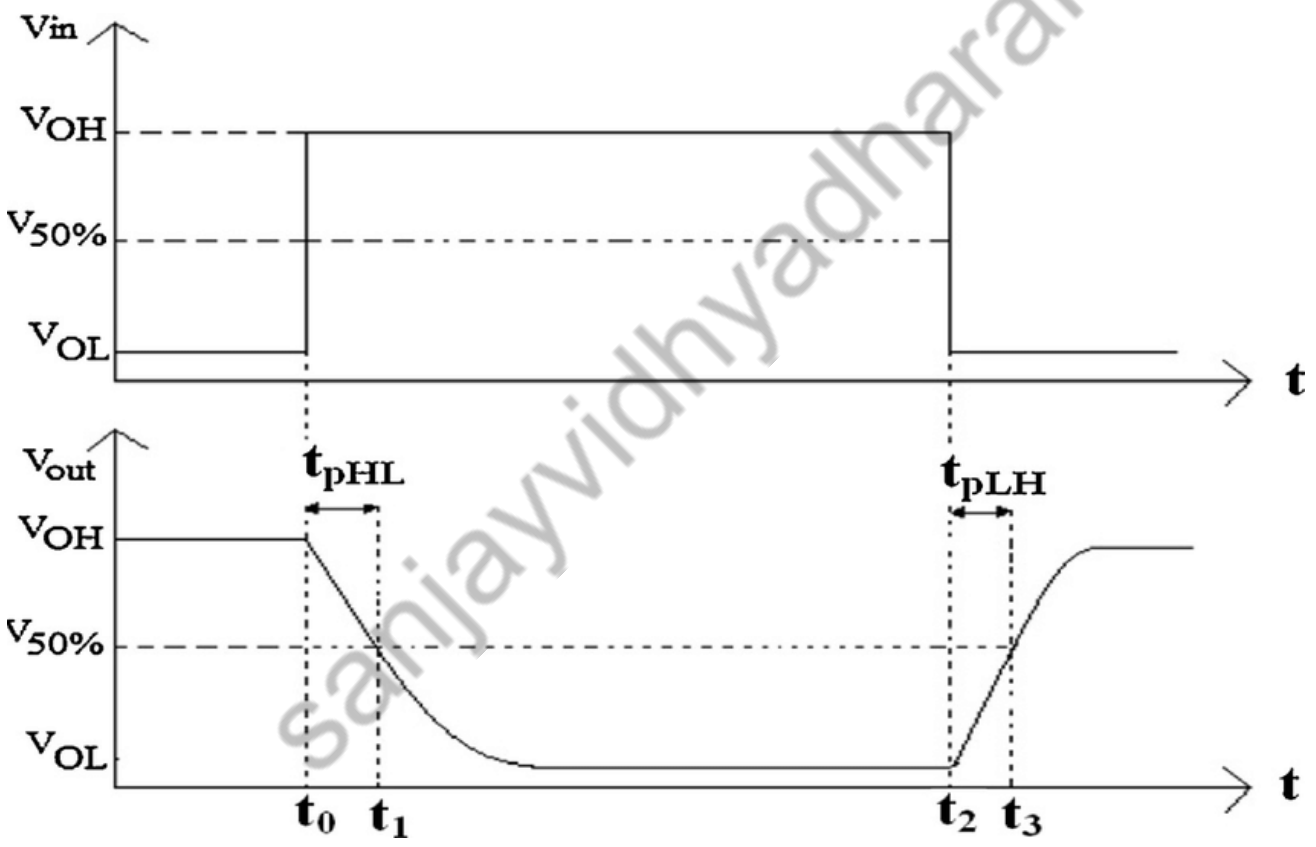
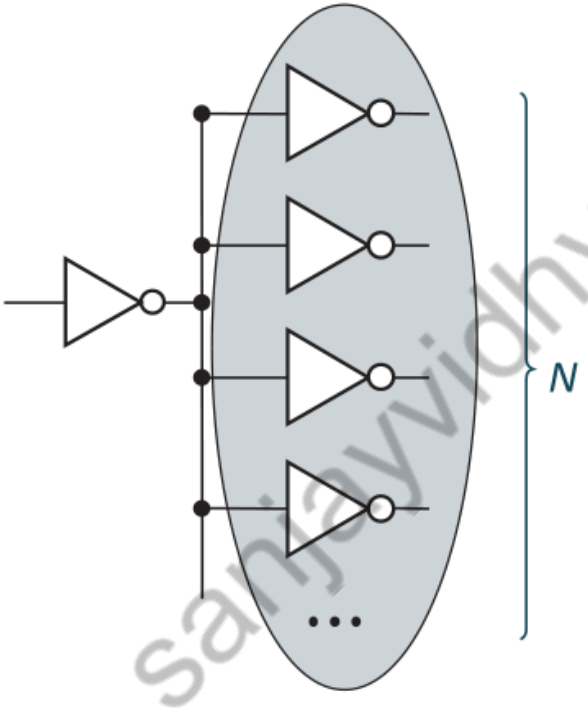
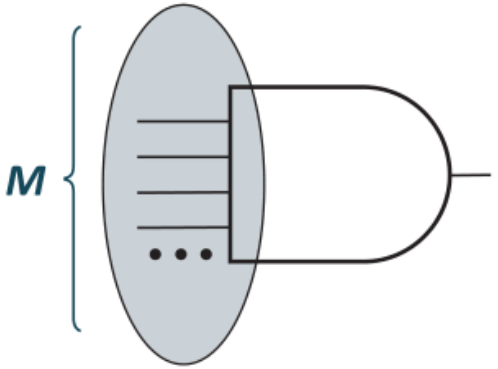


Figure of Merits of a Digital Circuit

3. Fan-in and Fan-Out



Fan-out *N*



Fan-in *M*

Figure of Merits of a Digital Circuit

4. Power and Energy Consumption

- **Power consumption of design determine**
  - How much energy is consumed per operation
  - How much heat the circuit dissipates

- **Determine critical design decision**
  - Power supply capacity, battery lifetime,
  - Supply line sizing, packaging and cooling

- **Peak power is important for supply line sizing**

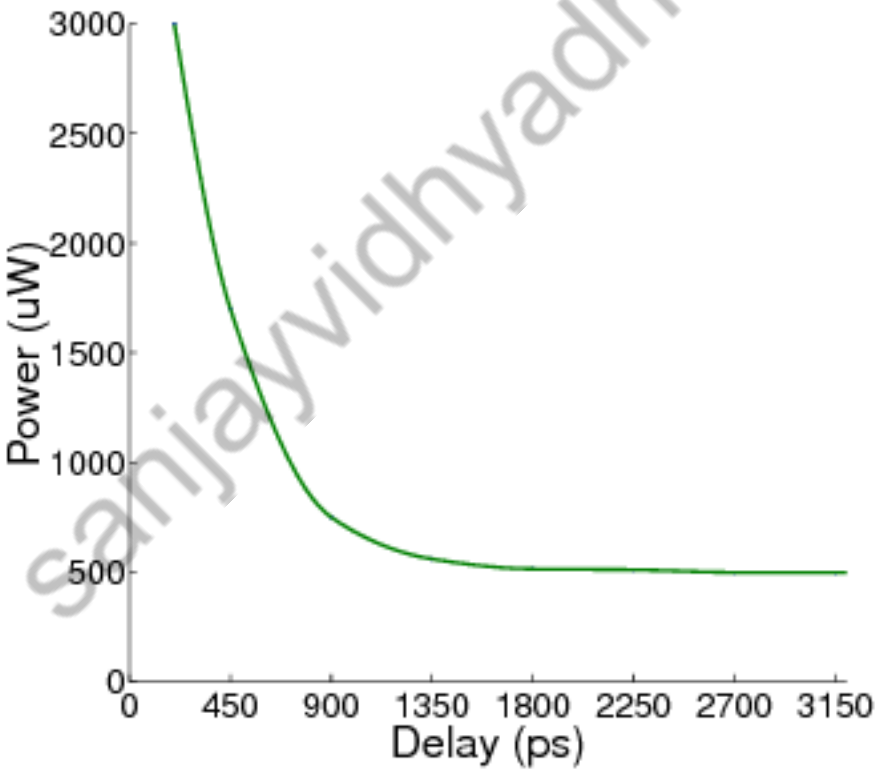
- **Average power dissipation is important for cooling or battery requirements**

Figure of Merits of a Digital Circuit

5. Power Delay Product

$P_{Dynamic} = Freq * V_{DD}^2 * C_L$

$$Propagation\ Delay\ (tpd) = \frac{K_1 C_L}{I_D} = \frac{K_2 C_L}{(V_{DD} - V_{th})^2}$$



Thank you