VLSI Design Using LT SPICE
SRAM Design

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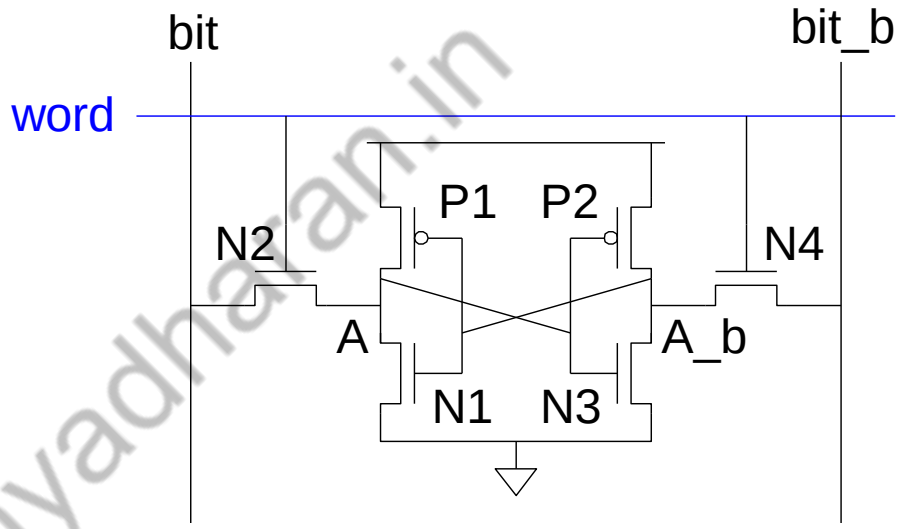
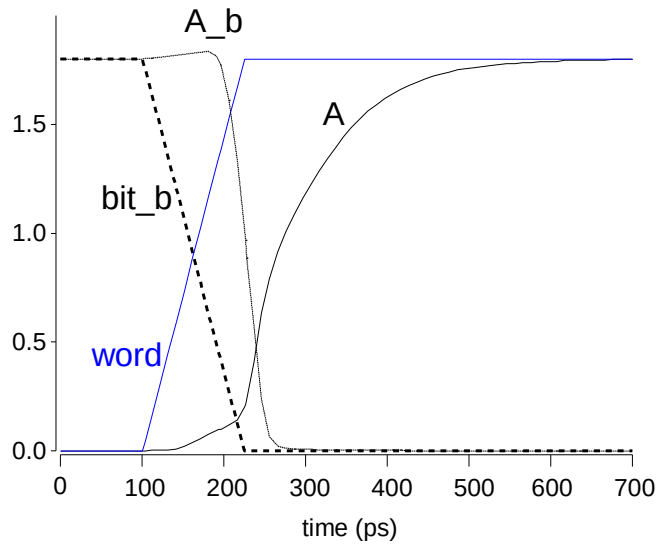
6T SRAM

Write

- Drive one bitline high, the other low
- Then turn on wordline
- Bitlines overpower cell with new value
- *Writability*
  - Must overpower feedback inverter
  - N2 >> P1

Ex: A = 0, A_b = 1,
bit = 1, bit_b = 0
Force A_b low, then A rises high



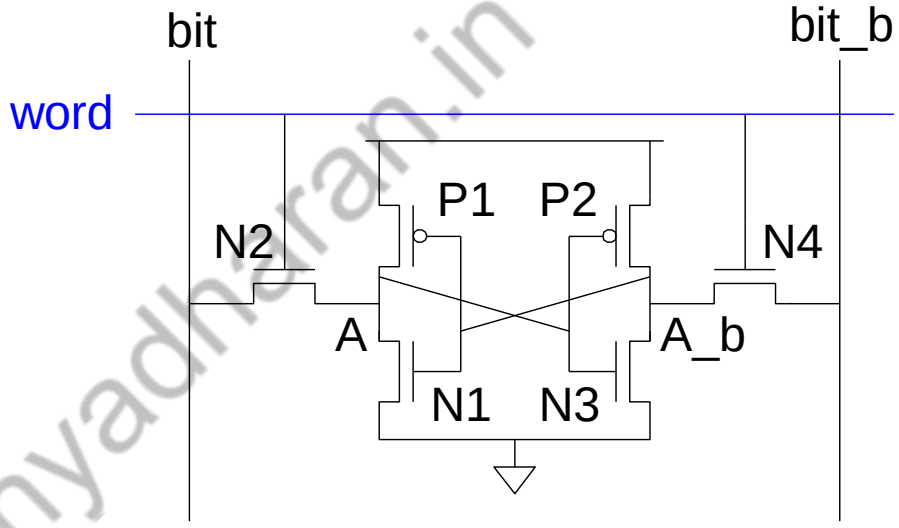


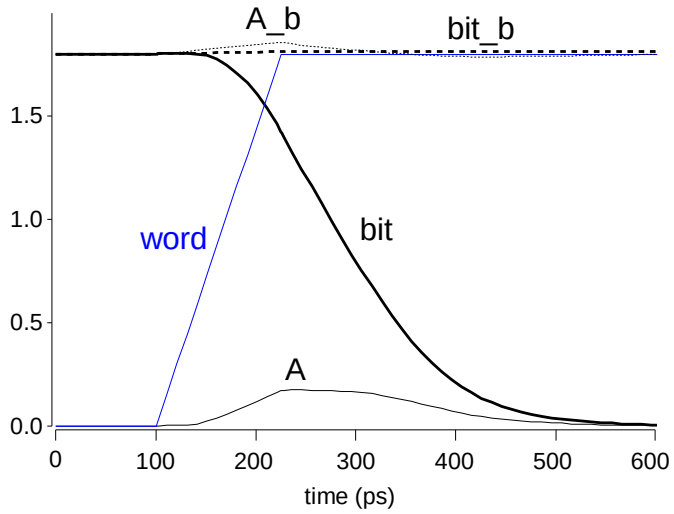
6T SRAM

Read

- Precharge both bitlines high
- Then turn on wordline
- One of the two bitlines will be pulled down by the cell
- *Read stability*
  - A must not flip
  - N1 >> N2

Ex: A = 0, A_b = 1
bit discharges, bit_b stays high
But A bumps up slightly



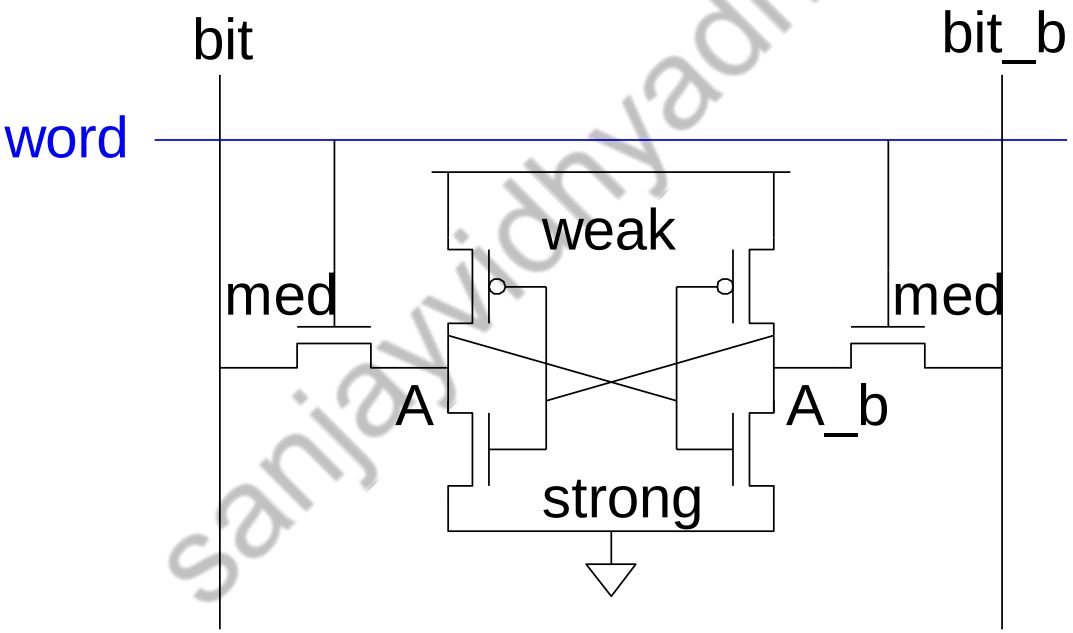


6T SRAM

SRAM Sizing

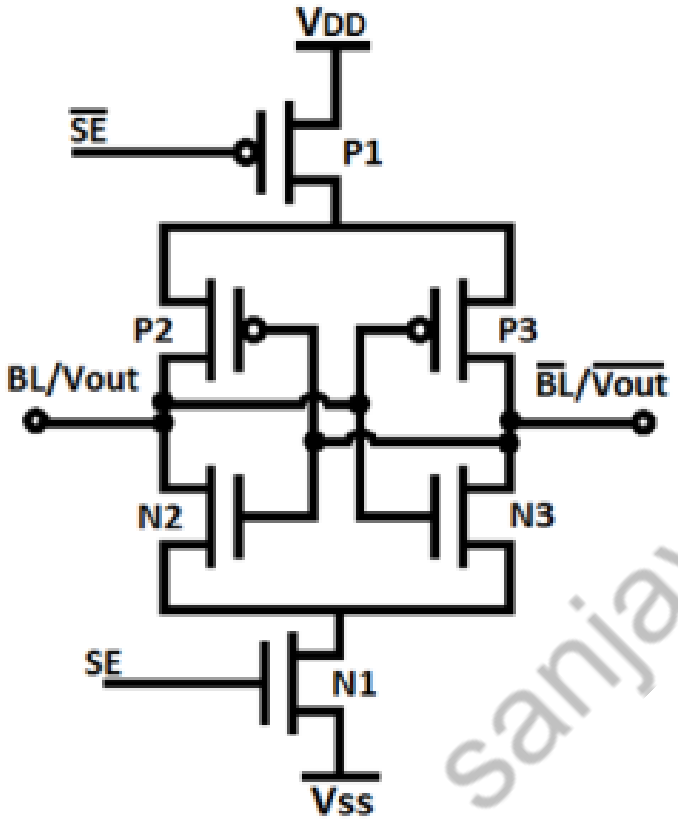
High bitlines must not overpower inverters during reads

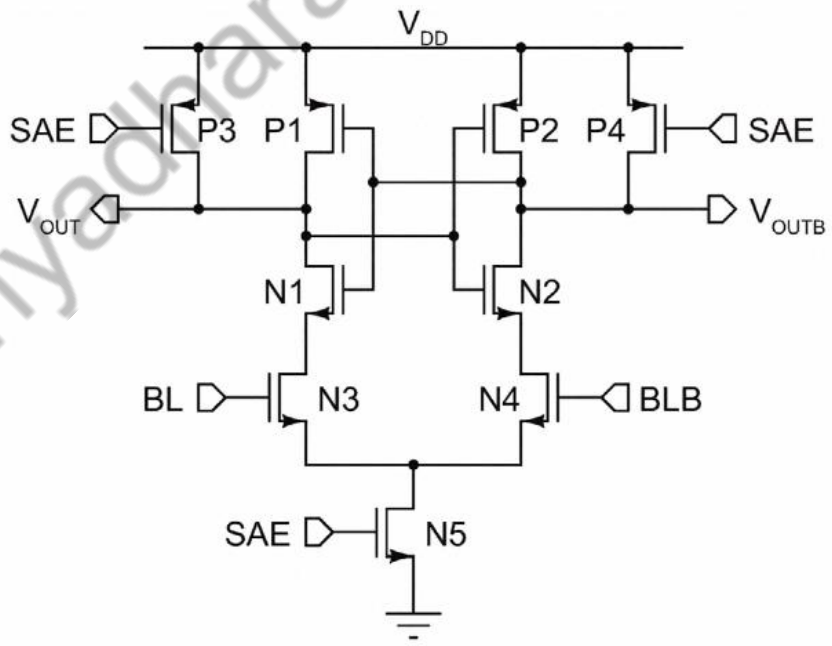
But low bitlines must write new value into cell



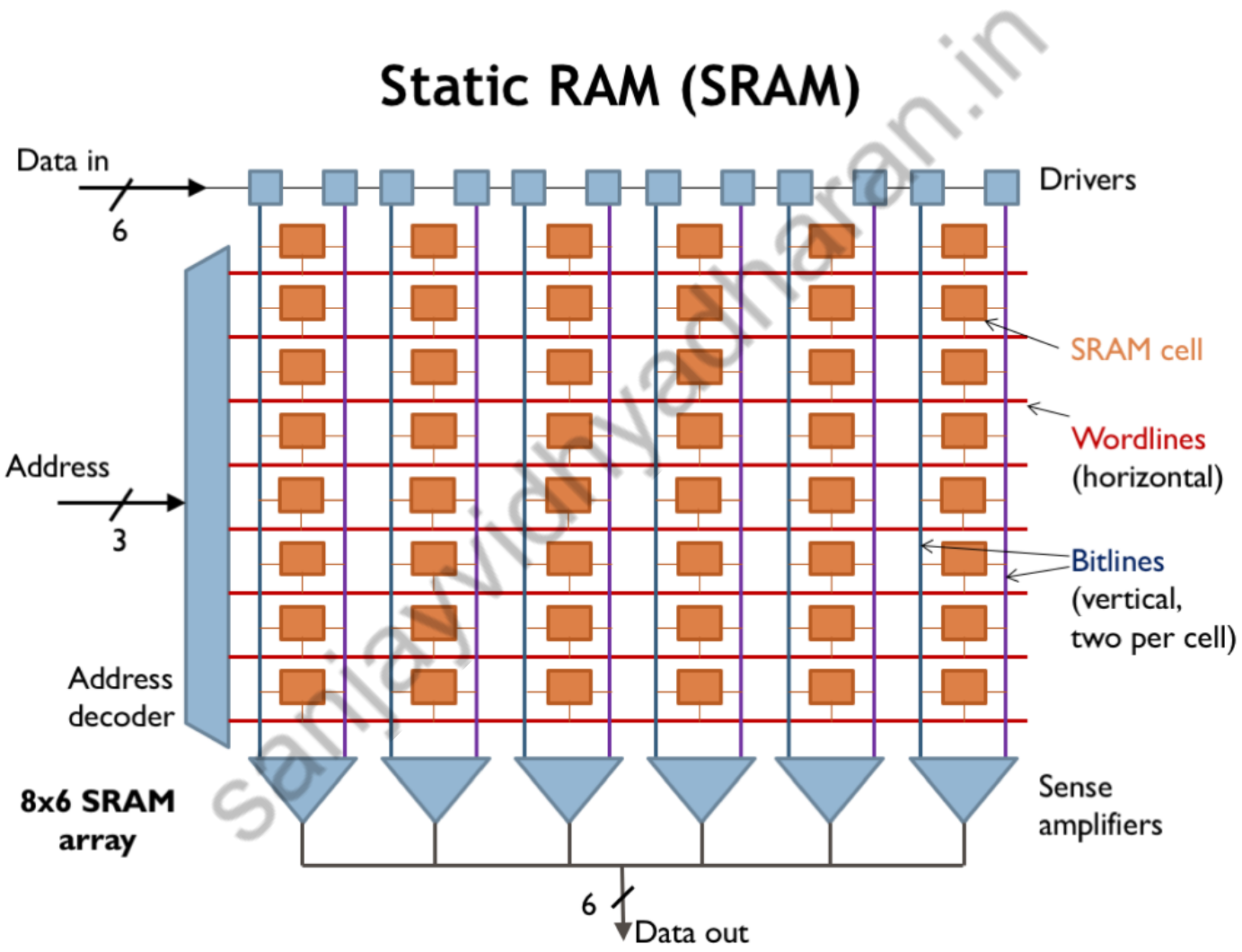
6T SRAM

SRAM Sense Amplifier





SRAM ARRAY



Thankyou