VLSI Design Using LT SPICE
Pass Transistor Logic Design

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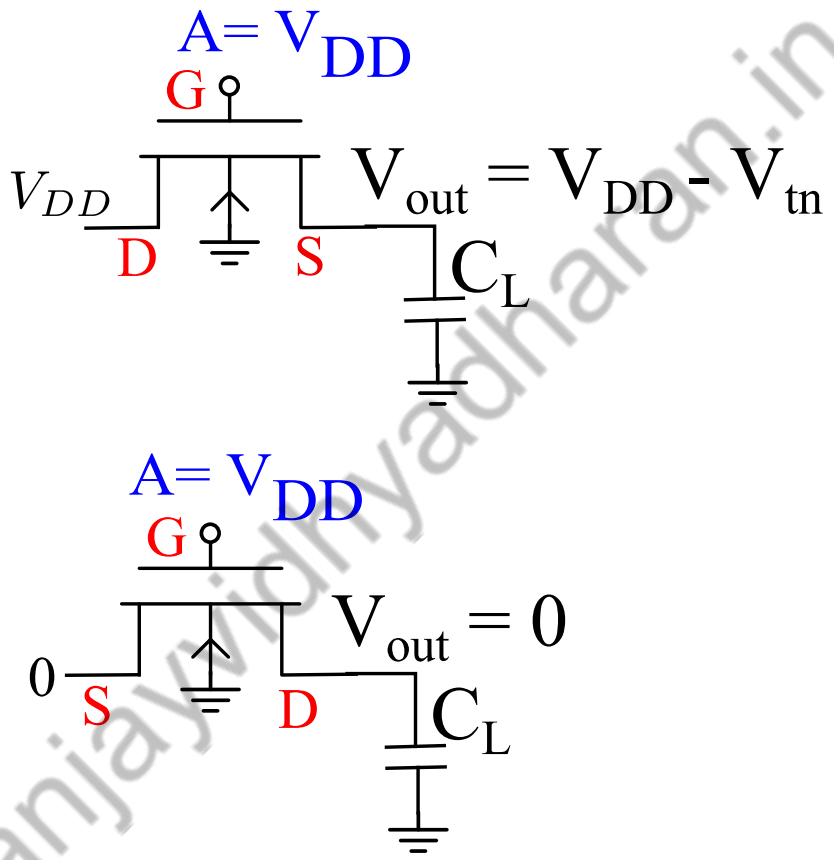
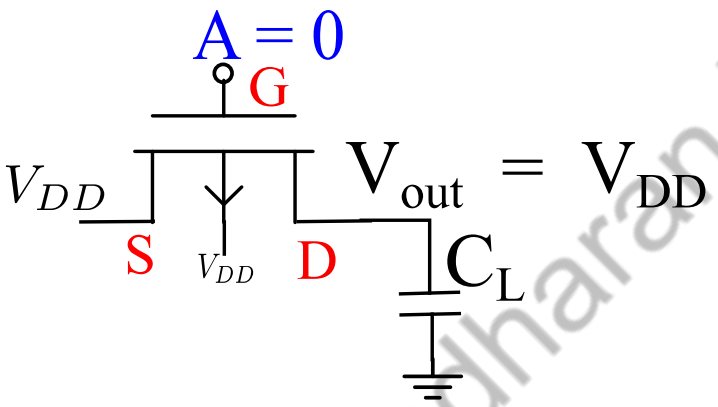
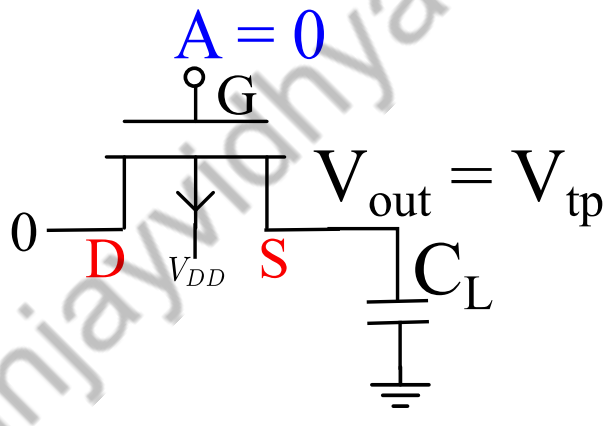
Pass Transistor Logic



- NMOS Pass perfect 0 but not 1

Pass Transistor Logic

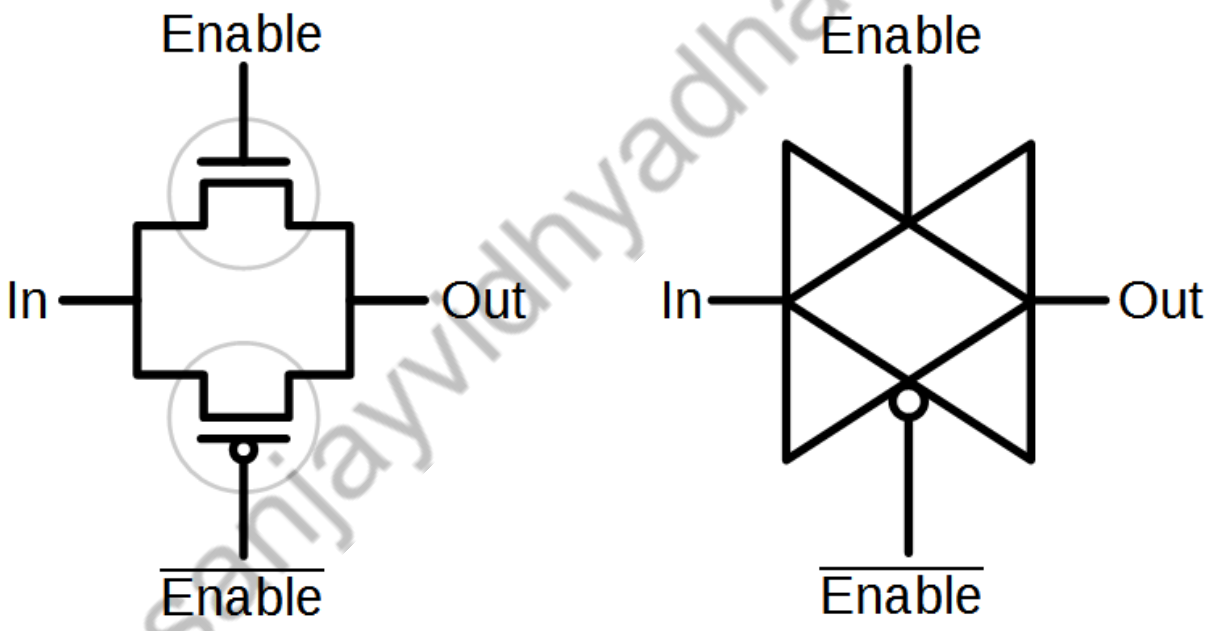




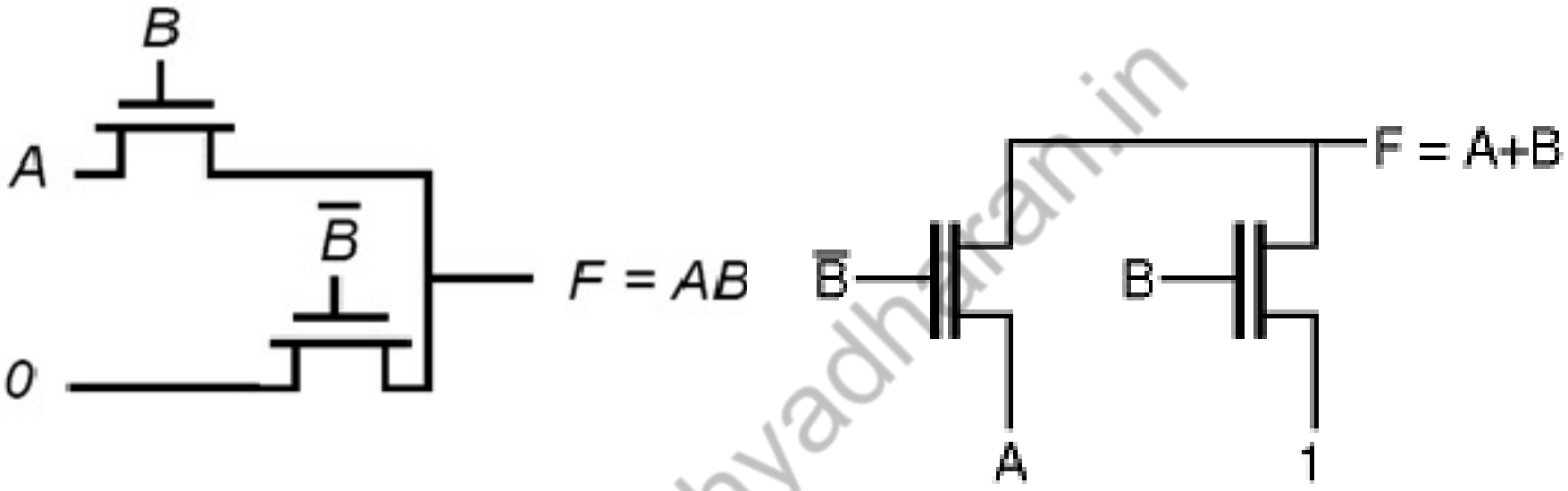
- PMOS Pass perfect 1 but not 0

Pass Transistor Logic

Complimentary Pass Transistor Logic (CPTL)



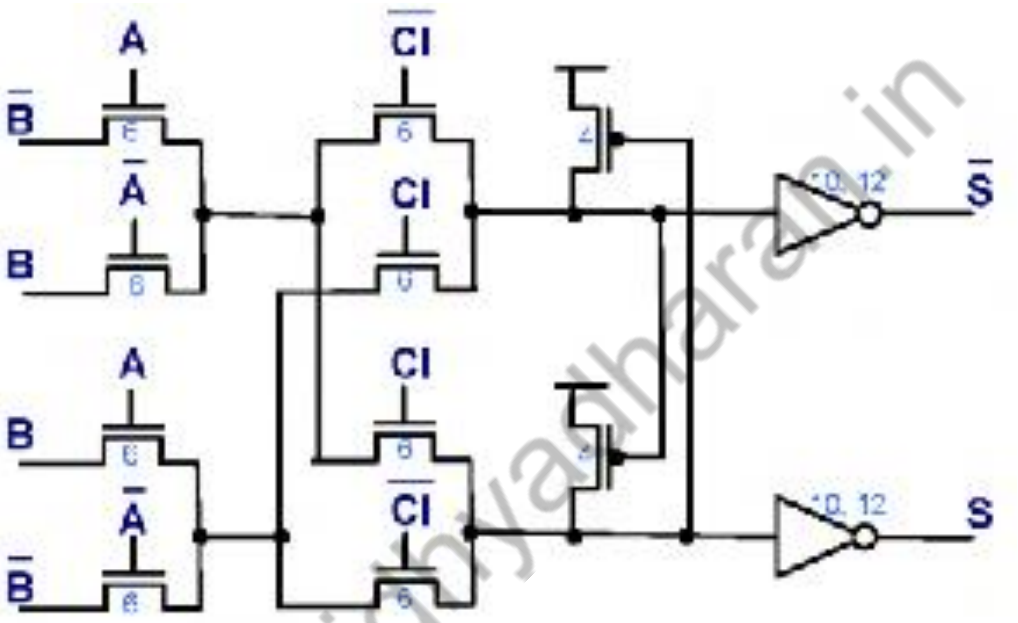
Pass Transistor Logic



- Negligible Static Dissipation
- Lesser Dynamic Dissipation
  - Short Circuit
  - Switching Loss

Pass Transistor Logic

Full Adder



$$Sum = A \bullet B' \bullet C_{in}' + A' \bullet B \bullet C_{in}' + A' \bullet B' \bullet C_{in} + A \bullet B \bullet C_{in}$$

For Cin = 0 Sum = A•B' + A'•B

For A = 0 Sum =B

For A = 1 Sum =B'

For Cin = 1 Sum = A'•B' + A•B

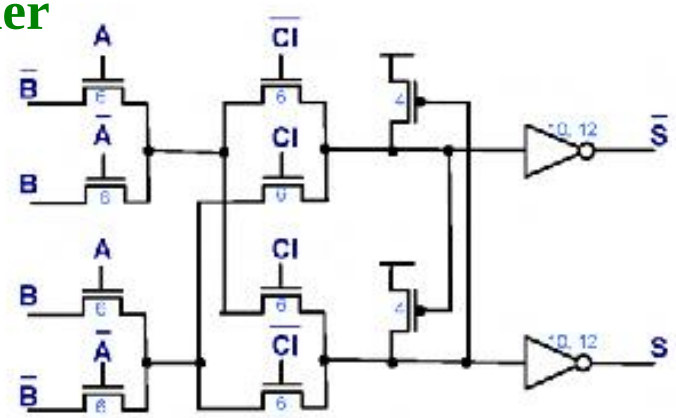
For A = 0 Sum =B'

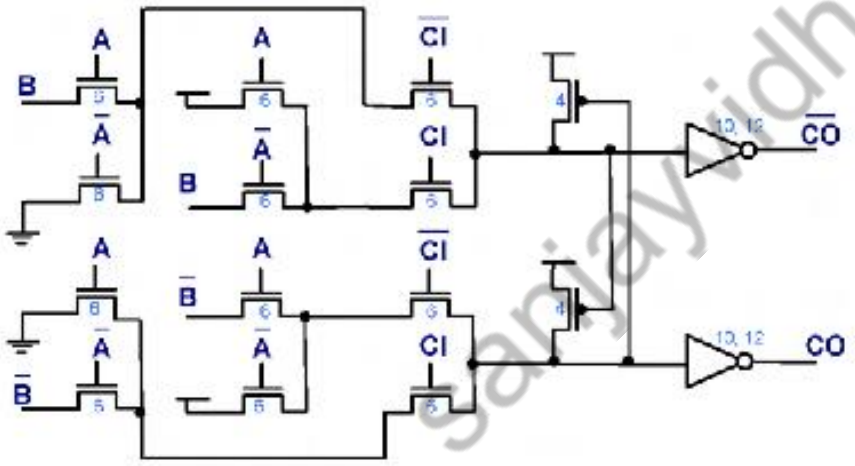
For A = 1 Sum =B

[8] L. Gao, "High performance Complementary Pass transistor Logic full adder," in Proceedings of 2011 International Conference on Electronic Mechanical Engineering and Information Technology, vol. 8, Aug. 2011, pp. 4306–4309.

Pass Transistor Logic

Full Adder





$$C_{out} = A \bullet B + B \bullet C_{in} + A \bullet C_{in}$$

$$C'_{out} = (A'+B')(B'+C'_{in})(A'+C'_{in})$$

For $C_{in} = 0$ $C'_{out} = (A'+B')$

For A = 0 $C'_{out} = 1$

For A = 1 $C'_{out} = B'$

For Cin = 1 $C'_{out} = (A'+B')\ B'\ A'$

For A = 0 $C'_{out} = B'$

For A = 1 $C'_{out} = 0$

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Thankyou