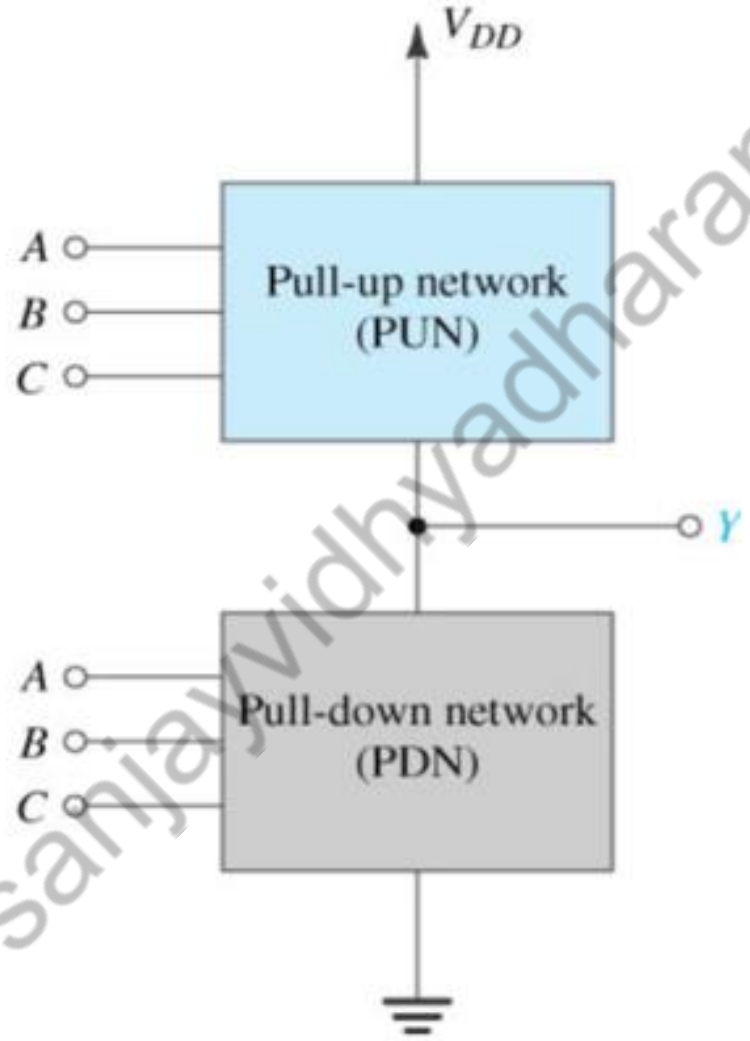
VLSI Design Using LT SPICE
Static CMOS Design

Wing Commander (Retd.) Dr. Sanjay Vidhyadharan

Dept. of EEE (WILP)

BITS Pilani

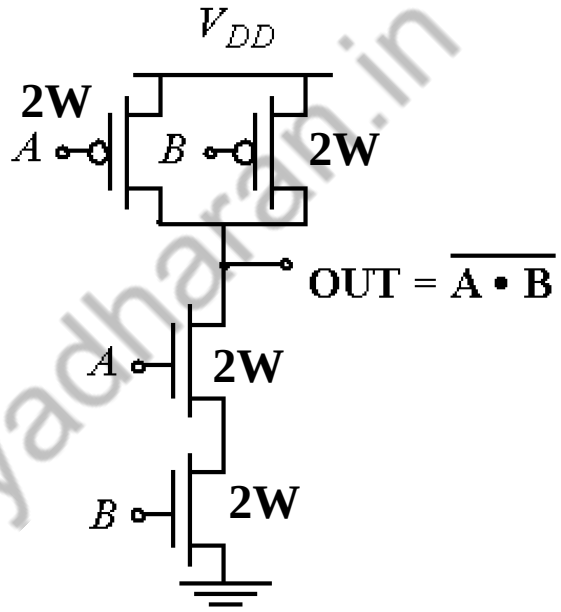
STATIC CMOS



STATIC CMOS

A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

Truth Table of a 2 input NAND gate



PDN By Taking complementary of the Required Function = A.B

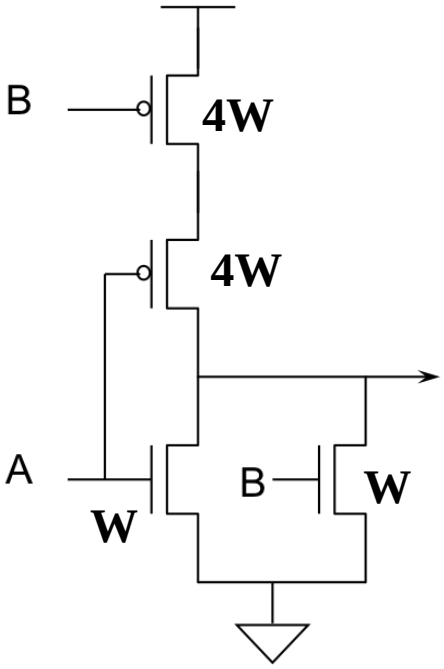
PUP By Taking the Function Directly = A' + B'

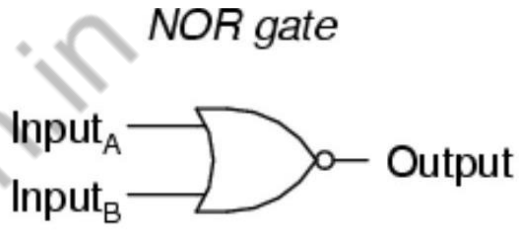
(Inversion of Function Taken care of by PMOS)

AND Implemented by Series Connection

OR Implemented by Parallel Connection

STATIC CMOS





A	B	Output
0	0	1
0	1	0
1	0	0
1	1	0

PDN By Taking complementary of the Required Function = A+B

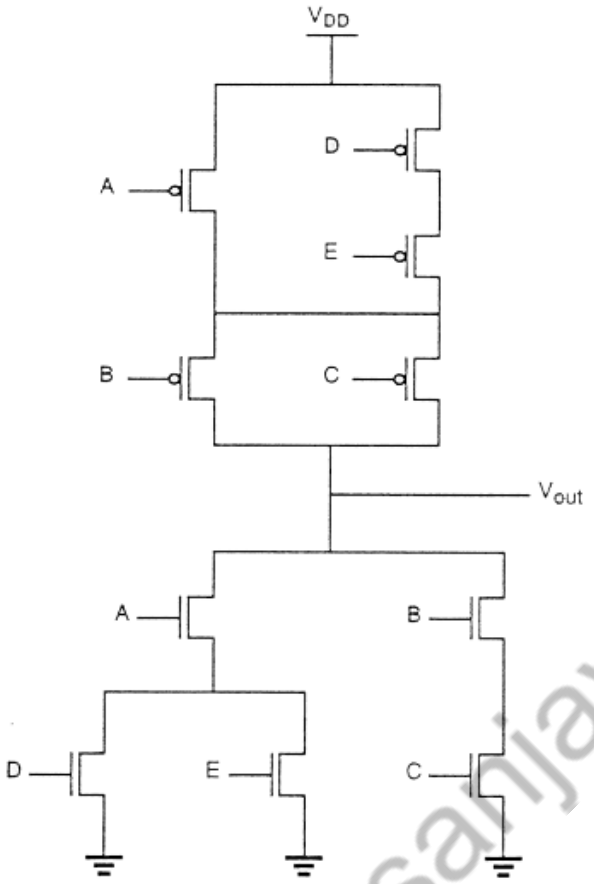
PUP By Taking the Function Directly = A' . B'

(Inversion of Function Taken care of by PMOS)

AND Implemented by Series Connection

OR Implemented by Parallel Connection

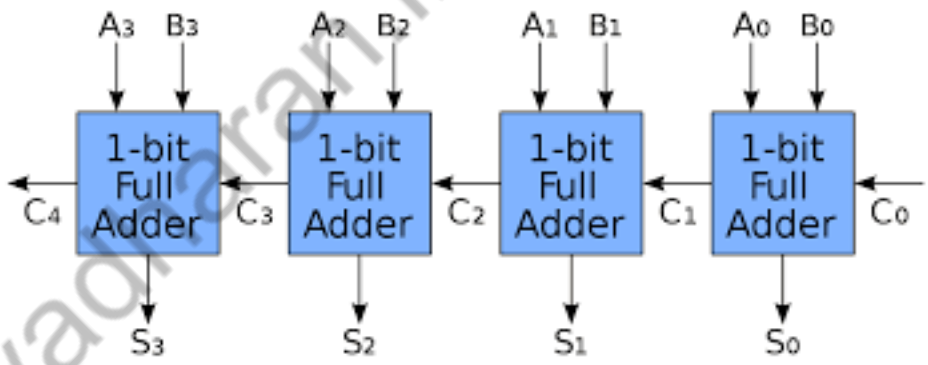
STATIC CMOS



Y'= A(D+E) + BC

Full Adder

Inputs			Outputs	
A	B	C_{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

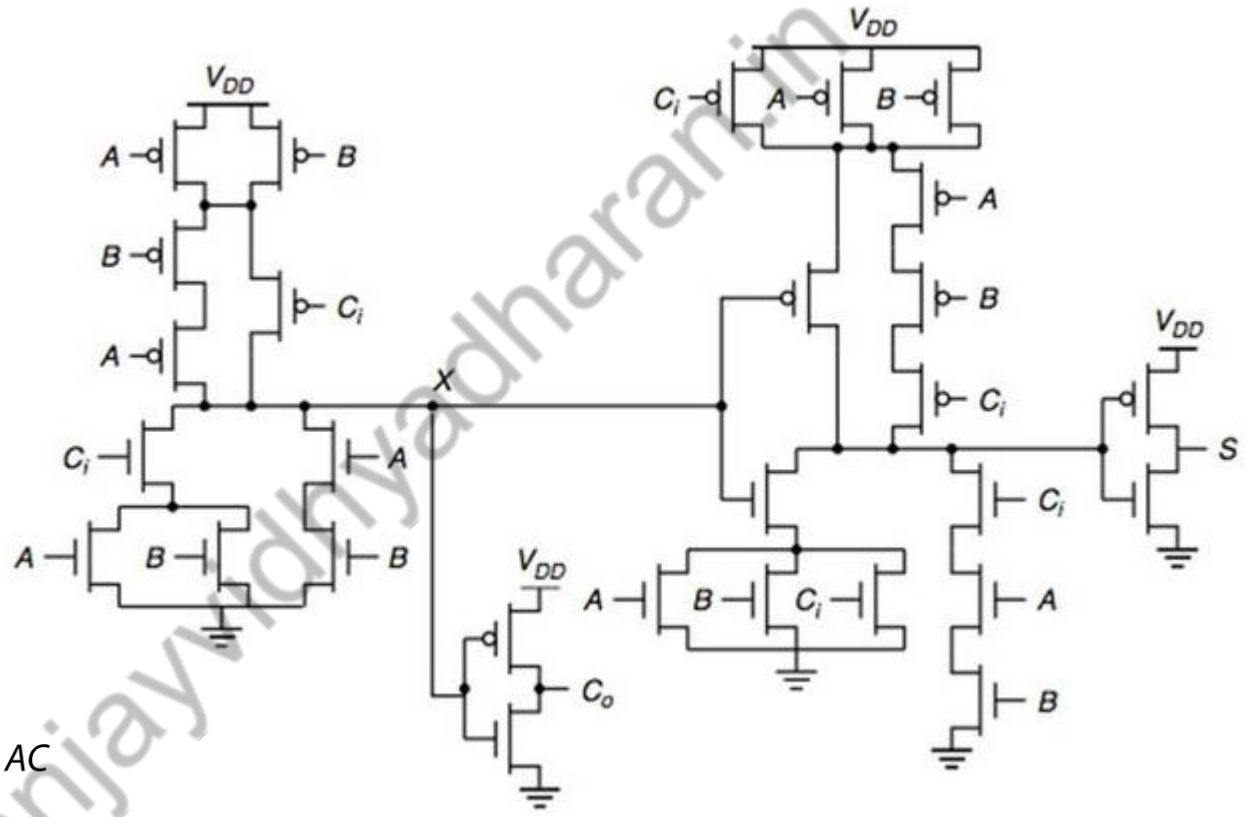


$$Carry(CY) = AB + BC + AC$$

$$Sum(S) = \bar{A}\bar{B}C\bar{B}C + A\bar{B}\bar{C} + \bar{A}B\bar{C} + ABC$$

$$\left.\begin{aligned} CY &= AB + C(A+B) \\ S &= \overline{CY}(A+B+C) + ABC \end{aligned}\right\} \text{Simplified Expressions}$$

Full Adder

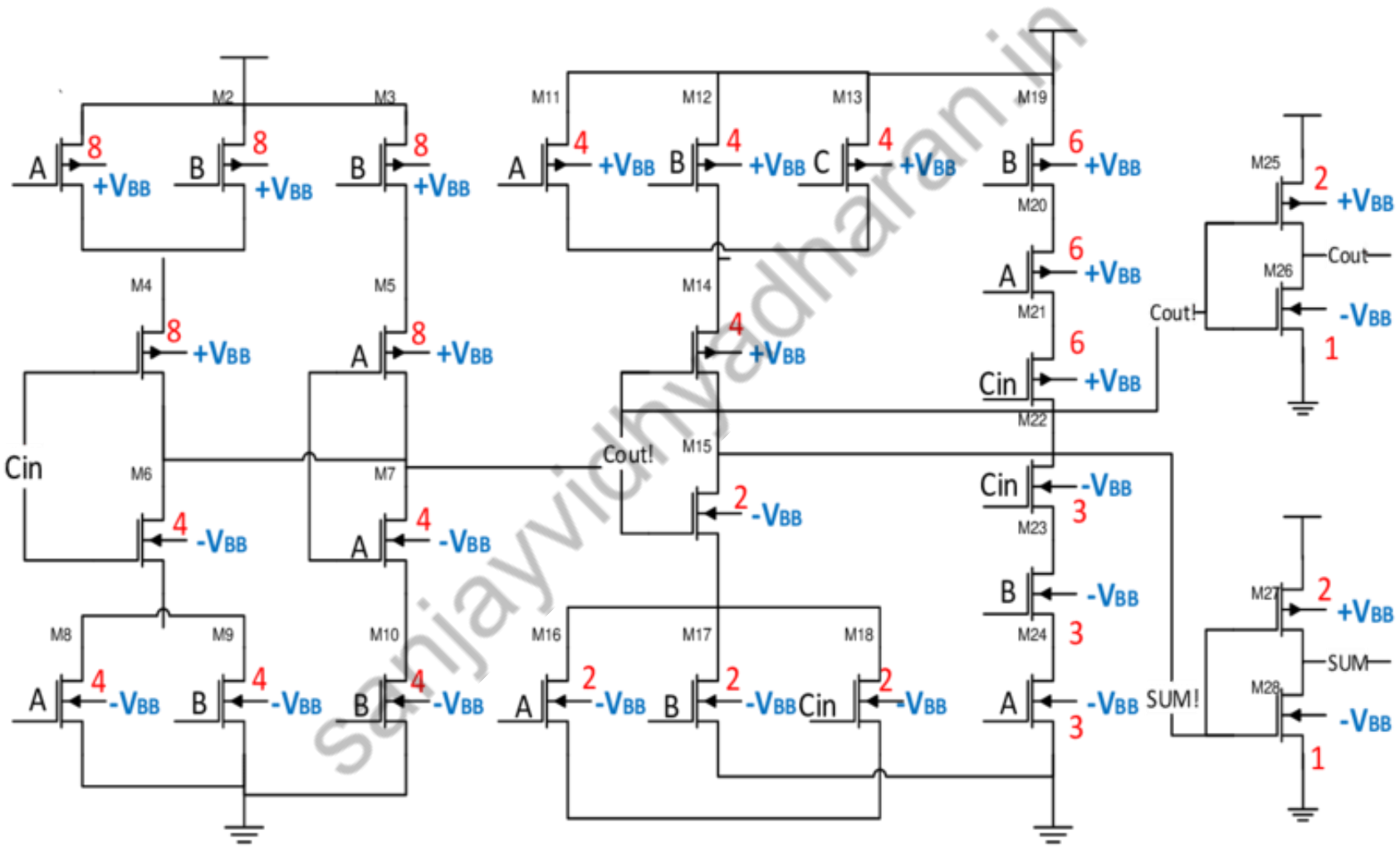


$$Carry(CY) = AB + BC + AC$$

$$Sum(S) = \bar{A}\bar{B}C\bar{B}C + A\bar{B}\bar{C} + \bar{A}B\bar{C} + ABC$$

$$\left.\begin{aligned} CY &= AB + C(A+B) \\ S &= \overline{CY}(A+B+C) + ABC \end{aligned}\right\} \text{Simplified Expressions}$$

Full Adder


M2
M3
M4
M5
M6
M7
M8
M9
M10
M11
M12
M13
M14
M15
M16
M17
M18
M19
M20
M21
M22
M23
M24
M25
M26
M27
M28
A
B
C
Cin
Cout!
SUM!
Cout
SUM
+VBB
-VBB
8
6
4
3
2
1
sanjayvidhyadharan.in

Thankyou