VLSI Design Using LT SPICE

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BITS Pilani

Aim of the Workshop

- **Session 1**
  - **Introduction to CMOS Design**
  - **Importing TSMC 180 nm Technology File in LT SPICE**
  - **NMOS and PMOS Characterization**
- **Session 2**
  - **Inverter Design and Characterization**
    - **Home Assignment : VCO**
- **Session 3**
  - **Static CMOS Design: Full Adder Design**
    - **Home Assignment : SR Latch**
- **Session 4**
  - **Dynamic CMOS Design: Dynamic Full Adder Design**
    - **Home Assignment : D-Flip Flop**

Aim of the Workshop

- **Session 5**
  - **Pass Transistor Logic: PTL Full Adder Design**
    - **Home Assignment : Multiplexer Design**
- **Session 6**
  - **Memory Design : 6T SRAM**
    - **Home Assignment : 4T / 7T SRAM , DRAM**

History of CMOS

- **Original idea of a FET introduced by Julius Lilienfield in the year of 1925**
- **A structure closely reassembling the MOSFET was proposed in 1935 by Oskar Heil**
- **In 1960s MOSFETs began to enter production**
- **In 1963 Fairchild company produces gates using both nMOS and pMOS transistor → earning the name CMOS**
- **CMOS circuits consumed only nanowatts of power → six order of magnitude less than their bipolar counterparts.**

Pentium

1993 : Technology : 0.8 μm (16.7 mm by 17.6 mm)

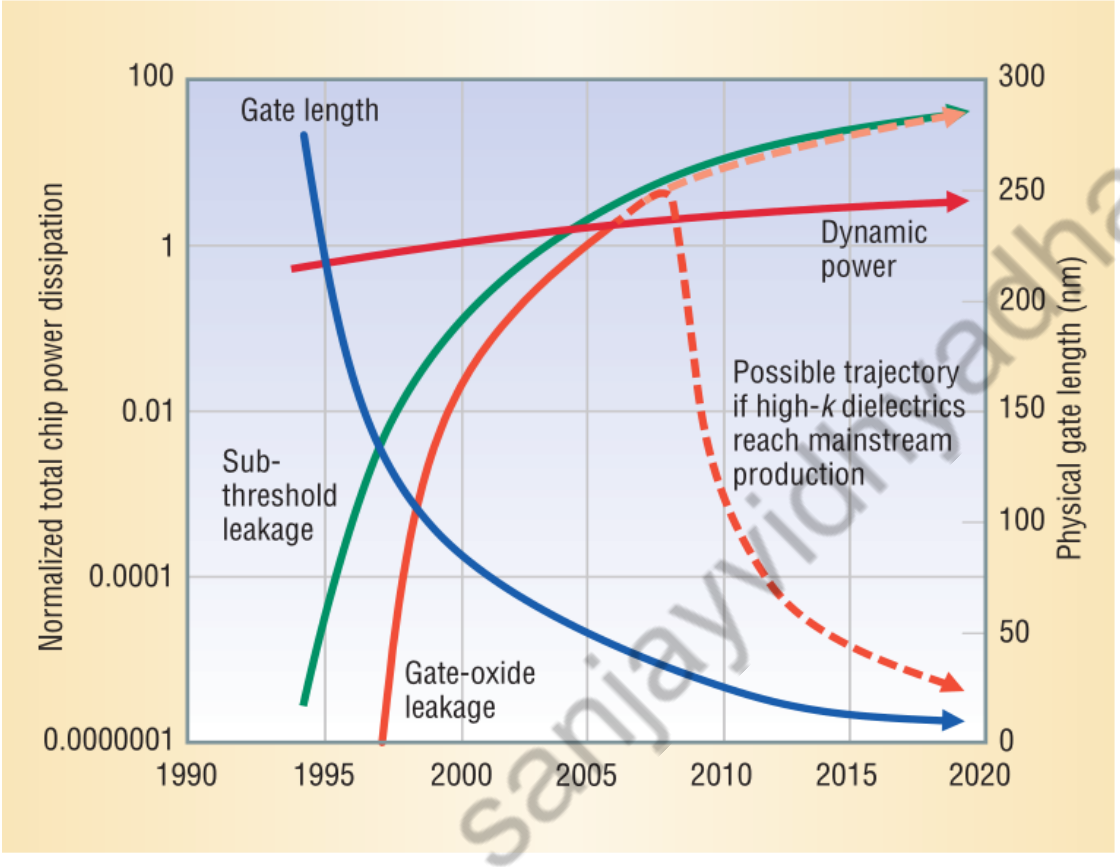
Latest CPUs and GPUs

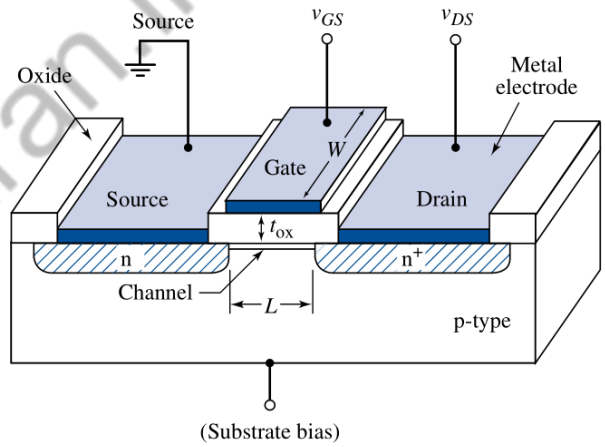
Latest Trends :- Intel : 14 nm AMD : 7nm

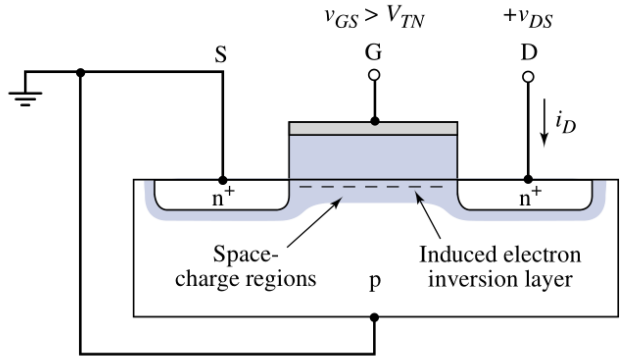
- Billions of Transistors/ Chip
- Frequency of Operation in GHz
- Complex Computational Capability

Limitations of CMOS Technology

ITRS Prediction of Power Consumption



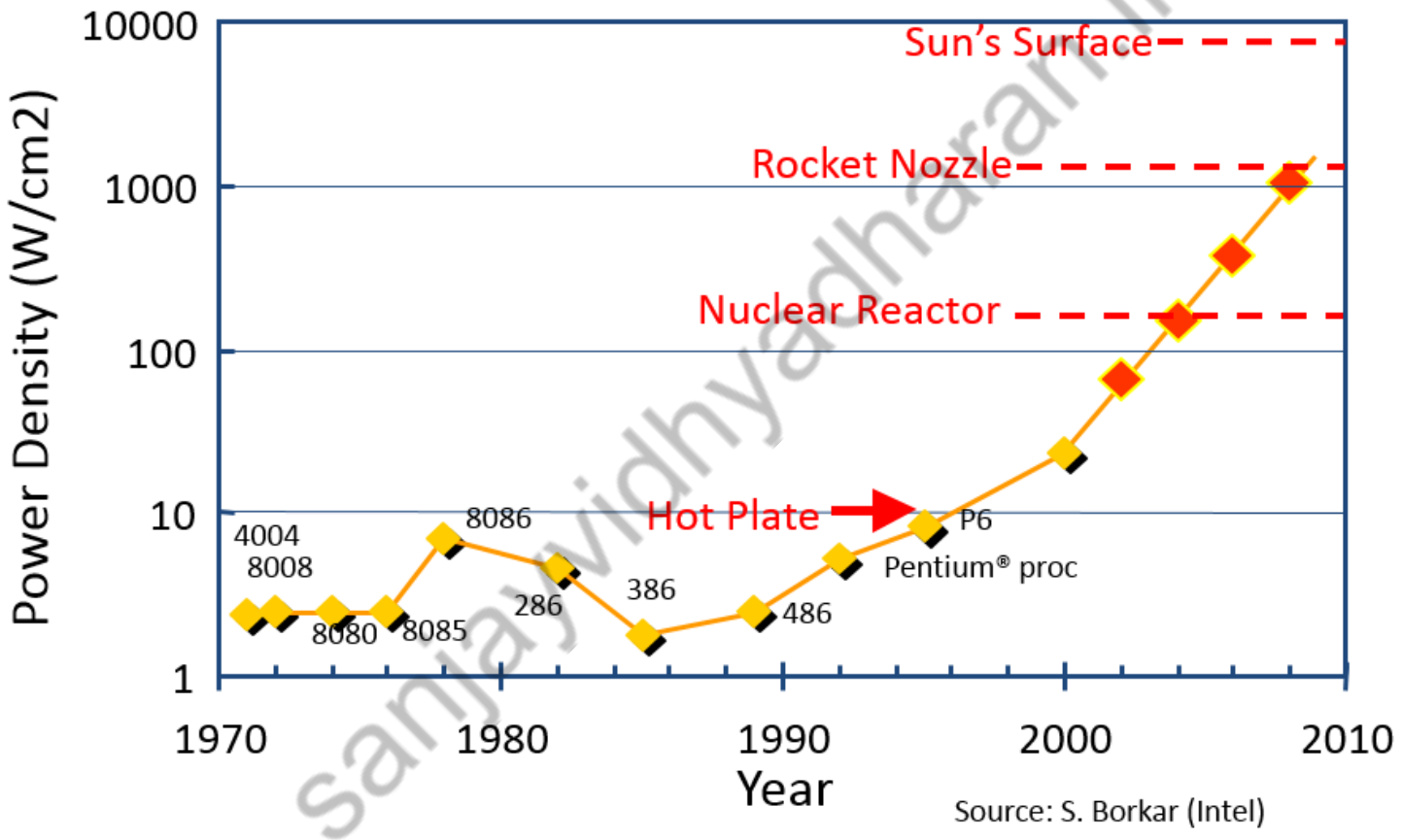




[1] Semiconductor Industry Assoc., International Technology Roadmap for Semiconductors, 2002 Update; http://public.itrs.net.

Limitations of CMOS Technology

Intel's Prediction of Power Consumption

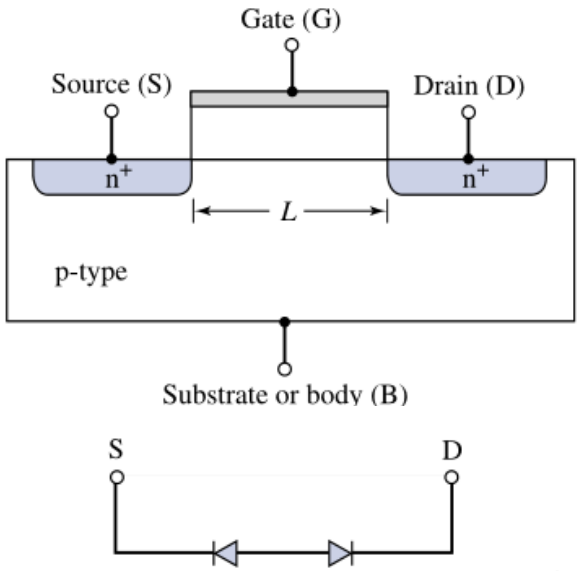


[2] Online Available: http://computerscience.chemeketa.edu/cs160Reader/Parallel Processing/MooresLaw.html

MOSFET OPERATION AS SWITCH

NMOSFET

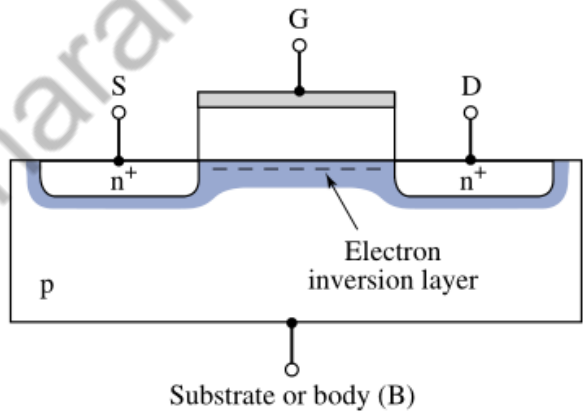
Switch OFF



I_{OFF}
Ideal = 0 Practically in pico amperes

R_{OFF}
Ideal = ∞ Practically in Mega/Giga Ohms

Switch ON

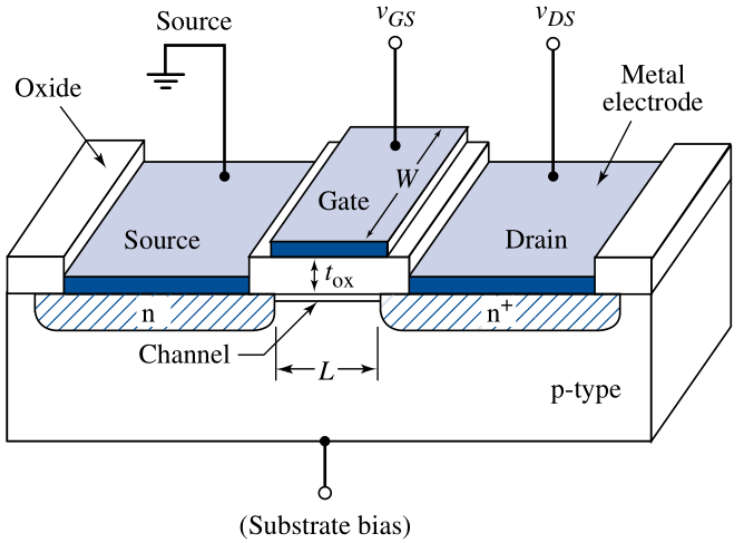


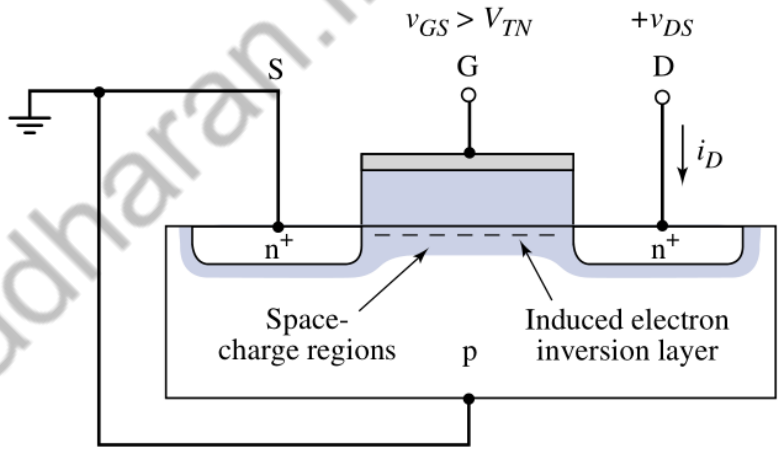
I_{ON}
Ideal = ∞ Practically in micro amperes

R_{ON}
Ideal = 0 Practically in few Ohms

MOSFET REGION OF OPERATION

NMOSFET

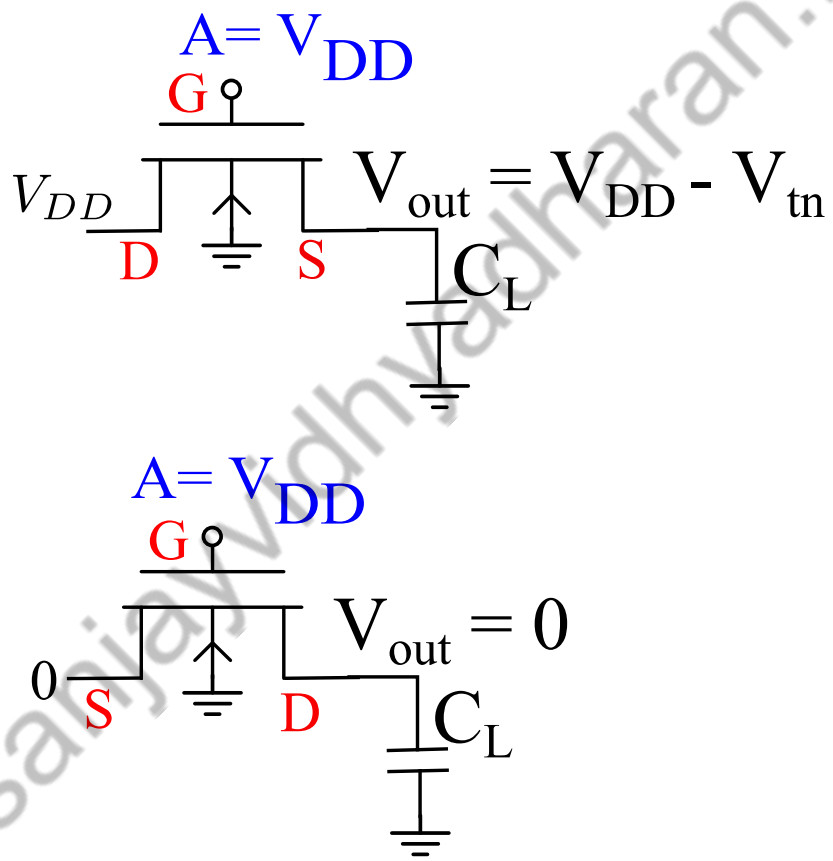




Cut Off	$V_{GS} \le V_T$	$I_{DS} = 0$
Linear	$V_{GS} > V_T$, $V_{DS} \le V_{GS} - V_T$	$I_{DS} = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$
Saturation	$V_{GS} > V_T$, $V_{DS} > V_{GS} - V_T$	$I_{DS} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T)^2$

MOSFET OPERATION AS SWITCH

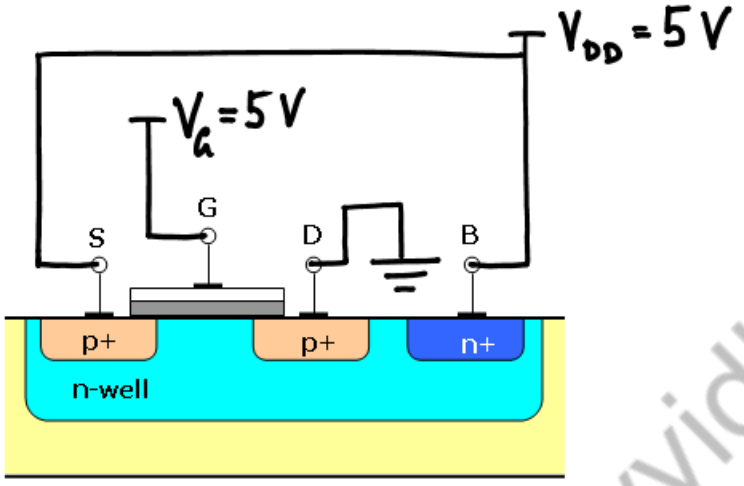
NMOSFET AS SWITCH

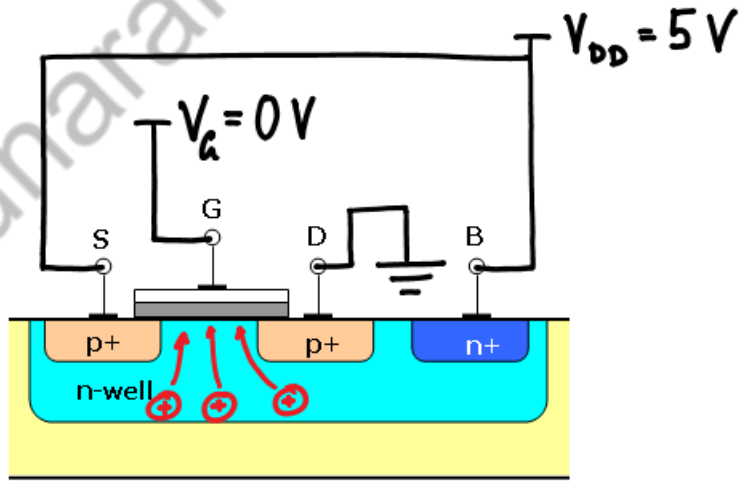


- NMOS can pass perfect 0 but not 1

MOSFET OPERATION AS SWITCH

PMOSFET





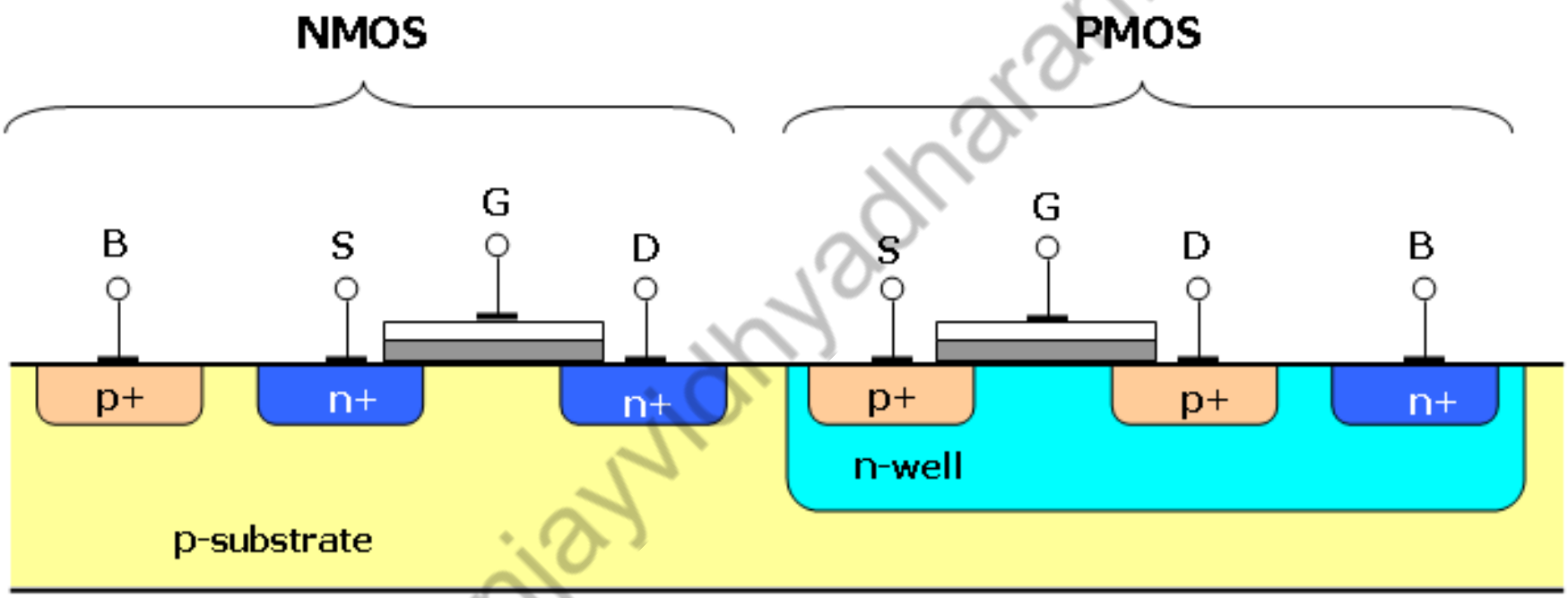
I_{OFF}
Ideal = 0 Practically in pico amperes

R_{OFF}
Ideal = ∞ Practically in Mega Ohms

I_{ON}
Ideal = ∞ Practically in micro amperes

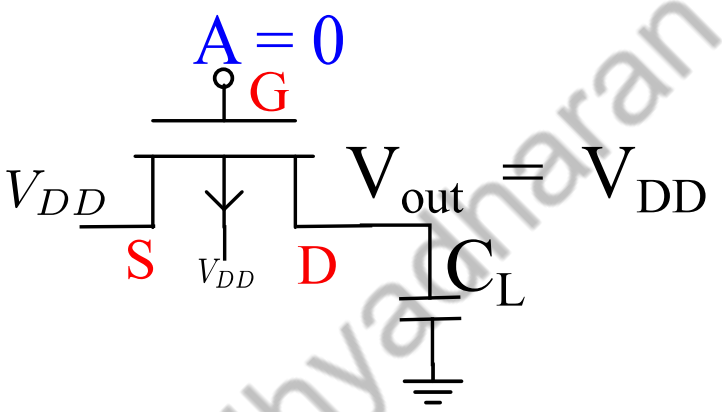
R_{ON}
Ideal = 0 Practically in few Ohm

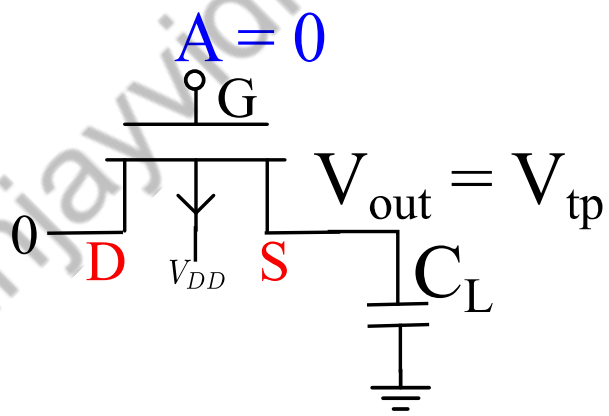
MOSFET OPERATION AS SWITCH



MOSFET OPERATION AS SWITCH

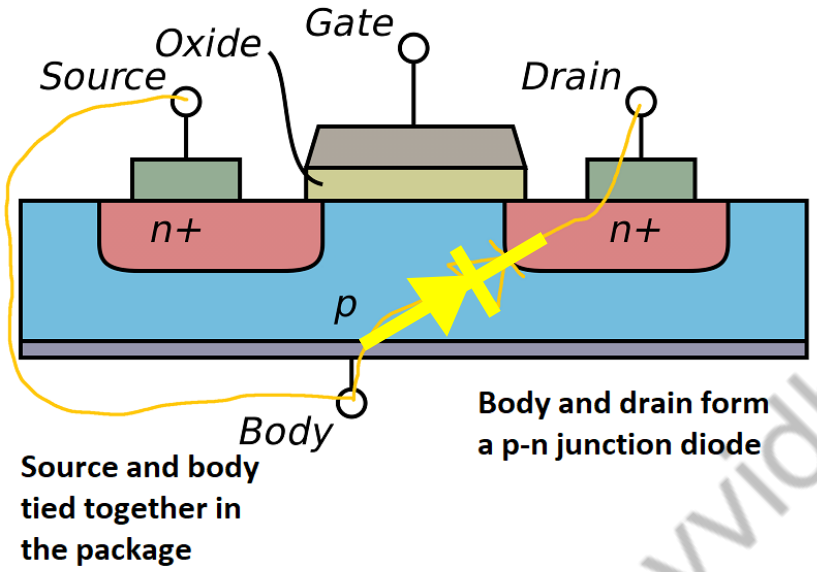
PMOSFET AS SWITCH

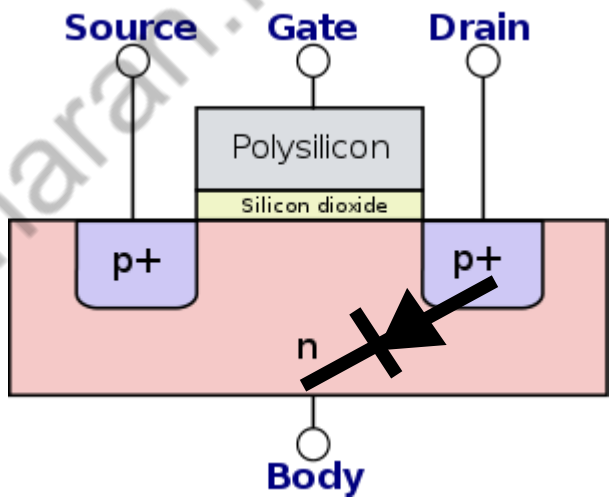




- PMOS pass perfect 1 but not 0

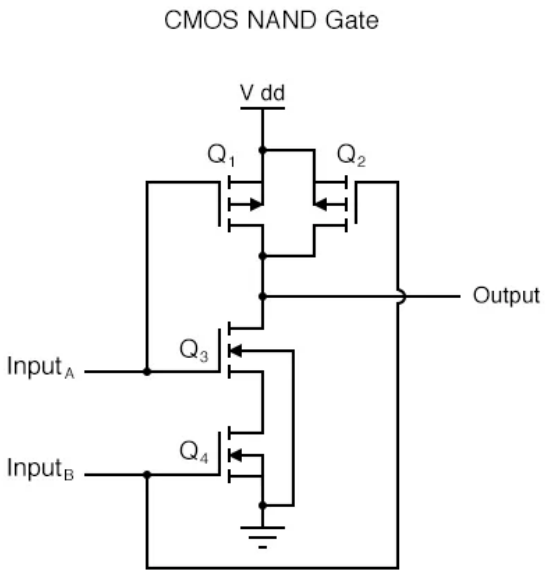
MOSFET BODY CONNECTION

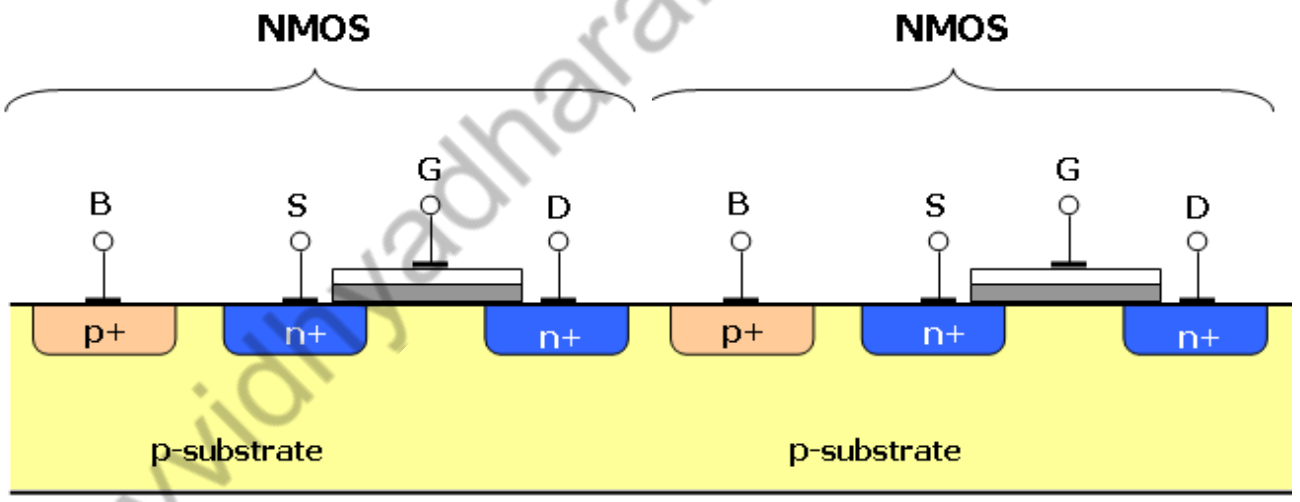




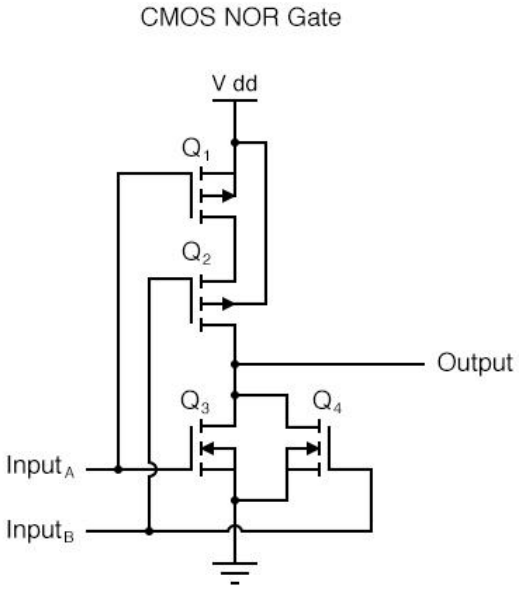
- NMOS Body to Lowest Possible Potential (Gnd)
- PMOS Body to Highest Possible Potential (V_{DD})

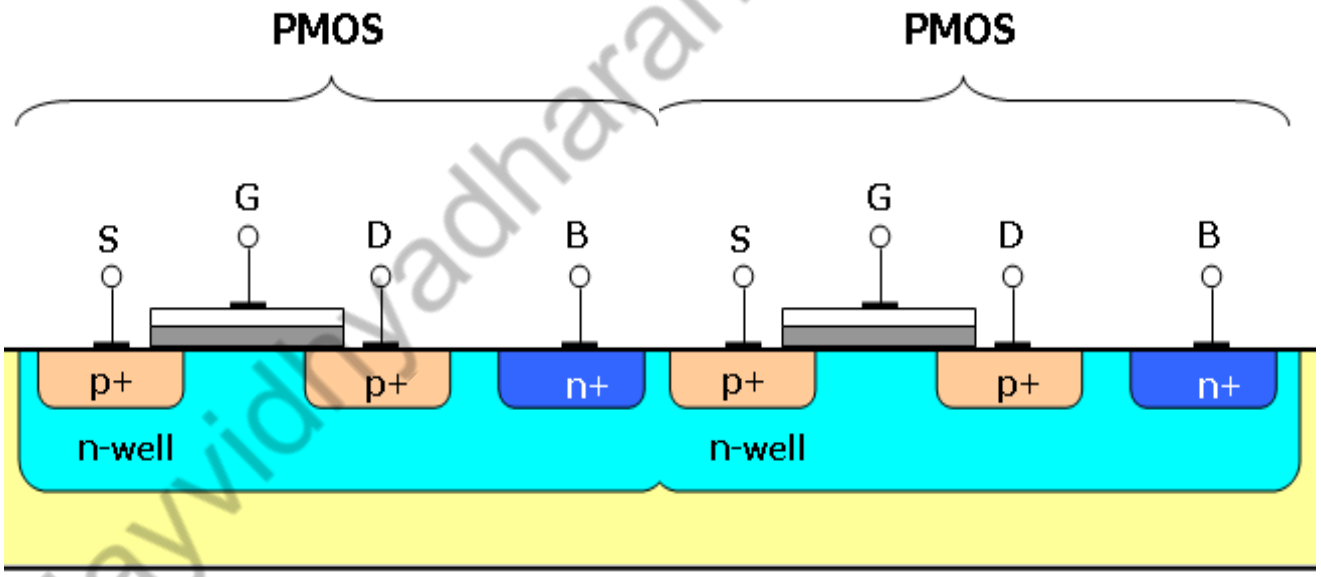
MOSFET BODY CONNECTION



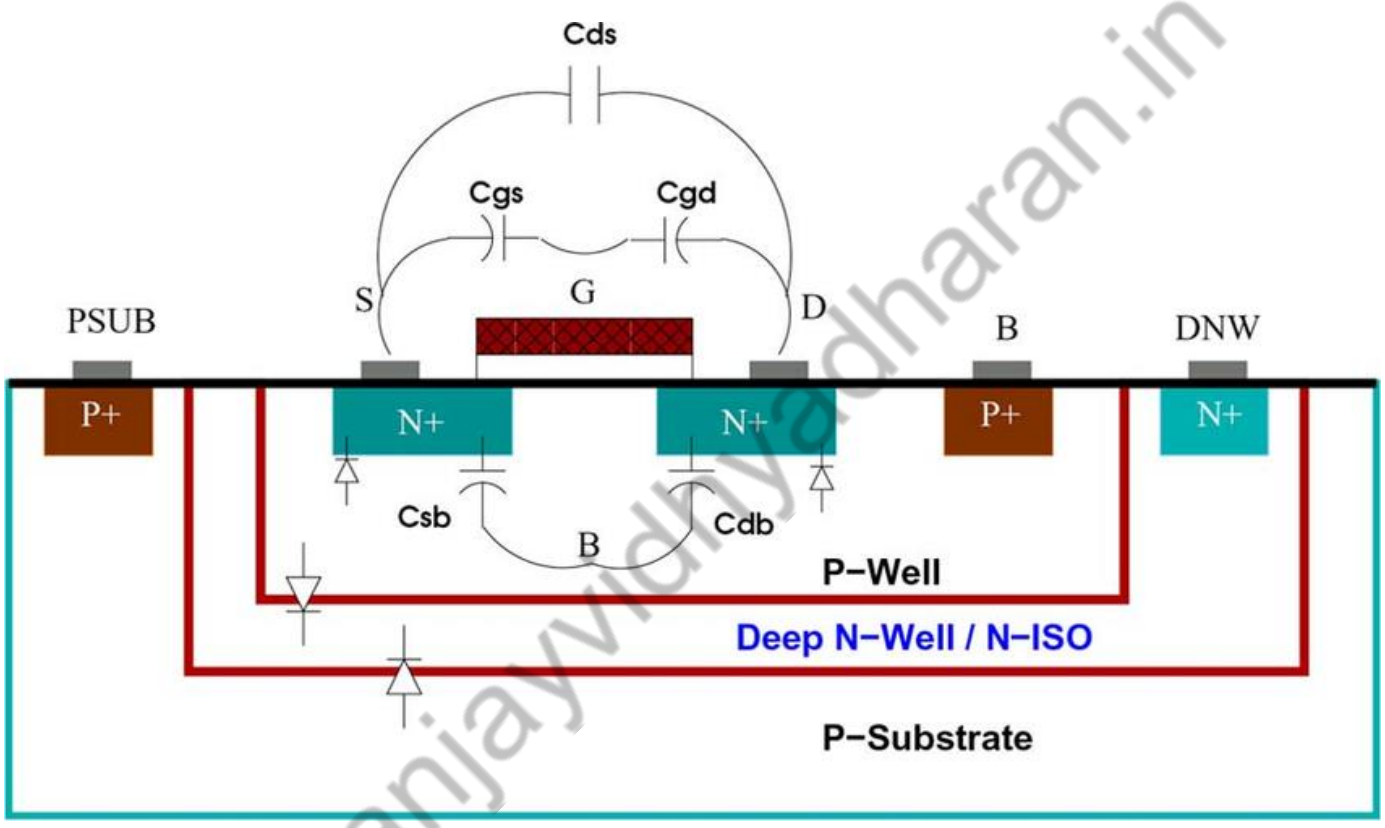


MOSFET BODY CONNECTION



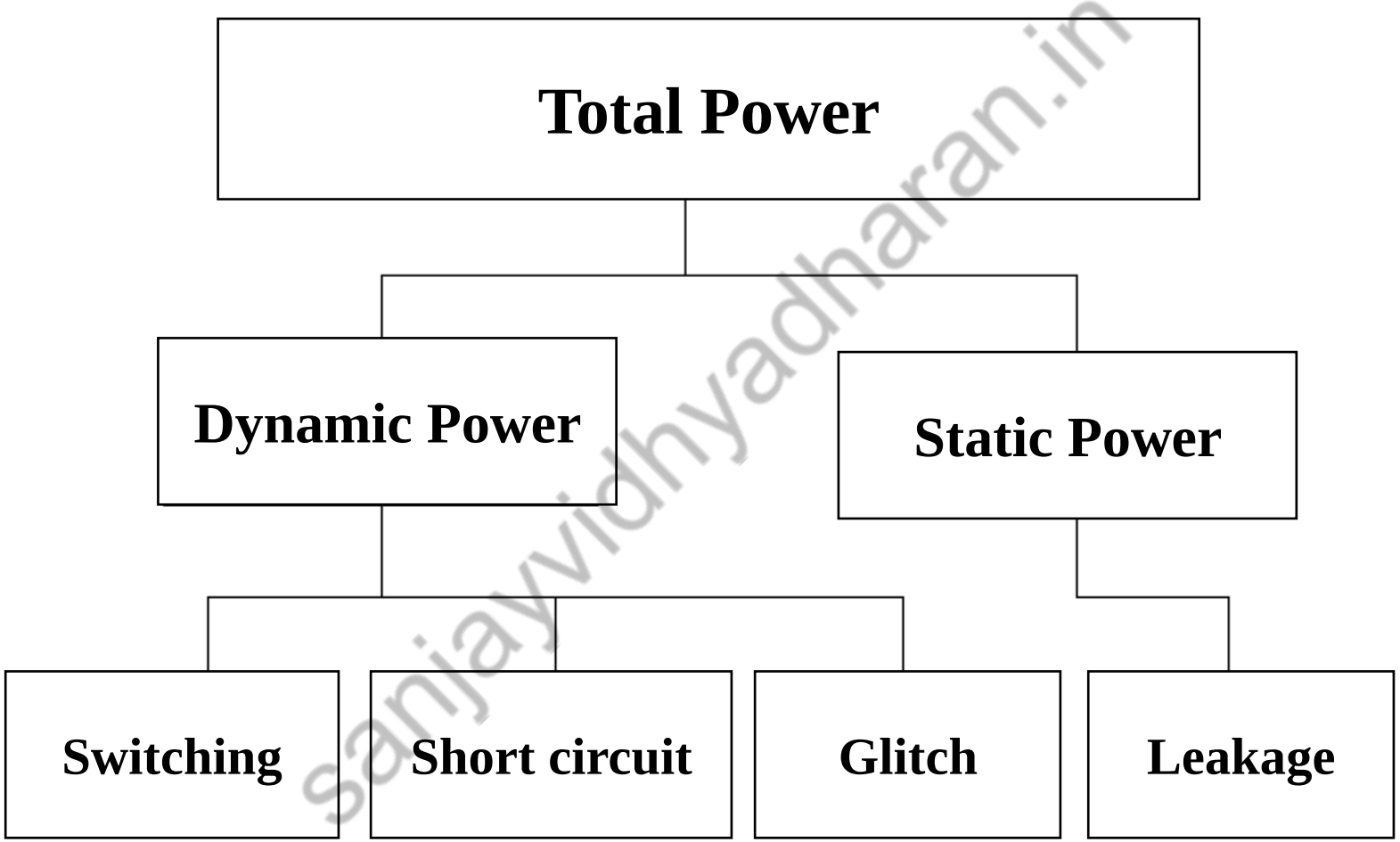


MOSFET BODY CONNECTION

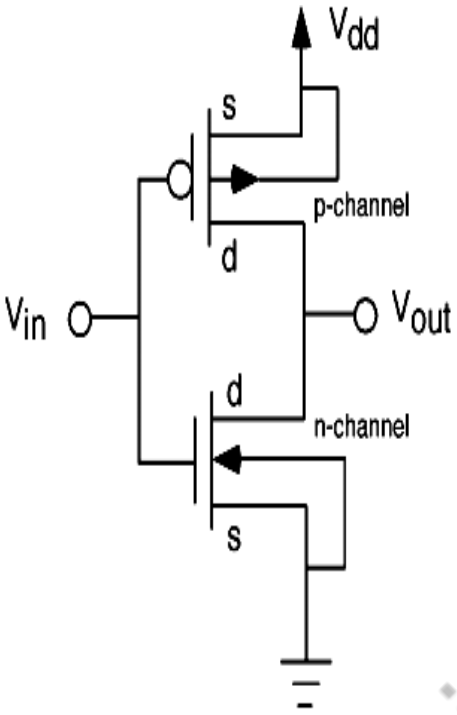


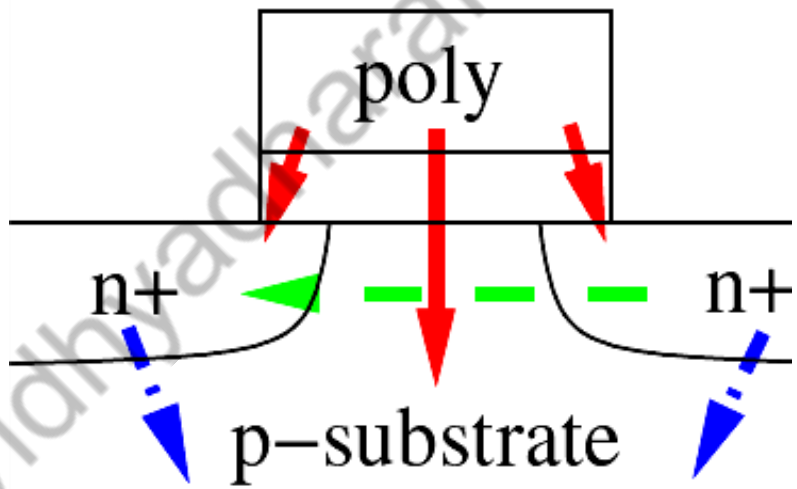
- MOS Double well : Body not same as Substrate

Power Dissipation in CMOS Circuits



Static Loss





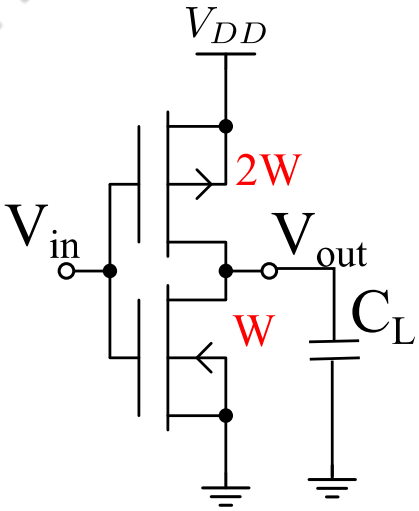
Static Power Dissipation in CMOS

Static Loss

➢ Causes for High Static Power Consumption

Effect of Decreasing V_{DD} on Delay

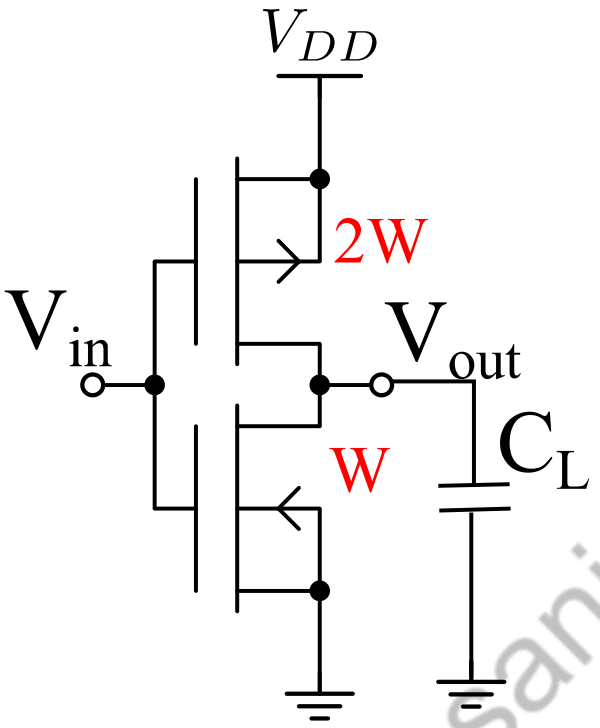
$$Propagation\ Delay\ (tpd) = \frac{K_1 C_L}{I_D} = \frac{K_2 C_L}{(V_{DD} - V_{th})^2}$$

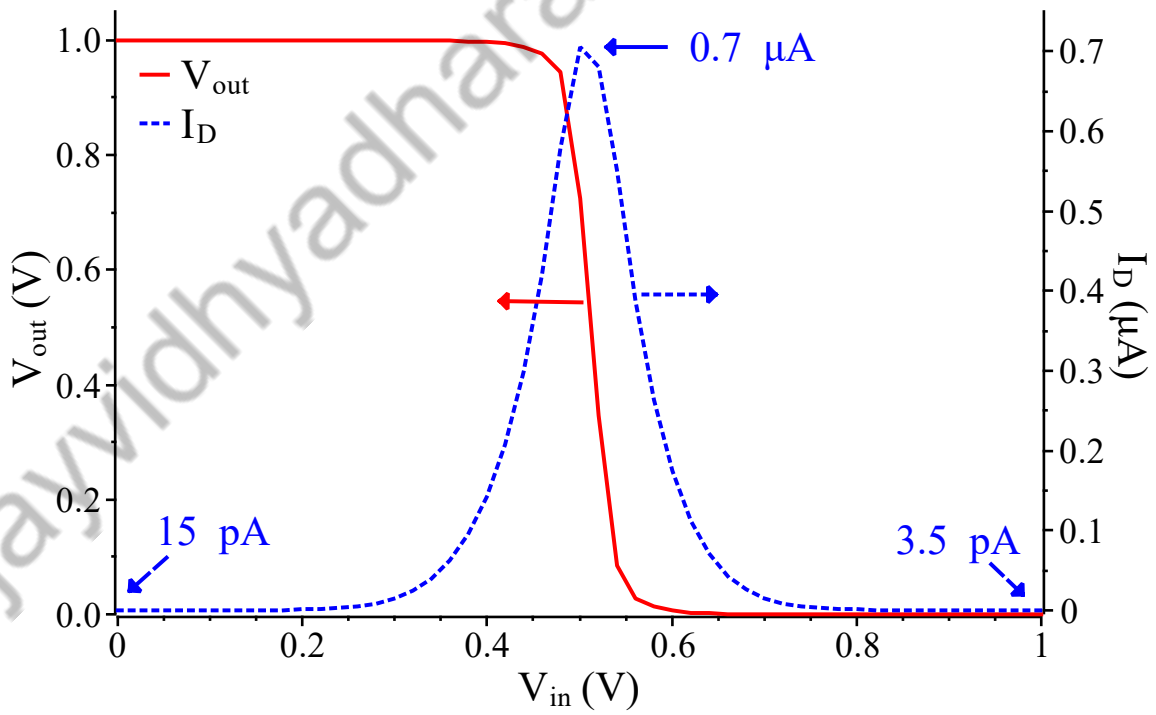


Effect of Decreasing V_{th} on Power

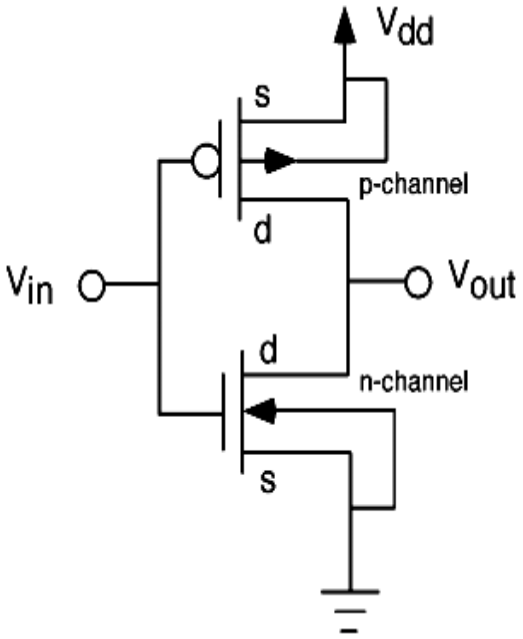
- Intel estimated leakage power consumption at more than 50W for a 100nm technology node.
- Leakage depends strongly on a Threshold voltage (V_{th}) of the transistor

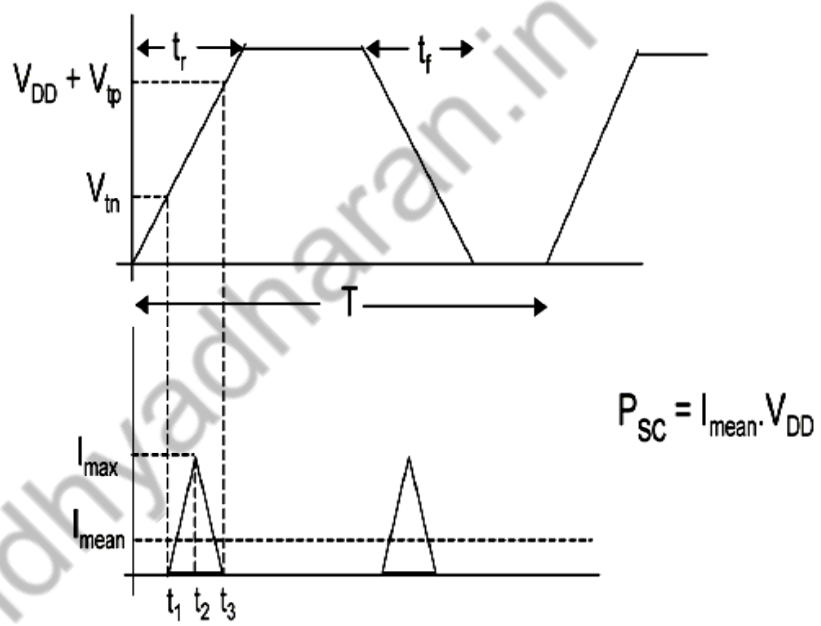
Static Loss





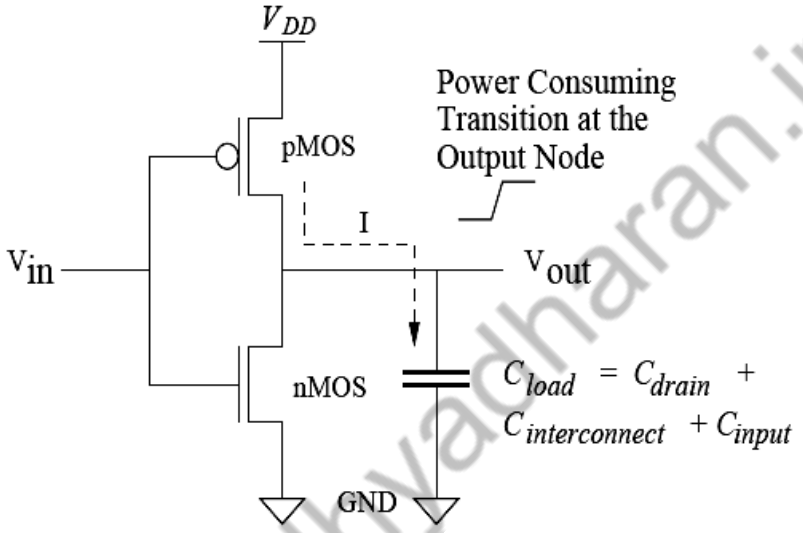
Short Circuit Loss





- Use devices with V_{th} close to $\frac{V_{DD}}{2}$ & steep switching characteristics
- Short Circuit loss reduces with C_{load}

Switching Loss



Energy stored in C_{Load} $(C_L) = \int_0^{V_{DD}} V_C \, C_L dV_c = \frac{1}{2}.V_{DD}^2 * C_L$

Energy consumed from power supply= $V_{DD} \int_0^T i(t)dt = V_{DD}.Q_{CL} = V_{DD}^2.C_L$

Energy dissipated in pMOSFET during charging = $\frac{1}{2}.V_{DD}^2.C_L$

Energy dissipated in nMOSFET during discharging = $\frac{1}{2}.V_{DD}^2.C_L$

Power Consumption = Frquency.$V_{DD}^2.C_L$

High Dynamic Power Consumption

$$P_{Dynamic} = Freq * V_{DD}^2 * C_L$$

- V_{DD} & C_L : Reduced by 30 % each generation
- Frequency : 43 % Increase
  - Architectural optimizations
  - Consumer requirements
- Transistors per chip : Increased exponentially
  - Advancement in lithography
  - Multilayer metallization
  - Efficient partitioning and routing techniques

Figure of Merits of a Digital Circuit

1. Noise Margin

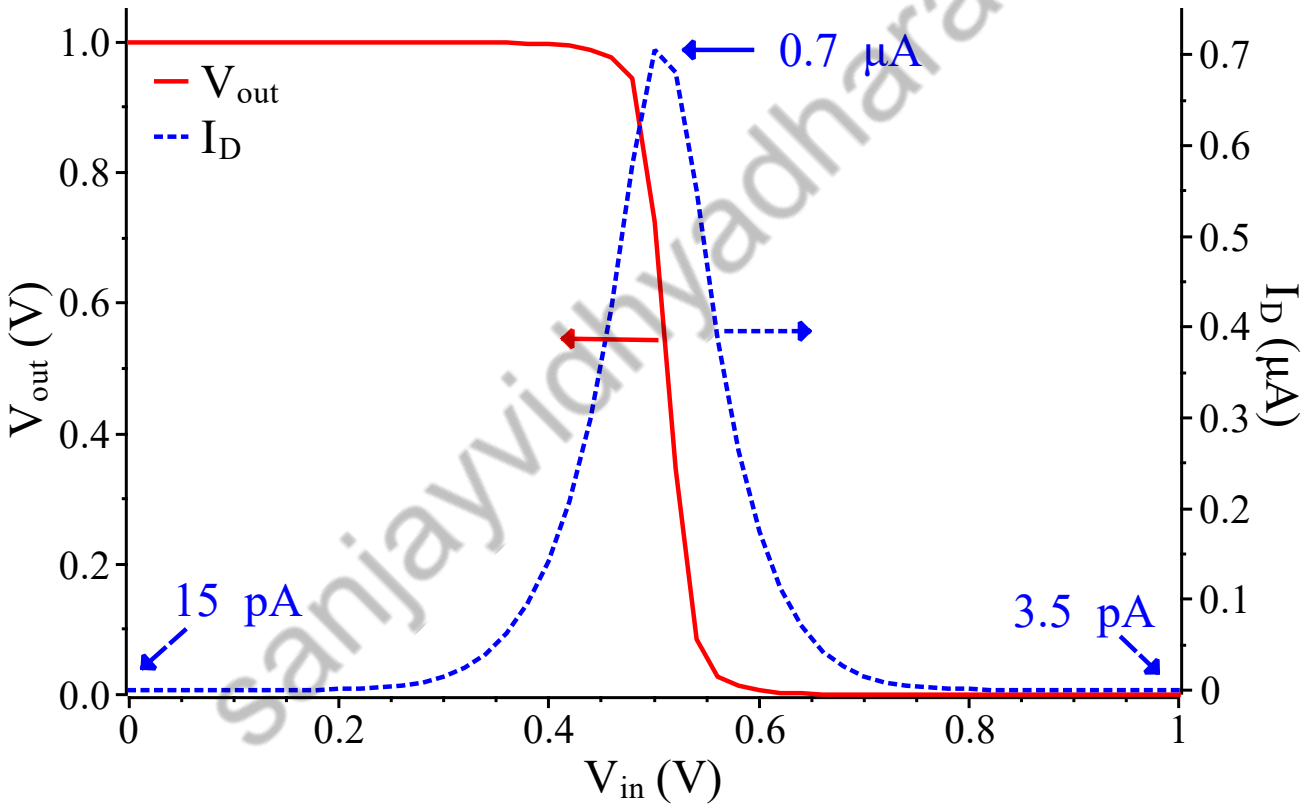


Figure of Merits of a Digital Circuit

2. Propagation Delay (Eg. Inverter)

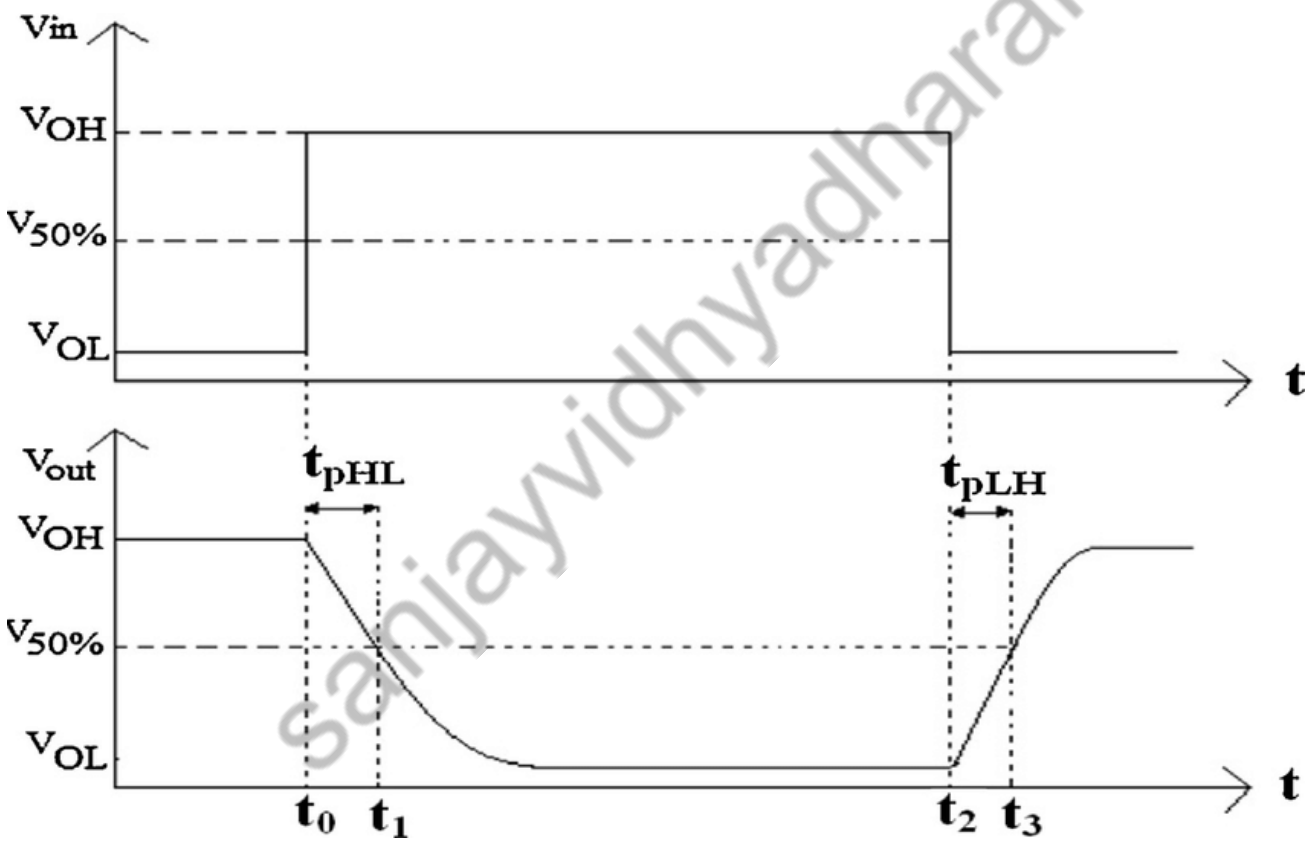


Figure of Merits of a Digital Circuit

3. Rise Time and Fall Time

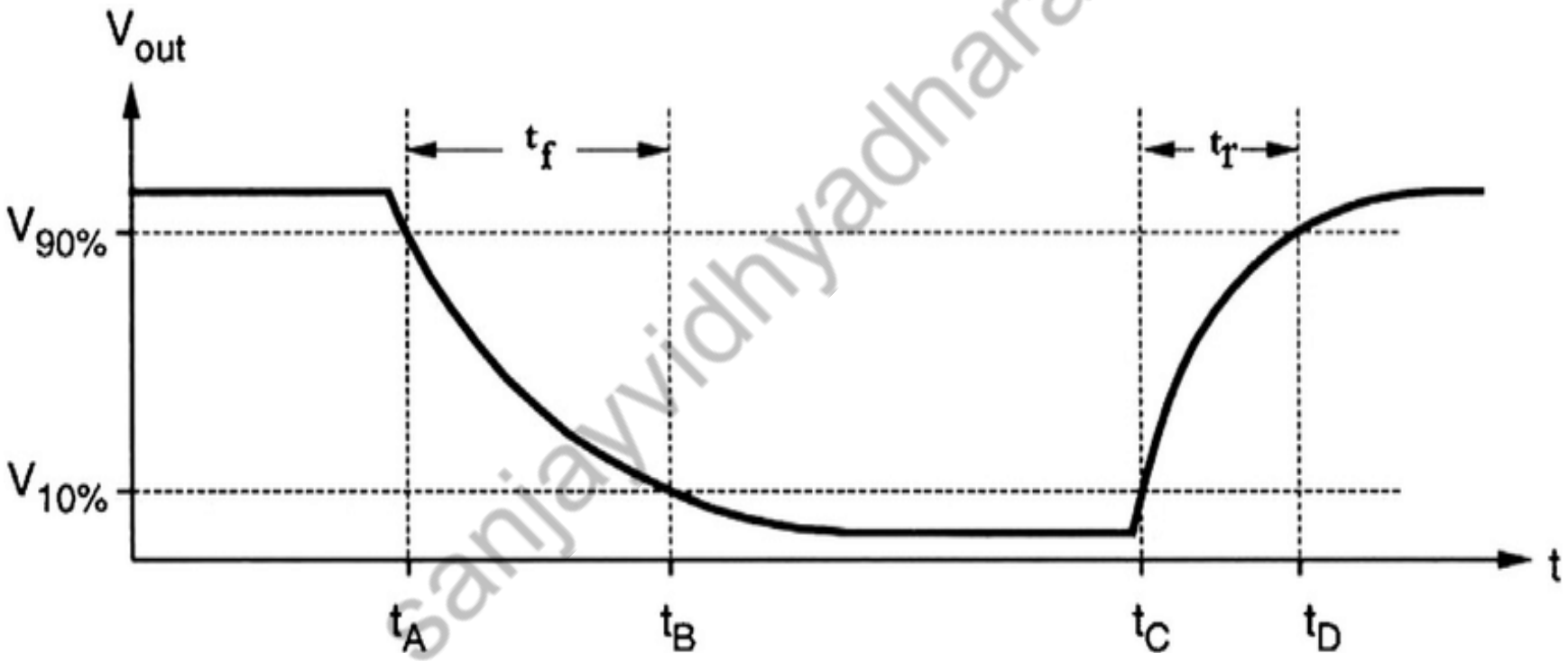
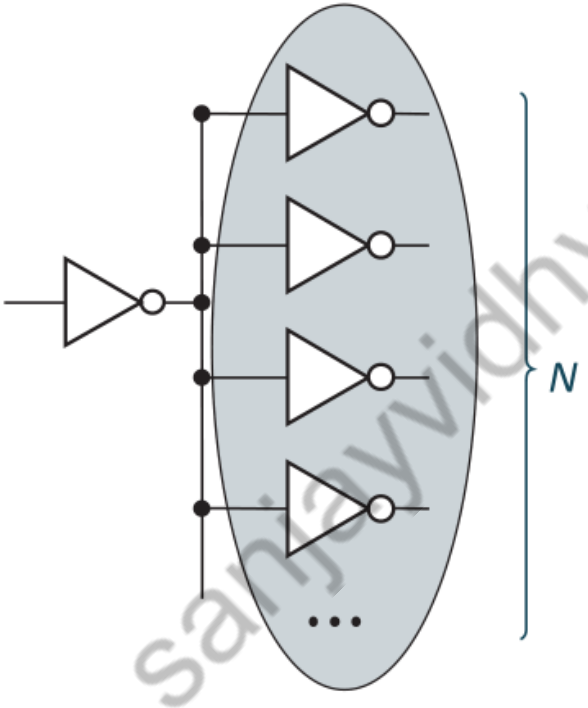
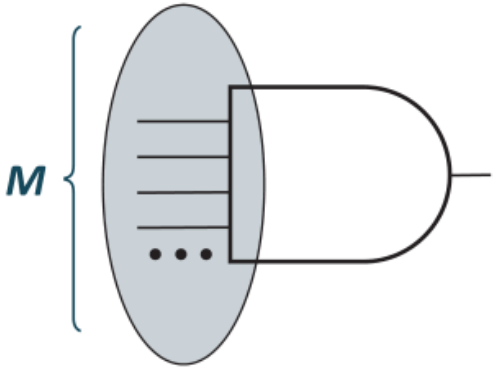


Figure of Merits of a Digital Circuit

4. Fan-in and Fan-Out



Fan-out *N*



Fan-in *M*

Figure of Merits of a Digital Circuit

5. Power and Energy Consumption

- **Power consumption of design determine**
  - How much energy is consumed per operation
  - How much heat the circuit dissipates

- **Determine critical design decision**
  - Power supply capacity, battery lifetime,
  - Supply line sizing, packaging and cooling

- **Peak power is important for supply line sizing**

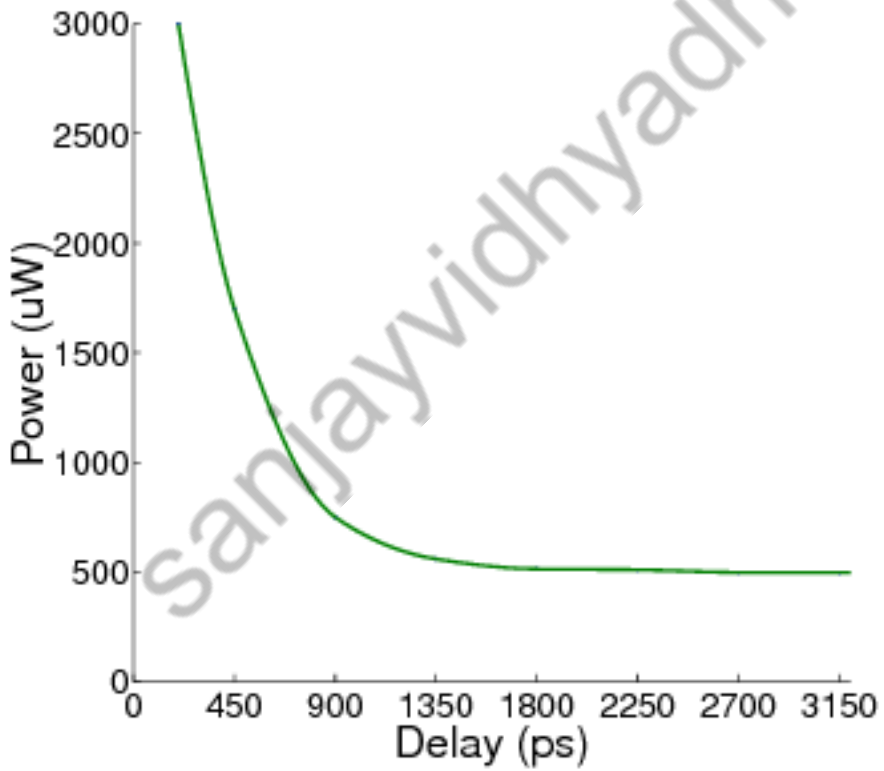
- **Average power dissipation is important for cooling or battery requirements**

Figure of Merits of a Digital Circuit

6. Power Delay Product

$P_{Dynamic} = Freq * V_{DD}^2 * C_L$

$$Propagation\ Delay\ (tpd) = \frac{K_1 C_L}{I_D} = \frac{K_2 C_L}{(V_{DD} - V_{th})^2}$$



Thankyou