# Digital Design : 2021-22
# Lecture 11 : Logic Gate Realization

**By Dr. Sanjay Vidhyadharan**

# NAND-NOR Implementations

NAND gate and NOR gates are called Universal gates

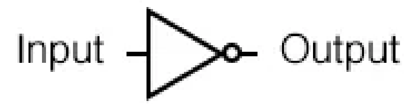
Any logic can be implemented using NAND/NOR gates

In CMOS NAND and NOR gates are basic gates

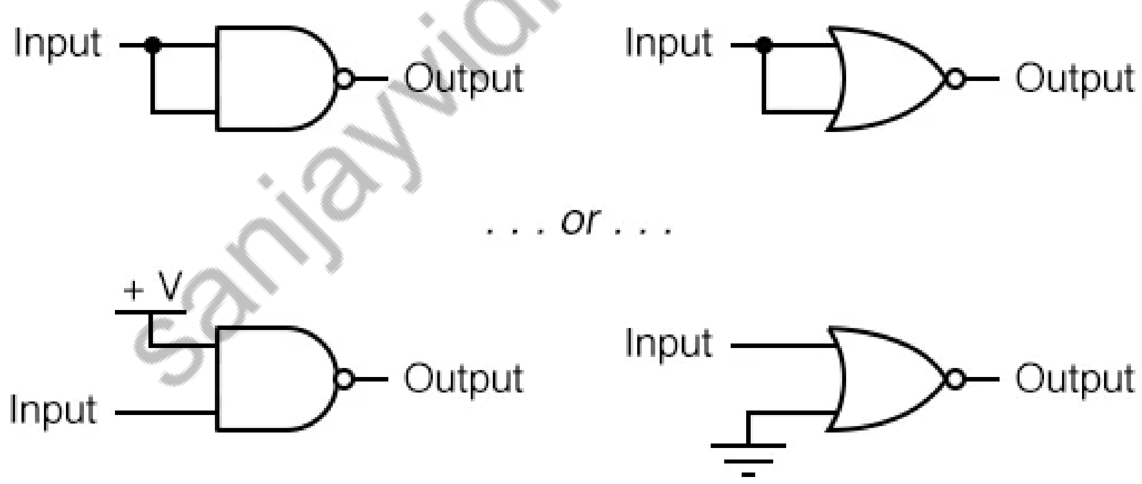
AND gate is realized by using NAND gate with Inverter

OR gate is realized by using NOR gate with Inverter

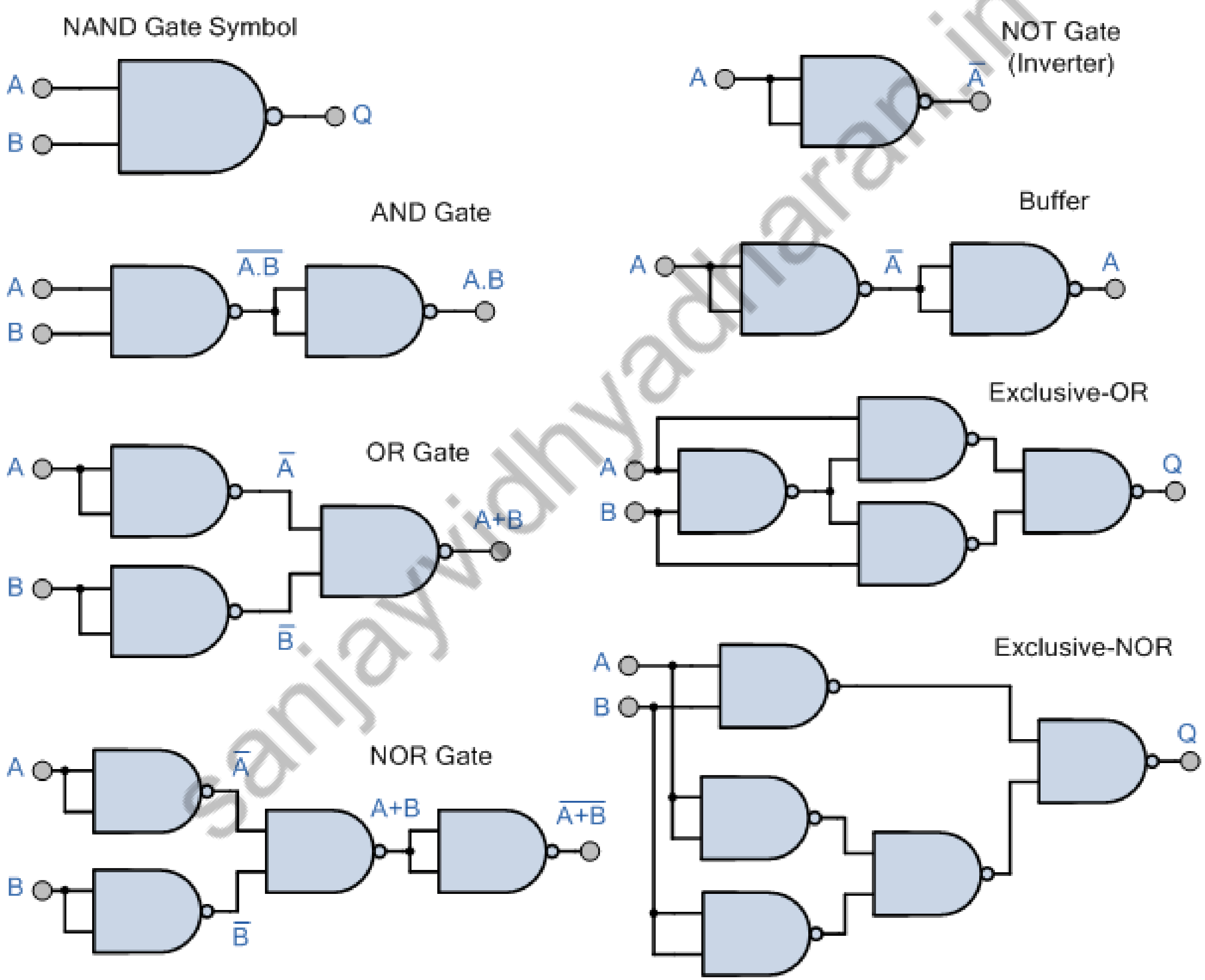
# NAND-NOR Implementations



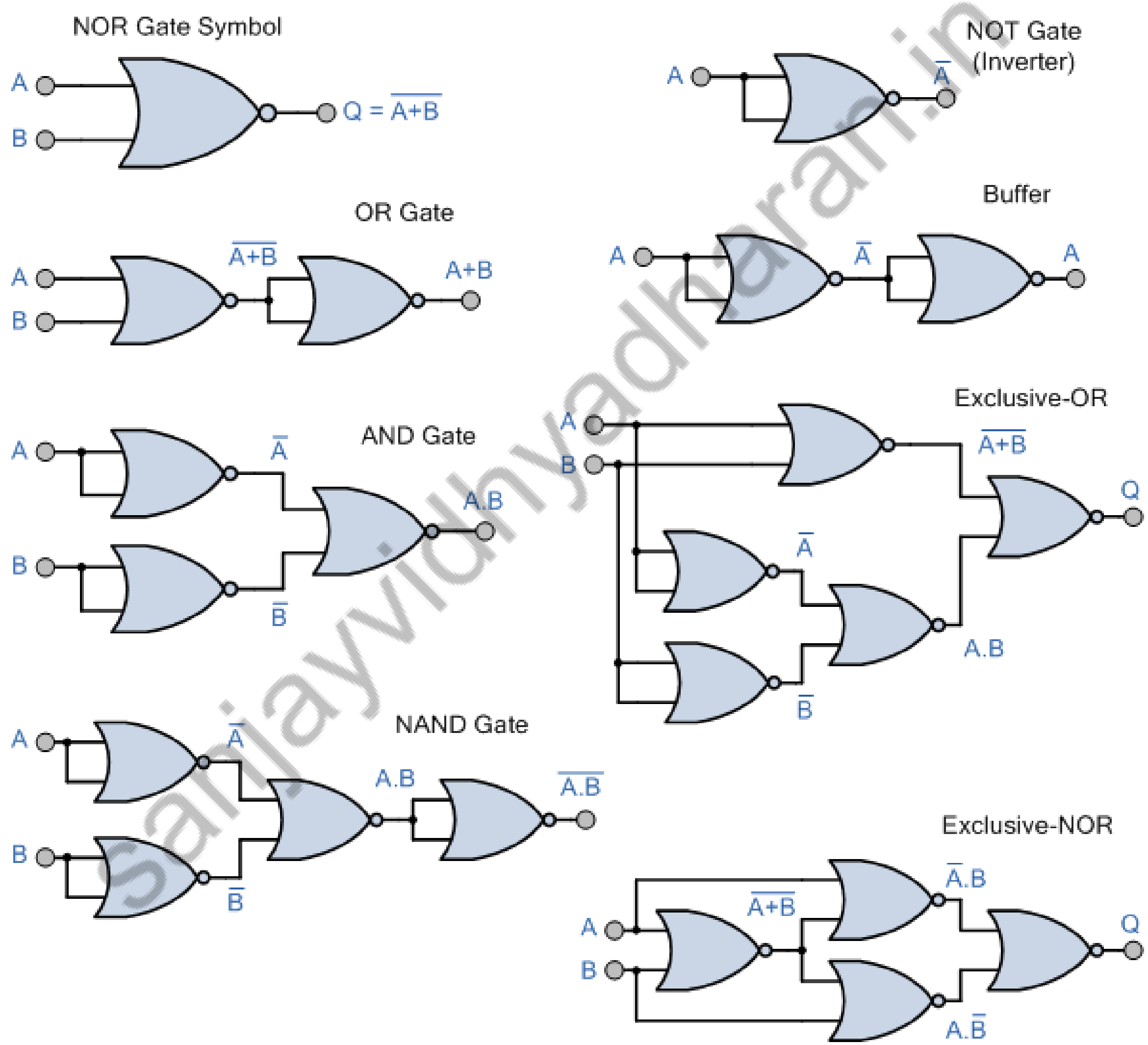

| Input | Output |
|---|---|
| 0 | 1 |
| 1 | 0 |



# NAND Implementations

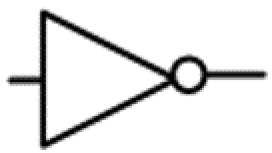
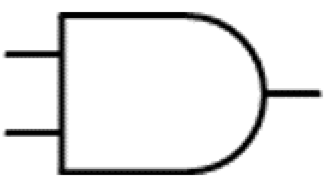
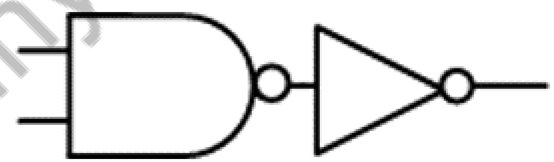
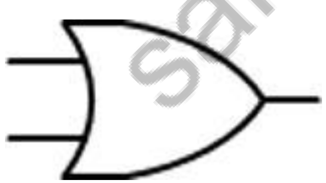
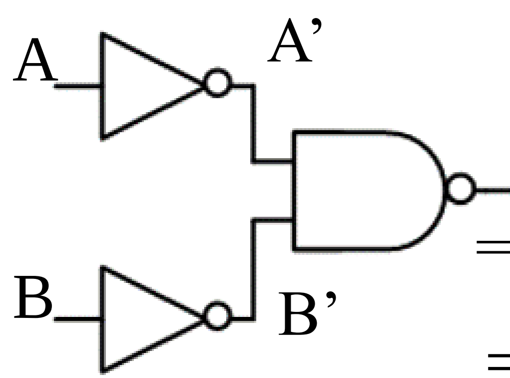


# NOR Implementations



# NAND Implementation



| Gate | NAND Implementation |
| --- | --- |
|  |  |
|  |  |
|  |  |



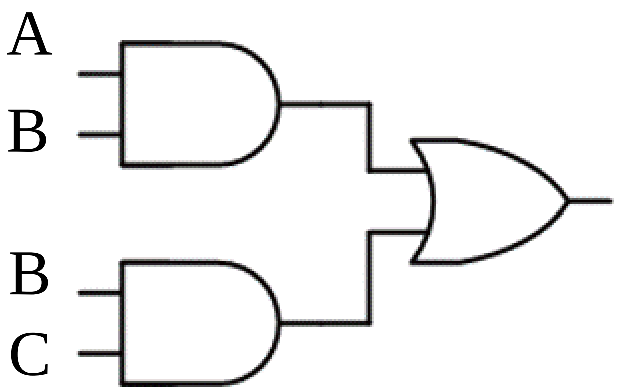
(A'B')'

= (A')' + (B')'

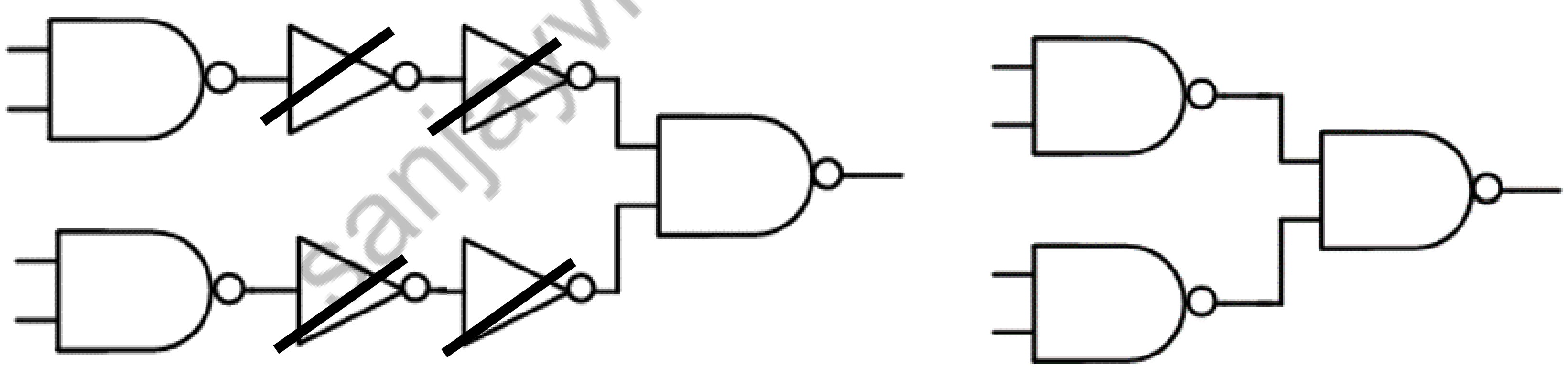
= A + B

# NAND Implementation

AB + BC

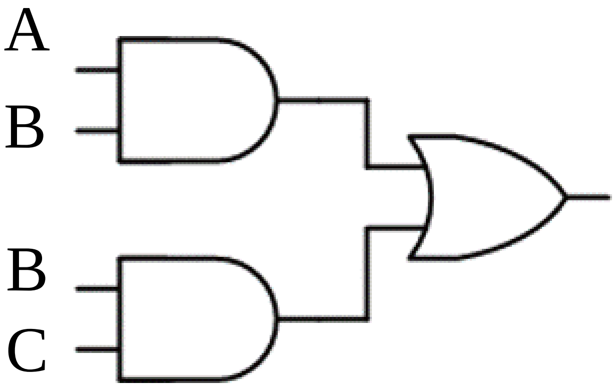


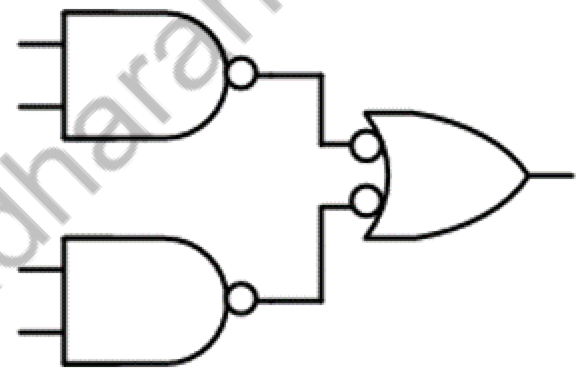

Replace each gate by its corresponding NAND realization

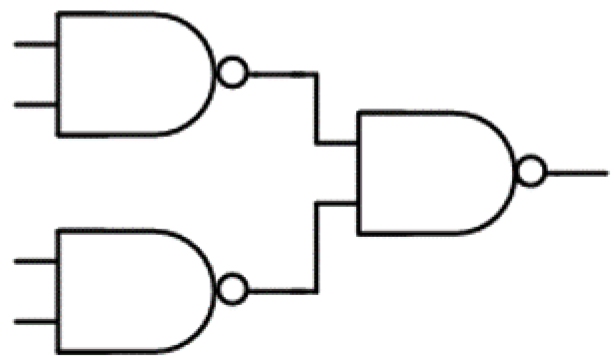


# NAND Implementation

AB + BC

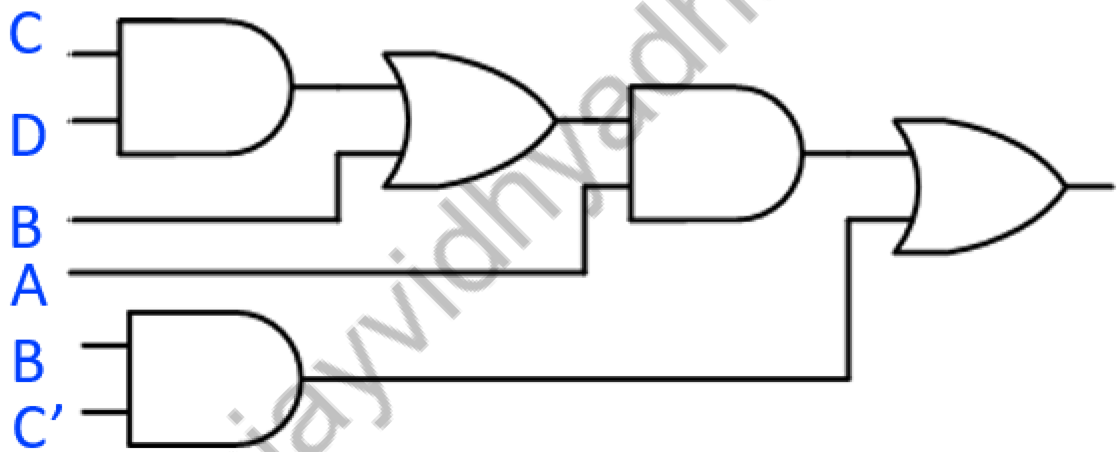




# NAND Implementation

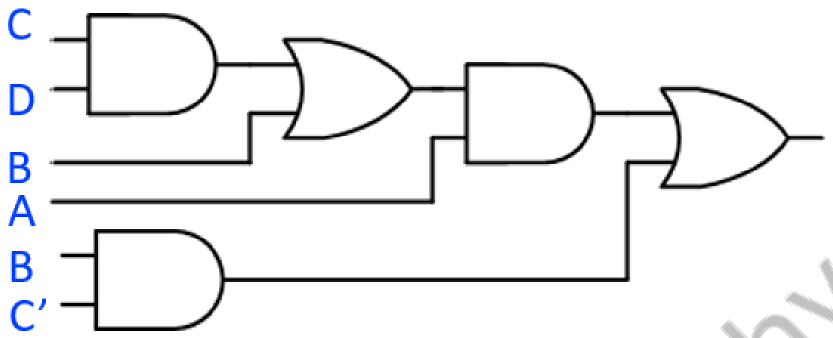
NAND gate realization        A(CD+B) + BC’

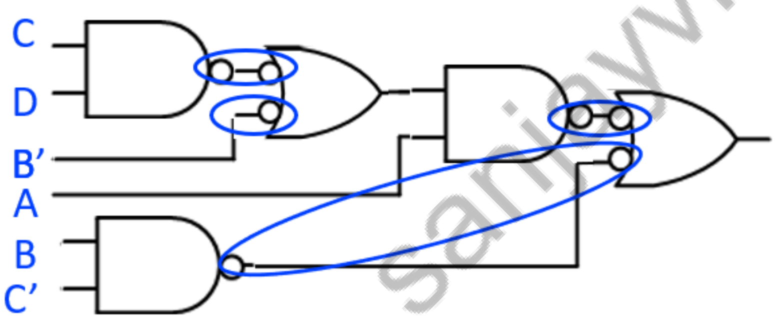


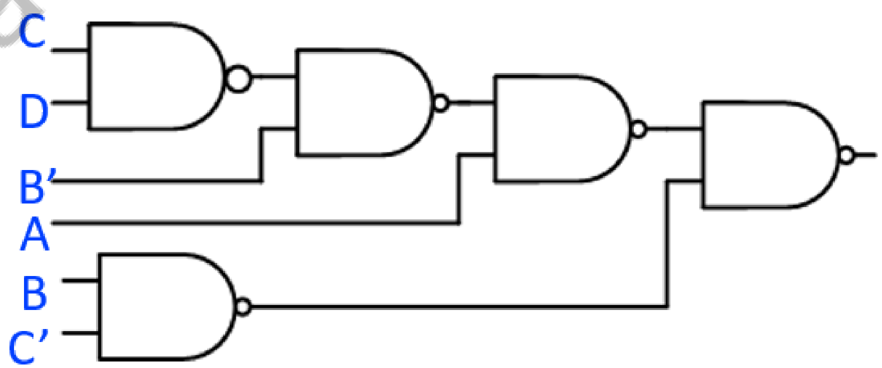
# NAND Implementation

NAND gate realization

A(CD+B) + BC’



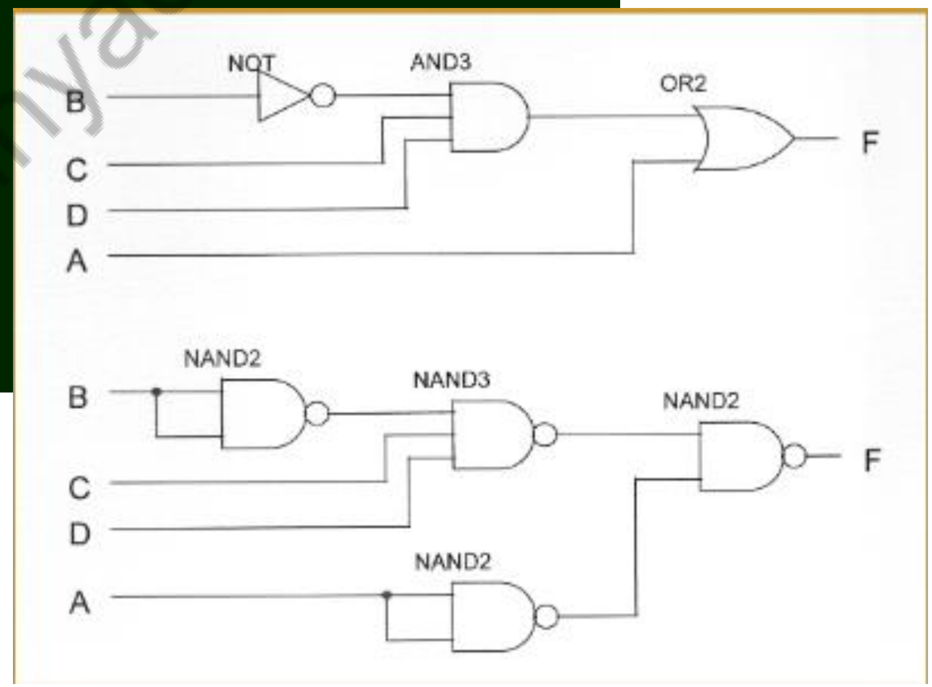
# NAND Implementation

| AB \ CD | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 0 | 1 | 0 |
| 01 | 0 | 0 | 0 | 0 |
| 11 | 1 | 1 | 1 | 1 |
| 10 | 1 | 1 | 1 | 1 |

B'CD

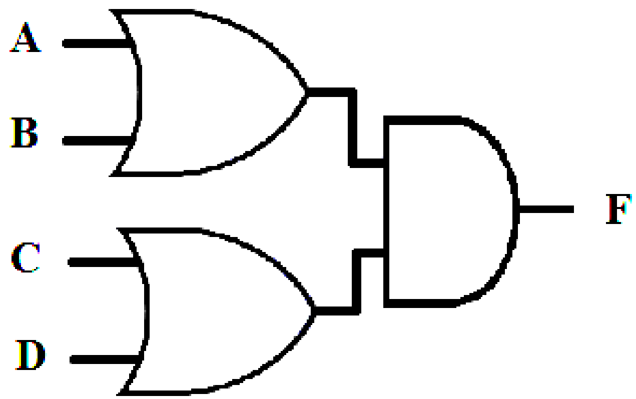
A

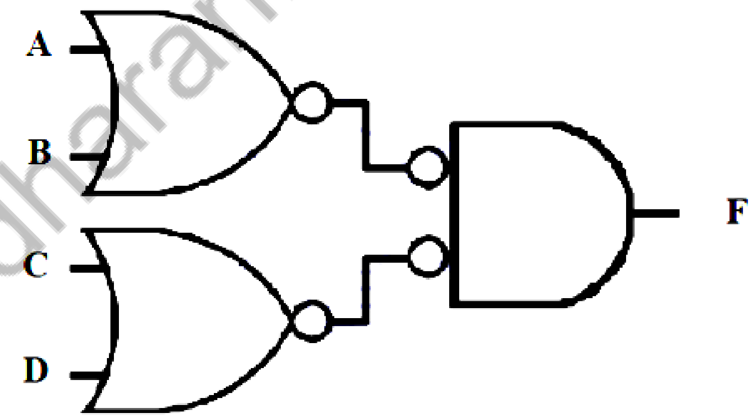
$$F = A + B'CD$$

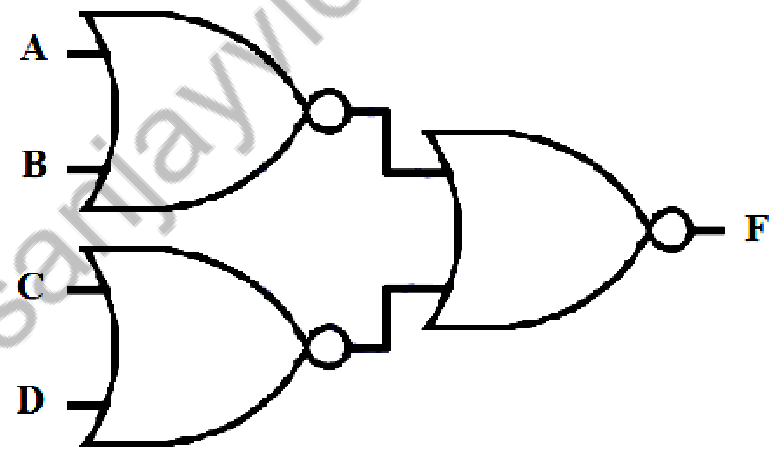


# NOR Implementation

$F = (A + B)(C + D))$



# Example - 1

Inputs are three (x, y, z) , Output is proposal (F)

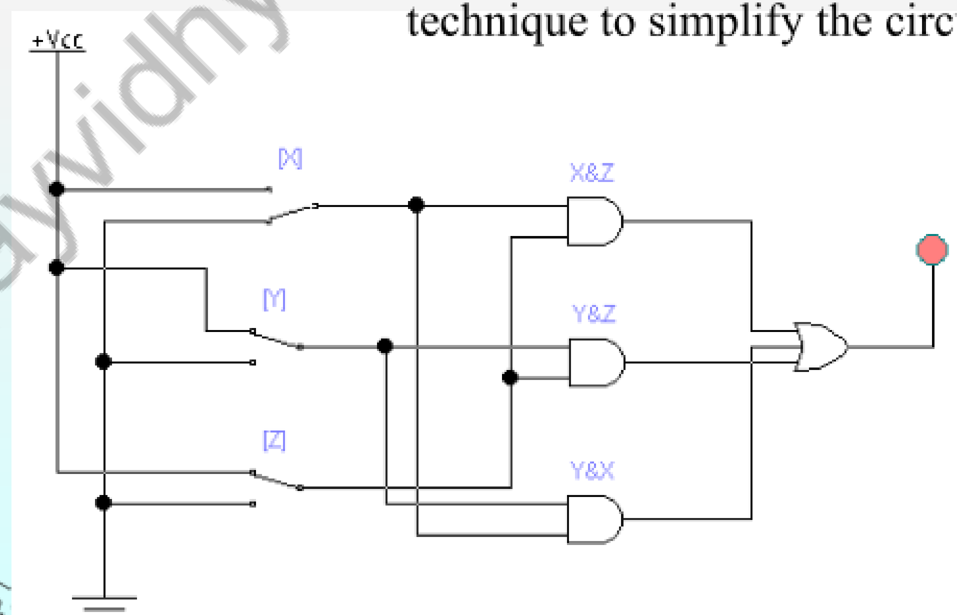
| Individual1 (X) | Individual2 (Y) | Individual3 (Z) | Proposal(F) |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

| X \ YZ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | | | 1 | |
| 1 | | 1 | 1 | 1 |

$$F = XY + XZ + YZ$$

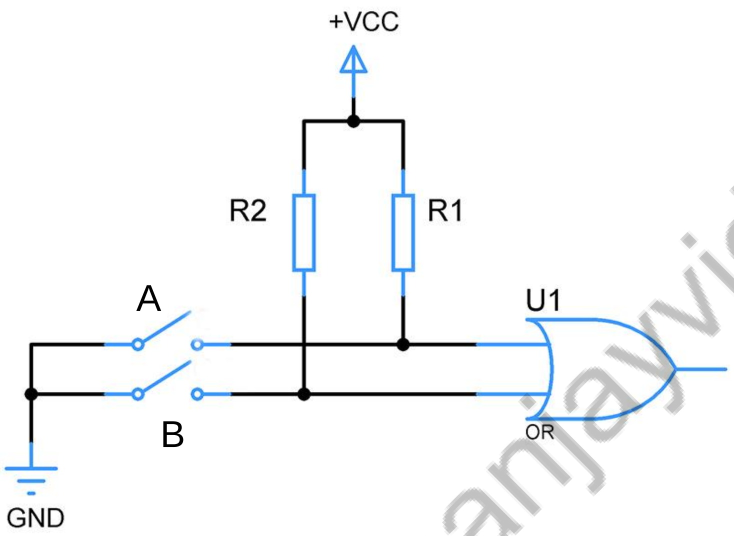
We used K-Map minimization technique to simplify the circuit.

We used truth table to make a relationship between inputs and output.

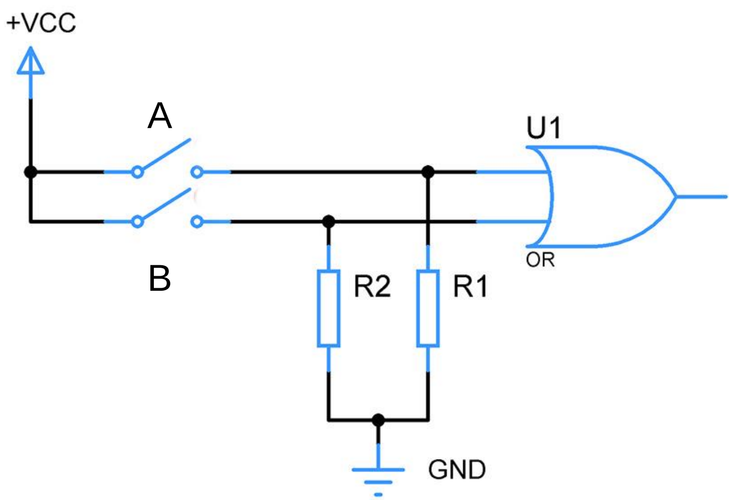


# Practical Implementation

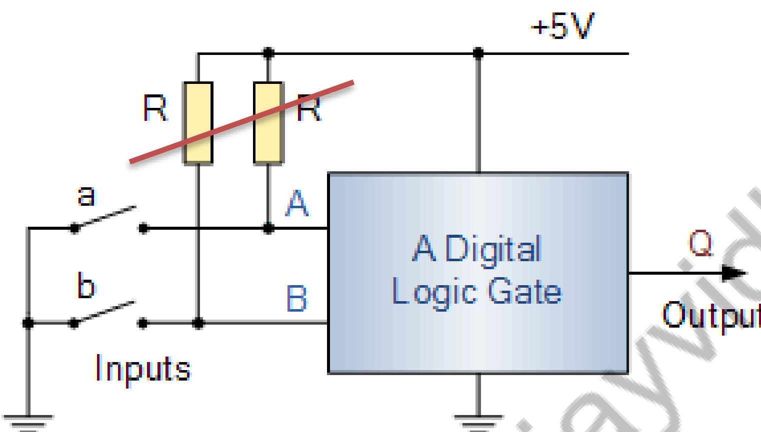
## Pull-up Resistor

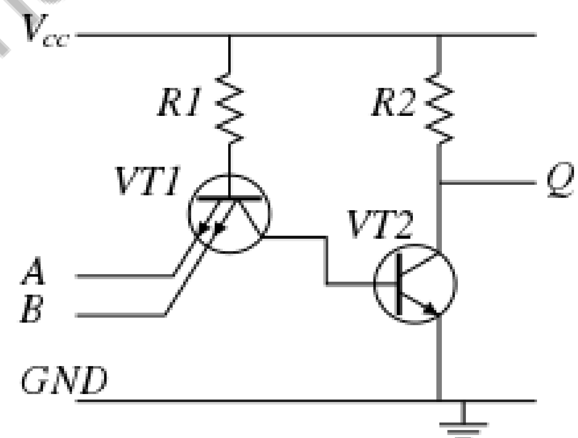



## Pull-down Resistor



# Practical Implementation TTL Gate



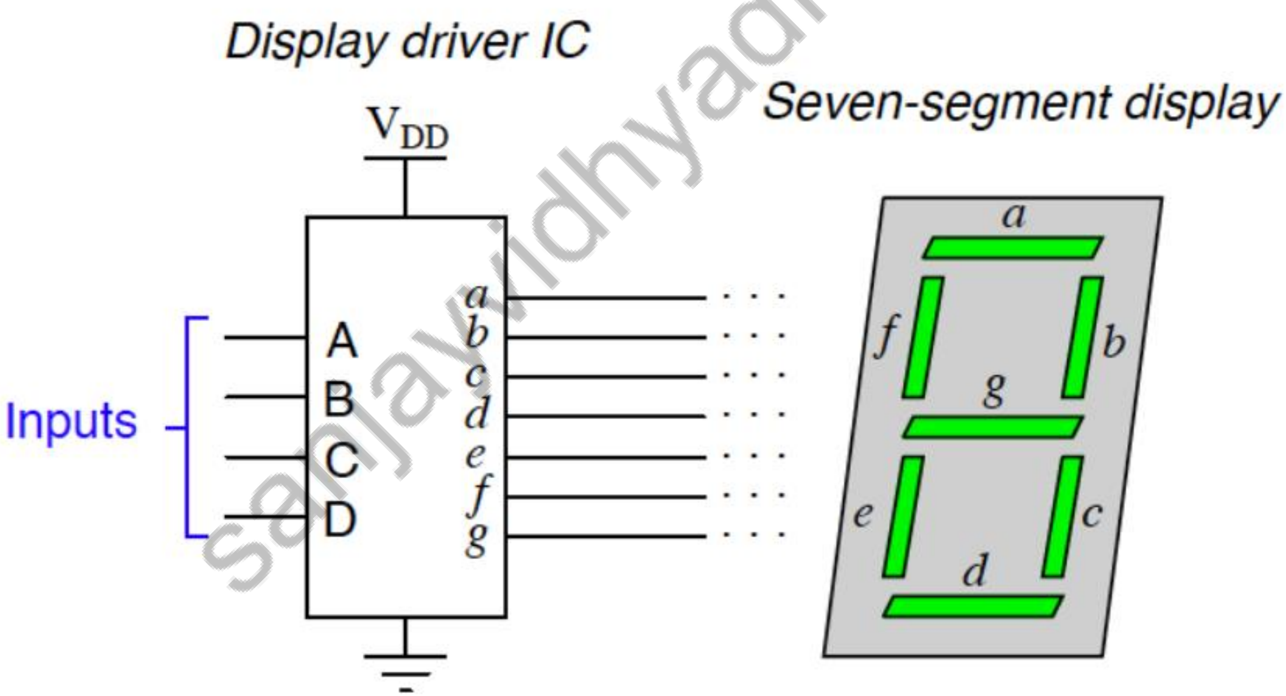



# Example - 2

Design a 7-segment Decoder

Inputs A,B,C, D $(0\text{-}9)_{10}$ valid inputs & $(10\text{-}15)_{10}$ Don't Care

Outputs a,b,c,d,e,f



# Example - 2

Design a 7-segment Decoder

Inputs A,B,C, D $(0\text{-}9)_{10}$ valid inputs & $(10\text{-}15)_{10}$ Don't Care

Outputs a,b,c,d,e,f

| D | C | B | A | a | b | c | d | e | f | g | Display |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | ”0” |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | ”1” |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | ”2” |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | ”3” |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | ”4” |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | ”5” |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | ”6” |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | ”7” |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | ”8” |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | ”9” |

# Example - 2

Design a 7-segment Decoder

Inputs A,B,C, D $(0\text{-}9)_{10}$ valid inputs & $(10\text{-}15)_{10}$ Don't Care

Outputs a,b,c,d,e,f

| AB \ CD | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 1 | 0 | 1 | 1 |
| 01 | 0 | 1 | 1 | 1 |
| 11 | × | × | × | × |
| 10 | 1 | 1 | × | × |

$a = A + C + BD + \overline{B}\,\overline{D}$

| AB \ CD | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 1 | 0 | 1 | 1 |
| 01 | 1 | 0 | 1 | 0 |
| 11 | × | × | × | × |
| 10 | 1 | 1 | × | × |

$b = \overline{B} + \overline{C}\,\overline{D} + CD$

| AB \ CD | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 1 | 1 | 1 | 0 |
| 01 | 1 | 1 | 1 | 1 |
| 11 | × | × | × | × |
| 10 | 1 | 1 | × | × |

$c = B + \overline{C} + D$

# Example - 2

Design a 7-segment Decoder

Inputs A,B,C, D $(0\text{-}9)_{10}$ valid inputs & $(10\text{-}15)_{10}$ Don't Care

Outputs a,b,c,d,e,f

| AB \ CD | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 1 | 0 | 1 | 1 |
| 01 | 0 | 1 | 0 | 1 |
| 11 | × | × | × | × |
| 10 | 1 | 1 | × | × |

$d = \bar{B}\bar{D} + C\bar{D} + B\bar{C}D + \bar{B}C + A$

| AB \ CD | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 1 | 0 | 0 | 1 |
| 01 | 0 | 0 | 0 | 1 |
| 11 | × | × | × | × |
| 10 | 1 | 0 | × | × |

$e = \bar{B}\bar{D} + C\bar{D}$

| AB \ CD | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 1 | 0 | 0 | 0 |
| 01 | 1 | 1 | 0 | 1 |
| 11 | × | × | × | × |
| 10 | 1 | 1 | × | × |

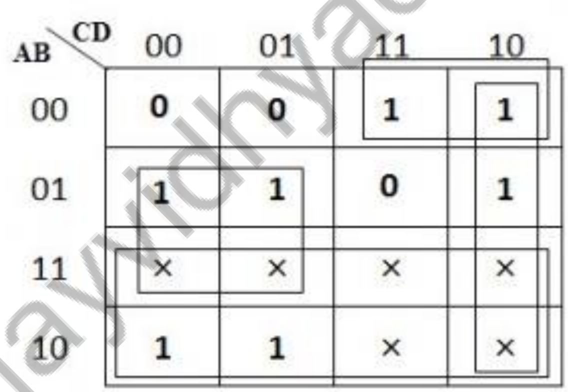
$f = A + \bar{C}\bar{D} + B\bar{C} + B\bar{D}$

# Example - 2

Design a 7-segment  Decoder

Inputs A,B,C, D $(0\text{-}9)_{10}$ valid inputs & $(10\text{-}15)_{10}$ Don't Care

Outputs a,b,c,d,e,f



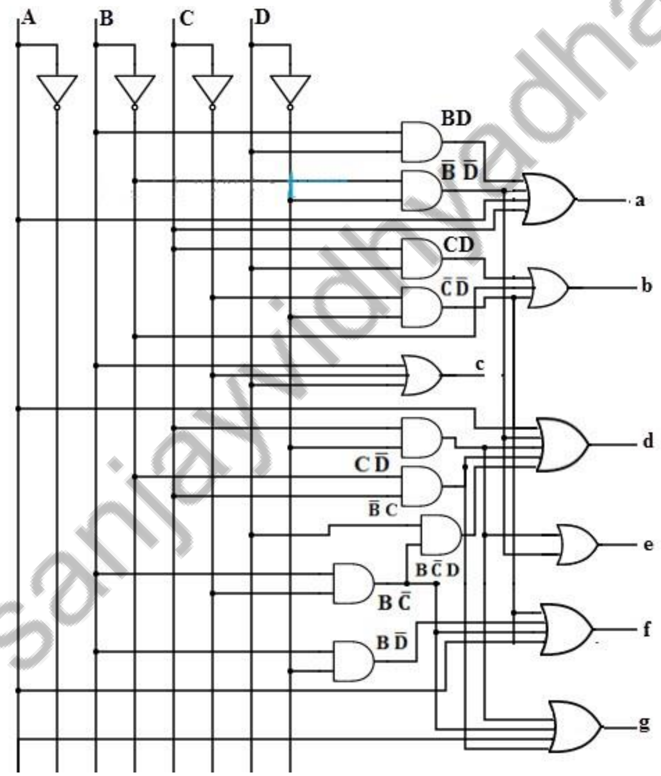

$$g = \overline{B}\,C + C\,\overline{D} + B\,\overline{C} + B\,\overline{C} + A$$

# Example - 2

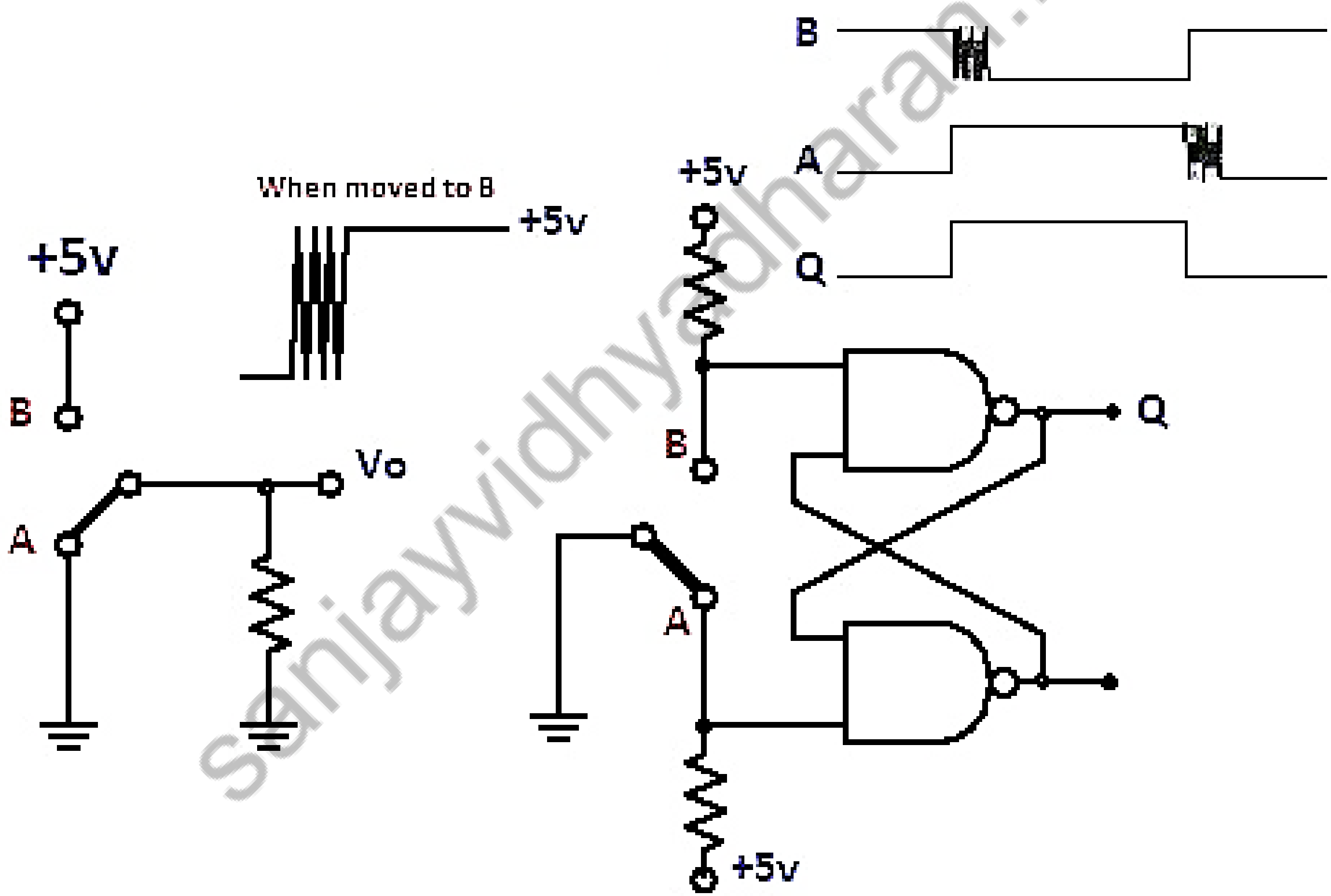
Design a 7-segment Decoder

Inputs A,B,C, D $(0\text{-}9)_{10}$ valid inputs & $(10\text{-}15)_{10}$ Don't Care

Outputs a,b,c,d,e,f



# De-Bouncing Switch



# Thank you