Introduction to Digital Design Course

By Dr. Sanjay Vidhyadharan

Textbooks

- T1: M.Moris Mano and Michael D. Ciletti " Digital Design", Pearson, 5th Edition, 2013.

- Reference Books:
  - R1. Neal S. Widmer, Gregory L. Moss & Ronald J. Tocci, "Digital Systems Principles and Applications" Pearson, 12th Edition, 2018.
  - R2. Charles H. Roth, Jr. and Larry L. Kinney "Fundamentals of Logic Design" Cengage Learning 7th Edition, 2013.
  - R3: M.Moris Mano and Michael D. Ciletti " Digital Logic and Computer Design", Pearson,, e-Book, 2016.

Course Content

Contact Hour	List of Topic Title	Topic	Text/Ref Book
1-2	Digital Systems and Numbering Systems: Digital systems, Binary Numbers, Number base Conversion: Decimal, Binary, Octal, hexadecimal Number, Complements	1.1- 1.4	T1 – Chapter 1 [1.1 – 1.5]
3-4	Digital Systems and Numbering Systems: Signed Binary Numbers, Binary codes, Binary Storage and registers, and Binary Logic	1.5-1.7	T1 – Chapter 1[1.6-1.9]
5-6	Boolean Algebra and Logic Gates: Basic Theorems and Properties of Boolean Algebra, Boolean Functions, Canonical and Standard Forms, Digital Logic Gates	2.1-2.4	T1- Chapter 2 [2.1-2.8]
7-8	Digital Logic Families: Characteristics of Digital ICs, Resistor Transistor Logic, Diode Transistor Logic, Transistor - Transistor Logic, 5400/7400 TTL series,	3.1-3.4	T2 – Chapter 4[4.1-4.3, 4.8, 4.10]
9-10	Digital Logic Families: Emitter Coupled Logic, MOS Logic, CMOS Logic, Tristate Logic Gate Level Minimization: Introduction, The Map Method-Two, Three and Four Variable Map.	3.5-3.8 4.1-4.2	T2 – Chapter 4 [4.11, 4.13,4.14, 4.20] T1 – Chapter 3 [3.1-3.3]
11-12	Gate Level Minimization: Five and Six Variable, Quine – McCluskey Minimization Technique, Product of Sums Simplification, Don't Care Conditions,	4.2-4.5	T1- Chapter 3[3.4-3.5] T2 – Chapter 5
13-14	Gate Level Minimization: NAND and NOR Implementations. Combinational Circuits: Introduction, Analysis and Design procedure, Binary Adder – Subtractor	4.6 5.1-5.3	T1 - - Chapter 3[3.6], Chapter 4 [4.1-4.5]
15 -16	Combinational Logic : Decimal Adder, Binary Multiplier, Magnitude Comparator Revision	5.4-5.6	T1 – Chapter 4 [4.6-4.8]

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Contact Hour	List of Topic Title	Topic	Text/Ref Book
17-18	Combinational Logic : Decoders, Encoders, Multiplexor, Demultiplexor	5.7-5.10	T1 – Chapter 4 [4.9 – 4.11]
19-20	Synchronous Sequential Circuits: Introduction to sequential circuits, Combinational Logic Vs Sequential Logic, Storage Elements: SR Latch, SR Flip Flop, J K Flip Flop, D Flip Flop	6.1-6.2.3	T1 – Chapter 5 [5.1-5.4]
21-22	Synchronous Sequential Circuits: Storage Elements-T Flip Flop, Master Slave Flip Flop, Characteristic tables and equations of flip flops, Analysis of Clocked Sequential Circuits, State Reduction	6.2.4-6.4	T1 – Chapter 5 [5.4, 5.5, 5.7]
23-24	Registers and Counters: Registers, Shift Registers, Ripple, Counter, Synchronous Counters	7.1-7.4	T1 – Chapter 6 [6.1-6.4]
25-26	Registers and Counters: Up Down Counter, Design of Mod n counter, Other Counters	7.5-7.6	T1 – Chapter 6 [6.4]
27-28	Memory And Programmable Logic: Random Access Memory, Memory Decoding, Error Detection and Correction, Read Only Memory,	8.1-8.4	T1 – Chapter 7 [7.1-7.5]
29-30	Memory And Programmable Logic : Programmable Logic Array, Programmable Array Logic, Sequential Programmable Devices A/D and D/A Converters: Digital to Analog Converters, An example of D/A Converter IC , Sample and Hold	8.5-8.7 9.1-9.3	T1 – Chapter 7 [7.6-7.9] T2 – Chapter 10 [10.1-10.4]
31-32	A/D and D/A Converters: Analog to Digital Converters, An example of A/D Converter IC Revision	9.4-9.5	T2 – Chapter 10 [10.5-10.6]

Course Calendar

Week	Date	Day	Contact Session	Remarks (If any)
1	14-Nov-21	Sunday	Contact Session 1	
2	21-Nov-21	Sunday	Contact Session 2	
3	28-Nov-21	Sunday	Contact Session 3	
4	05-Dec-21	Sunday	Contact Session 4	
5	12-Dec-21	Sunday	Contact Session 5	
6	18-Dec-21	Saturday	Lab session	Digital Design and Data Structures
6	19-Dec-21	Sunday	Contact Session 6	
7	26-Dec-21	Sunday	Contact Session 7	
8	02-Jan-22	Sunday	Contact Session 8	
9	09-Jan-22	Sunday	Buffer Session	
10	16-Jan-22	Sunday	Mid Semester	2 courses(LAO-FN & DD-AN)
11	23-Jan-22	Sunday	Mid Semester	2 courses(DS-FN & CT-AN)
12	30-Jan-22	Sunday	Contact Session 9	
13	06-Feb-22	Sunday	Contact Session 10	
14	13-Feb-22	Sunday	Contact Session 11	
15	20-Feb-22	Sunday	Contact Session 12	
16	27-Feb-22	Sunday	Contact Session 13	
17	05-Mar-22	Saturday	Lab session	Digital Design and Data Structures
17	06-Mar-22	Sunday	Contact Session 14	
18	13-Mar-22	Sunday	Contact Session 15	
19	20-Mar-22	Sunday	Contact Session 16	
20	27-Mar-22	Sunday	Buffer Session	
21	03-Apr-22	Sunday	Comprehensive Exam	2 courses(LAO-FN & DD-AN)
22	10-Apr-22	Sunday	Comprehensive Exam	2 courses (DS-FN & CT-AN)

Evaluation

Sl.No.	Evaluation Component	Type	Weight	Duration	Day, Date, Session, Time
EC - 1	Quiz 1	Online	5%	TBA	To be announced
	Quiz 2	Online	5%		To be announced
	Assignment 1	Online	5%		To be announced
	Lab Exam	Online	15%		To be announced
EC - 2	Mid-Semester Test	Open Book	30%	2 hours	16-01-2022 AN 2.00 -4.00 PM
EC - 3	Comprehensive Exam	Open Book	40%	3 hours	03-04-2022 AN 2.00 – 5.00 PM

Thank you