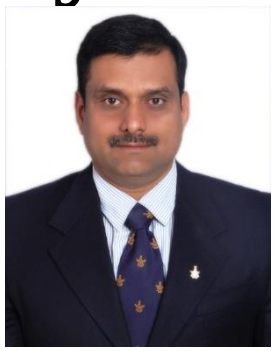
BITS Pilani
Hyderabad Campus
Department of Electrical Engineering

# Digital Design : 2021-22
# Lab 1: Implementation of Majority Circuit using TTL Gates in Tinkercad

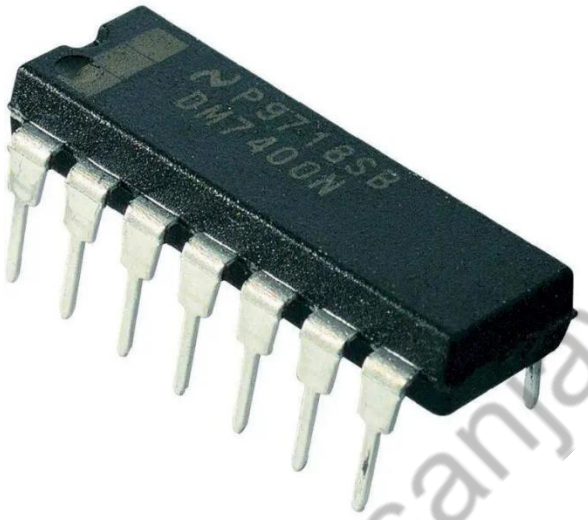


**By Dr. Sanjay Vidhyadharan**

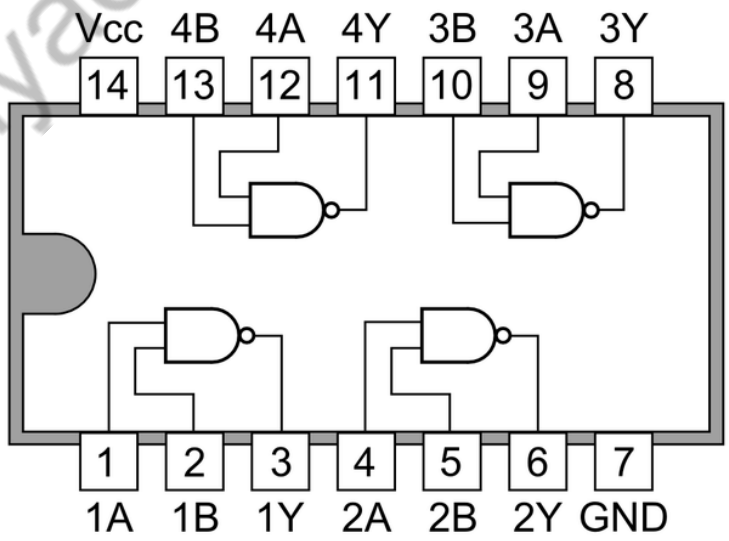


# 74XX Series TTL ICs

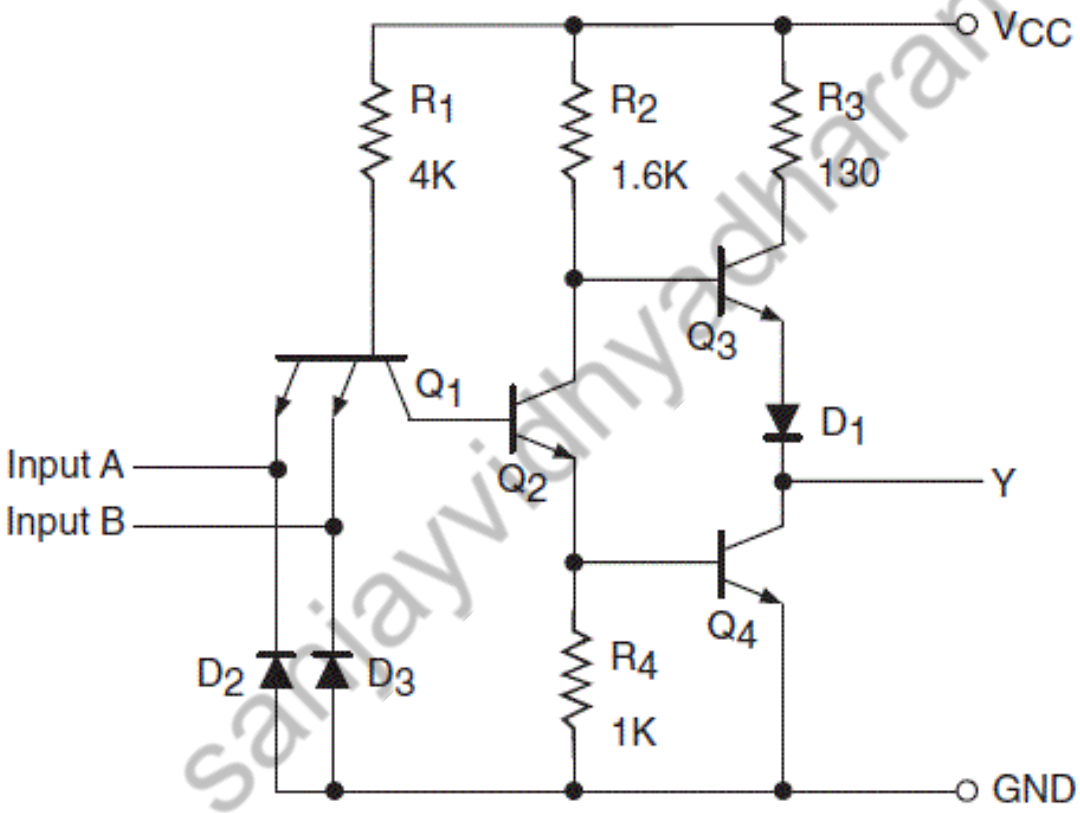
## 7400 NAND




7400 Quad 2-input NAND Gates



# TTL Gate






**TTL 2 input NAND Gate**

# 74XX Series TTL ICs

## 7400 NAND DATA SHEET



FAIRCHILD
SEMICONDUCTOR™

September 1986
Revised July 2001

DM7400 Quad 2-Input NAND Gates

### DM7400
### Quad 2-Input NAND Gates

#### General Description

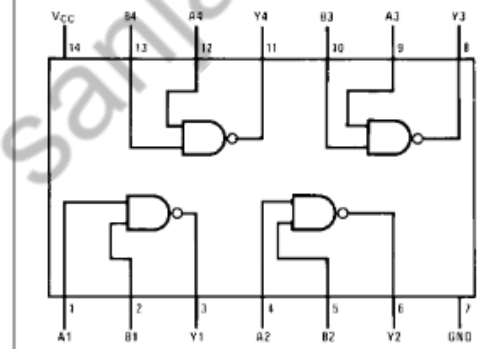
This device contains four independent gates each of which performs the logic NAND function.

#### Ordering Code:

| Order Number | Package Number | Package Description |
|---|---|---|
| DM7400M | M14A | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| DM7400N | N14A | 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

#### Connection Diagram




#### Function Table

$Y = \overline{AB}$

| Inputs | | Output |
|---|---|---|
| A | B | Y |
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

H = HIGH Logic Level
L = LOW Logic Level

# 74XX Series TTL ICs

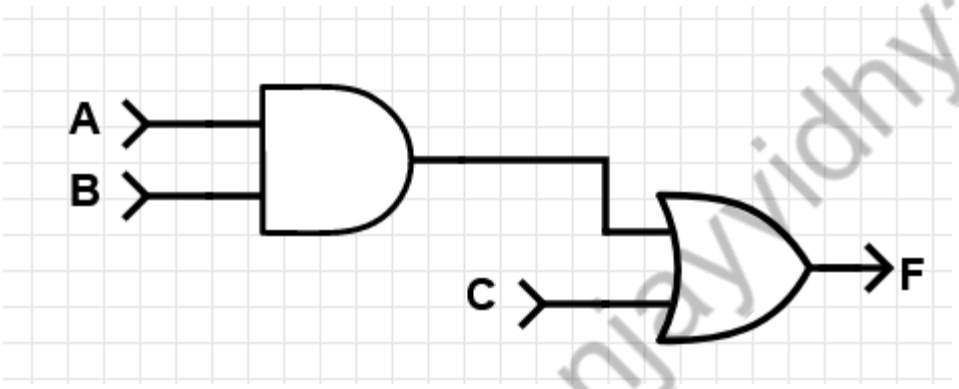
## 7400 NAND DATA SHEET

### Recommended Operating Conditions

| Symbol | Parameter | Min | Nom | Max | Units |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 4.75 | 5 | 5.25 | V |
| $V_{IH}$ | HIGH Level Input Voltage | 2 | | | V |
| $V_{IL}$ | LOW Level Input Voltage | | | 0.8 | V |
| $I_{OH}$ | HIGH Level Output Current | | | −0.4 | mA |
| $I_{OL}$ | LOW Level Output Current | | | 16 | mA |
| $T_A$ | Free Air Operating Temperature | 0 | | 70 | °C |

# Sample Run

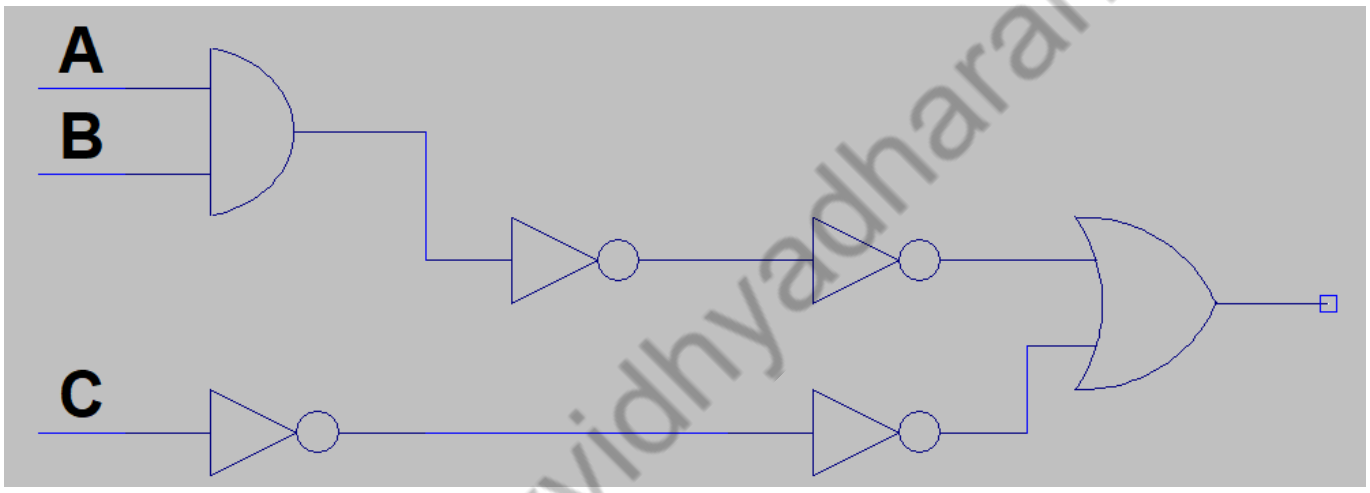
## F= AB+C (Implementation with AND & OR Gates)

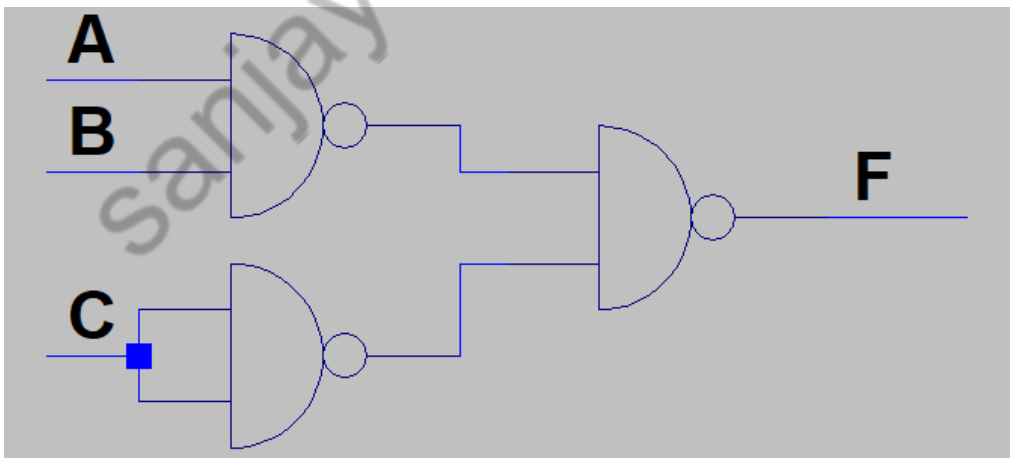



| A | B | C | F |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 |

# Sample Run

**F= AB+C Implementation with NAND Gates**



# Problem Definition for DD: Lab 1

## Problem 1: Implement the Majority Circuit

| A | B | C | F |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

$$F = AB + BC + CA + ABC$$

$$F = AB + BC + CA$$

# Problem definition for DD: Lab 1

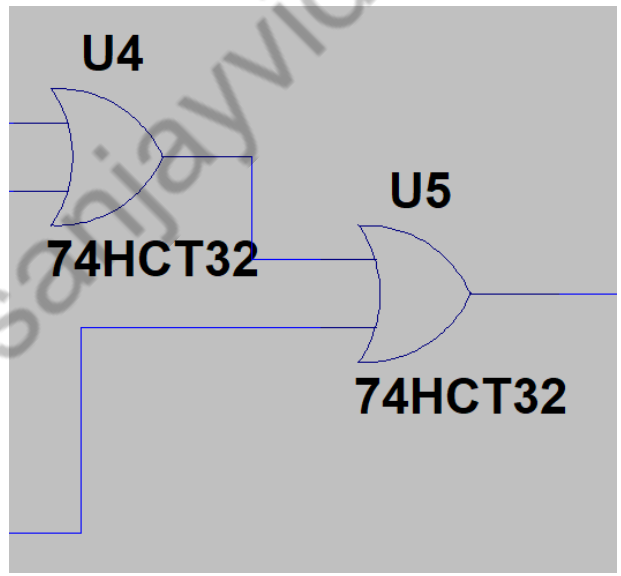
## Problem 1: Implement the Majority Circuit

**Run1 : Implement F with AND & OR gates**

**Check output for all combinations of Input**

**F= AB+BC+CA**

**Hint: Use Three 2 i/p AND & Two 2 i/p OR GATE**



# Problem definition for DD: Lab 1

## Problem 1: Implement the Majority Circuit

**Run1 : Implement F with NAND gates**

**F= AB+BC+CA**

**Check output for all combinations of Input**

**Hint: Use Three 2 i/p NAND & One 3 i/p NAND GATE**

# Demonstration