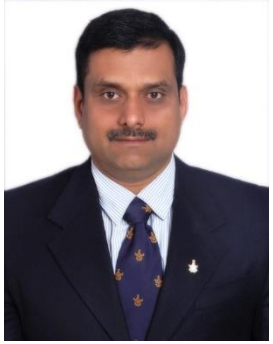
MPI Tutorial-11

Memory Interface

By Dr. Sanjay Vidhyadharan



Question 1

- **Design an 8088 based system that has the following memory requirements:**
  - **256K of ROM from 00000_H**
  - **256K of ROM from $C0000_H$**
  - **256K of RAM from 60000_H.**

Available Chips:

64K ROM -8

64K RAM -4

LS138-2

Solution 1

- 256K of ROM from 00000_H
- 00000 to $3FFFF_H$
- 256K of ROM from $C0000_H$
- C0000 to $FFFFF_H$
- 256K of RAM from 60000_H.

  60000 to $9FFFF_H$

Available Chips:

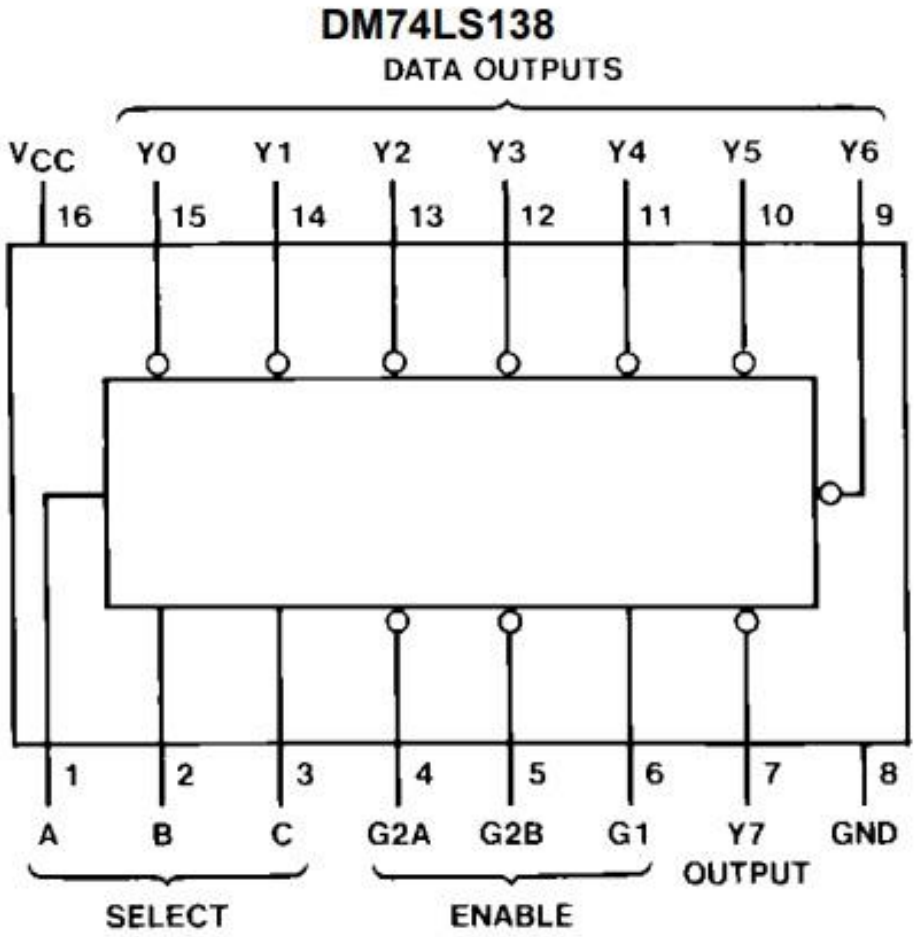
64K ROM -8 ---A_0-A_{15}

64K RAM -4 ---A_0-A_{15}

1K	10 Lines
2K	11 Lines
4K	12 Lines
8K	13 Lines
16 K	14 Lines
32 K	15 Lines
64 K	16 Lines
128 K	17 Lines
256 K	18 Lines
512 K	19 Lines
1M	20 Lines

256 K	18 Lines	0011-1111-1111-1111-1111

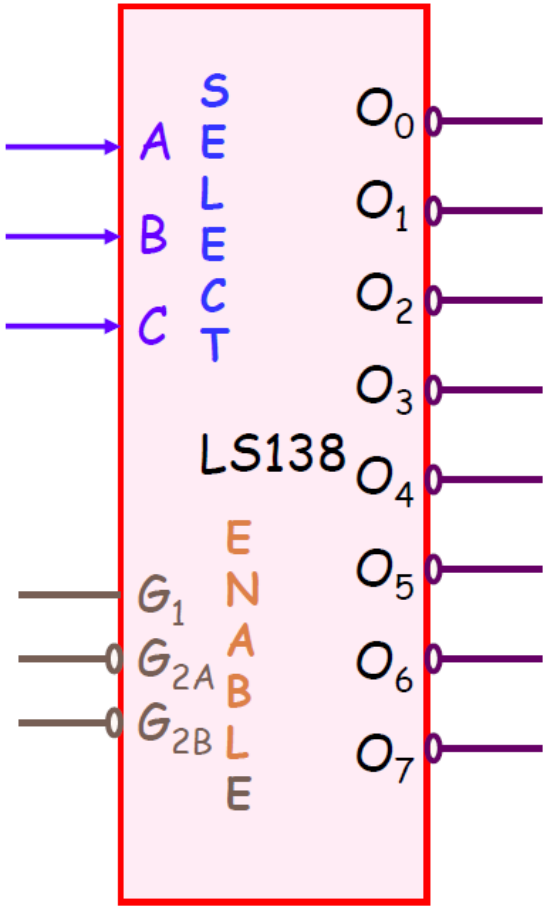
Solution 1


DM74LS138
DATA OUTPUTS
VCC
Y0
Y1
Y2
Y3
Y4
Y5
Y6
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
A
B
C
G2A
G2B
G1
Y7
GND
OUTPUT
SELECT
ENABLE


HD74LS138P
9D36

Solution 1

SN54/74LS138 Decoder/Demultiplexer



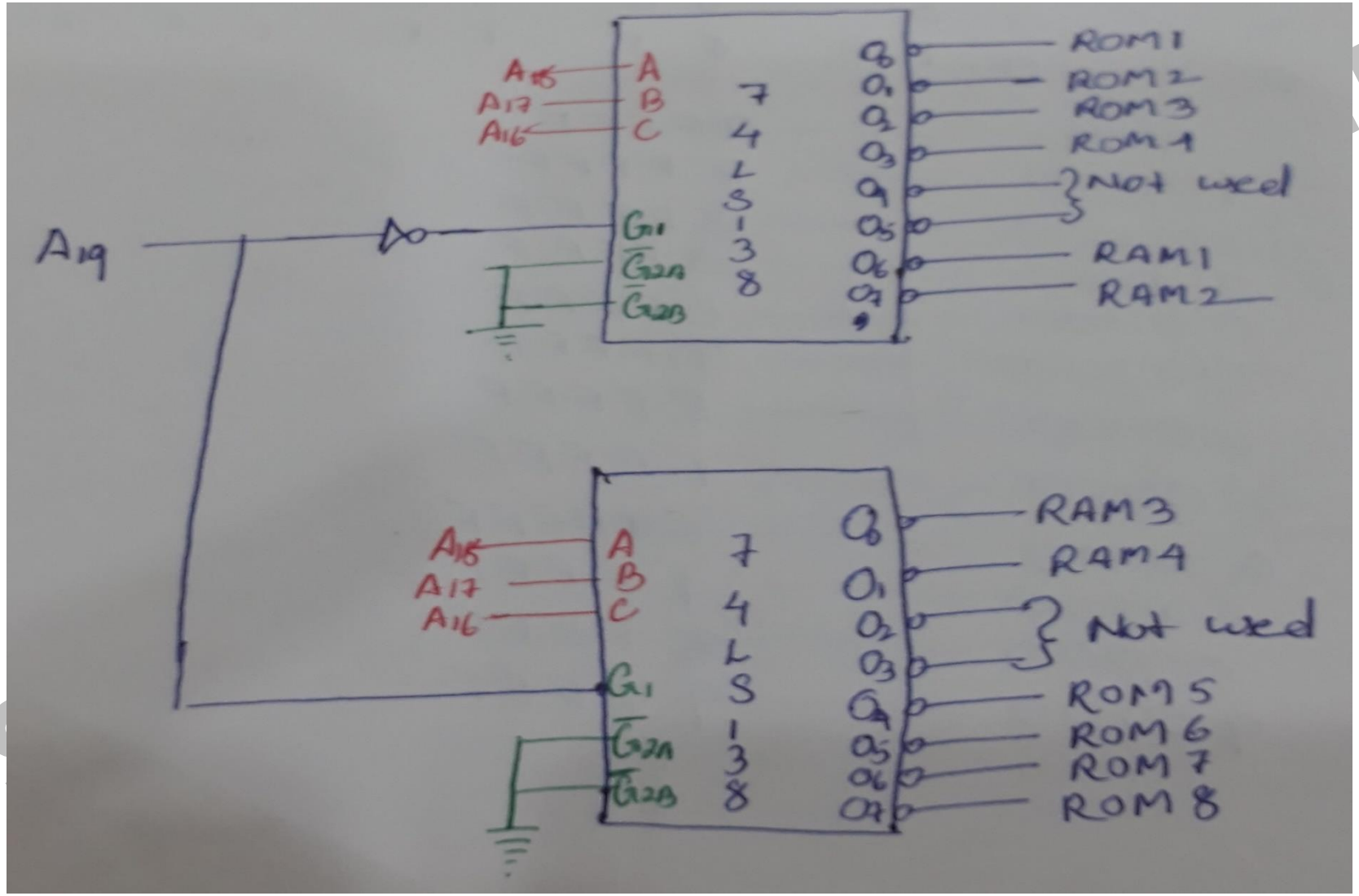
INPUT						OUTPUT							
ENABLE			SELECT										
G_1	G_{2A}	G_{2B}	A	B	C	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7
0	X	X	X	X	X	1	1	1	1	1	1	1	1
X	1	X	X	X	X	1	1	1	1	1	1	1	1
X	X	1	X	X	X	1	1	1	1	1	1	1	1
1	0	0	0	0	0	0	1	1	1	1	1	1	1
1	0	0	0	0	1	1	0	1	1	1	1	1	1
1	0	0	0	1	0	1	1	0	1	1	1	1	1
1	0	0	0	1	1	1	1	1	0	1	1	1	1
1	0	0	1	0	0	1	1	1	1	0	1	1	1
1	0	0	1	0	1	1	1	1	1	1	0	1	1
1	0	0	1	1	0	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0

Solution 1

CHIP	A19	A18	A17	A16	DECODER O/P
ROM1	0	0	0	0	D1 O_0
ROM2	0	0	0	1	D1 O_1
ROM3	0	0	1	0	D1 O_2
ROM4	0	0	1	1	D1 O_3
RAM1	0	1	1	0	D1 O_6
RAM2	0	1	1	1	D1 O_7
RAM3	1	0	0	0	D1 O_0
RAM4	1	0	0	1	D2 O_1
ROM5	1	1	0	0	D2 O_4
ROM6	1	1	0	1	D2 O_5
ROM7	1	1	1	0	D2 O_6
ROM8	1	1	1	1	D2 O_7

LS138-2 -A_{16}-A_{18} directly connected to decoder A,B,C select lines

Solution 1

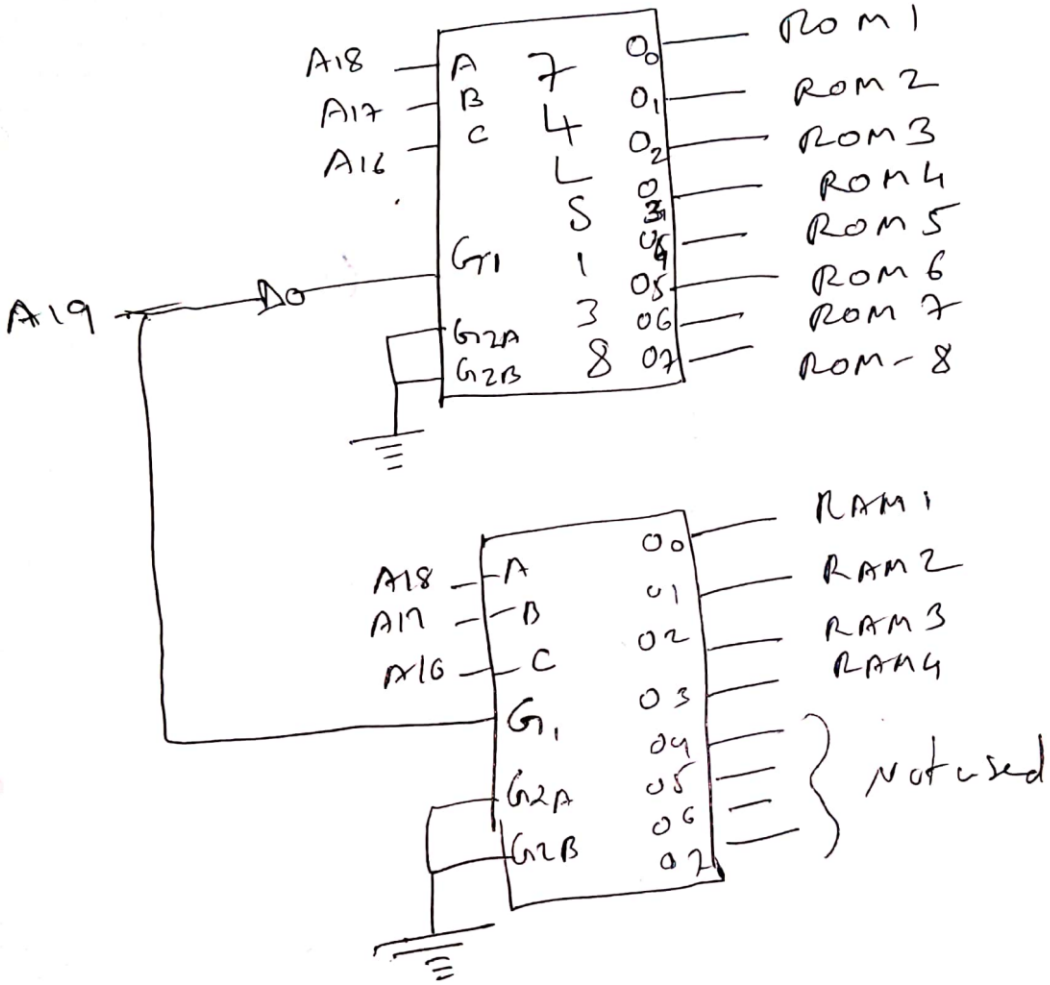

A19
A15
A17
A16
A
B
C
G1
G2A
G2B
74LS138
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
ROM1
ROM2
ROM3
ROM4
Not used
RAM1
RAM2
A15
A17
A16
A
B
C
G1
G2A
G2B
74LS138
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
RAM3
RAM4
Not used
ROM5
ROM6
ROM7
ROM8

Solution 1

CHIP	A19	A18	A17	A16	DECODER O/P
ROM1	0	0	0	0	D1 O_0
ROM2	0	0	0	1	D1 O_1
ROM3	0	0	1	0	D1 O_2
ROM4	0	0	1	1	D1 O_3
ROM5	0	1	0	0	D1 O_4
ROM6	0	1	0	1	D1 O_5
ROM7	0	1	1	0	D1 O_6
ROM8	0	1	1	1	D1 O_7
RAM1	1	0	0	0	D2 O_0
RAM2	1	0	0	1	D2 O_1
RAM3	1	0	1	0	D2 O_2
RAM4	1	0	1	1	D2 O_3

LS138-2 -A_{16}-A_{18} directly connected to decoder A,B,C select lines

Solution 1


A18
A17
A16
A19
A
B
C
G1
G2A
G2B
74LS138
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
ROM 1
ROM 2
ROM 3
ROM 4
ROM 5
ROM 6
ROM 7
ROM - 8
A18
A17
A16
A
B
C
G1
G2A
G2B
O0
O1
O2
O3
O4
O5
O6
O7
RAM 1
RAM 2
RAM 3
RAM 4
Not used

Question 2

Design 8088 based system interface with

SRAM: 16 KB From 02000_H

ROM: 16 KB From 09000_H

Memory chips to be used are as per following specification

SRAM- 2K X 8bit ROM- 2K x 8bit

74138 decoders (4 numbers available)

Using these decoders and minimum number of logic gates draw the memory interfacing diagram

Solution 2

- 16K of SRAM from 02000_H
- 02000 to $05FFF_H$
- 16K of ROM from 09000_H
- 09000 to $0CFFFF_H$

1K	10 Lines
2K	11 Lines
4K	12 Lines
8K	13 Lines
16 K	14 Lines
32 K	15 Lines
64 K	16 Lines
128 K	17 Lines
256 K	18 Lines
512 K	19 Lines
1M	20 Lines

Available Chips:

2K ROM -8 ---A_0-A_{10}

2K SRAM -8 ---A_0-A_{10}

16 K	14 Lines	0000-0011-1111-1111-1111

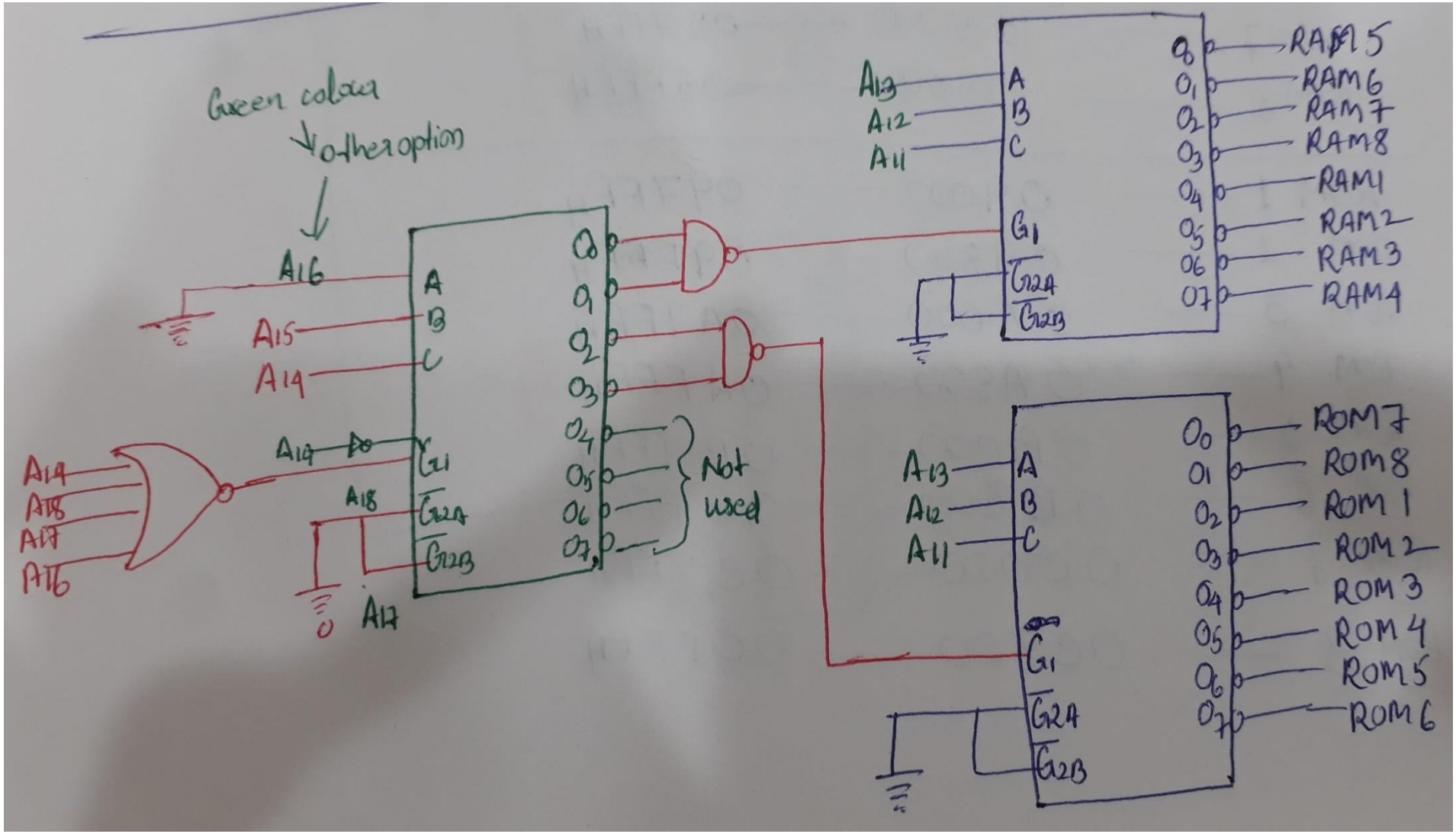
Solution 2

CHIP	A15	A14	A13	A12	A11	DECODER O/P
RAM1	0	0	1	0	0	D1 O_4
RAM2	0	0	1	0	1	D1 O_5
RAM3	0	0	1	1	0	D1 O_6
RAM4	0	0	1	1	1	D1 O_7
RAM5	0	1	0	0	0	D1 O_0
RAM6	0	1	0	0	1	D1 O_1
RAM7	0	1	0	1	0	D1 O_2
RAM8	0	1	0	1	1	D1 O_3

Solution 2

CHIP	A15	A14	A13	A12	A11	DECODER O/P
ROM1	1	0	0	1	0	D2 O_2
ROM2	1	0	0	1	1	D2 O_3
ROM3	1	0	1	0	0	D2 O_4
ROM4	1	0	1	0	1	D2 O_5
ROM5	1	0	1	1	0	D2 O_6
ROM6	1	0	1	1	1	D2 O_7
ROM7	1	1	0	0	0	D2 O_0
ROM8	1	1	0	0	1	D2 O_1

Solution 2


Green colour
other option
A16
A15
A14
A13
A12
A11
A18
A17
A0
A
B
C
G1
G2A
G2B
O0
O1
O2
O3
O4
O5
O6
O7
Not used
RAM5
RAM6
RAM7
RAM8
RAM1
RAM2
RAM3
RAM4
ROM7
ROM8
ROM1
ROM2
ROM3
ROM4
ROM5
ROM6

Question 3

Design an 80286 based system that has the following memory requirements: (80286 – 24 Address Lines – 16 MB)

- 4M of ROM and the rest is RAM
- Half of the ROM - mapped to address space starting at 00 00 00_H
- Half to address space starting from E0 00 00_H
- The RAM is mapped continuously from address 20 00 00H.

Available Chips:

1M ROM -4

1M RAM -12

LS138-4

Solution 3

- **Total memory =16 MB**
- **Given 4 MB ROM so 12 MB RAM**
- **2MB - from 000000_H**
- **2MB - from $E00000_H$**
- **12MB - from 200000_H**

<u>Available Chips:</u>

1MB ROM -4 chips ---A_0-A_{10}

1MB RAM -12 chips---A_0-A_{10}

LS138 - 2

Solution 3

- ROM_{1E}---000000,000002,…….$1FFFFE_H$
- ROM_{1O}---000001,000003,…….$1FFFFF_H$
- ROM_{2E}--E00000,E00002,…….$FFFFFE_H$
- ROM_{2O}---E00001,E00003,…….$FFFFFF_H$
- RAM_1---- 200000—$3FFFFF_H$
- RAM_2---- 400000—$5FFFFF_H$
- RAM_3---- 600000—$7FFFFF_H$
- RAM_4---- 800000—$9FFFFF_H$
- RAM_5---- A00000—$BFFFFF_H$
- RAM_6---- C00000—$DFFFFF_H$

1K	10 Lines
2K	11 Lines
4K	12 Lines
8K	13 Lines
16 K	14 Lines
32 K	15 Lines
64 K	16 Lines
128 K	17 Lines
256 K	18 Lines
512 K	19 Lines
1M	20 Lines

1M	20 Lines	1111-1111-1111-1111-1111
2M	21 Lines	1FFFFF

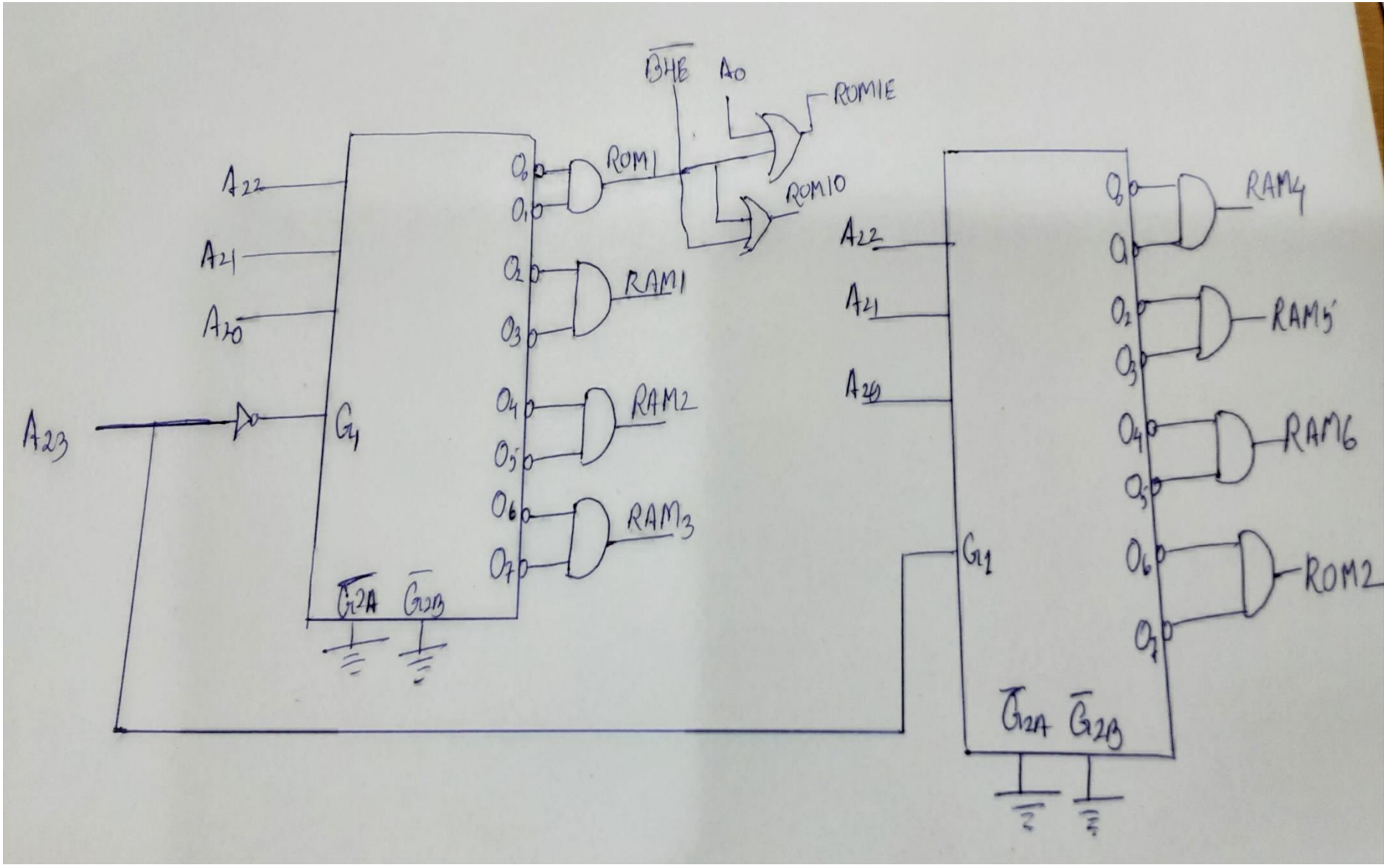
Solution 3

CHIP	A23	A22	A21	A20	DECODER O/P
$R0M_1$	0	0	0	0	D1 O_0
ROM_1	0	0	0	1	D1 O_1
ROM_2	1	1	1	0	D2 O_6
ROM_2	1	1	1	1	D2 O_7

Solution 3

CHIP	A23	A22	A21	A20	DECODER O/P
RAM1	0	0	1	0	D1 O_2
RAM1	0	0	1	1	D1 O_3
RAM2	0	1	0	0	D1 O_4
RAM2	0	1	0	1	D1 O_5
RAM3	0	1	1	0	D1 O_6
RAM3	0	1	1	1	D1 O_7
RAM4	1	0	0	0	D2 O_0
RAM4	1	0	0	1	D2 O_1
RAM5	1	0	1	0	D2 O_2
RAM5	1	0	1	1	D2 O_3
RAM6	1	1	0	0	D2 O_4
RAM6	1	1	0	1	D2 O_5

Solution 3


BHE
A0
ROMIE
ROM1
ROM10
A22
A21
A20
A23
G1
RAM1
RAM2
RAM3
G2A
G2B
RAM4
RAM5
RAM6
ROM2

Thank You