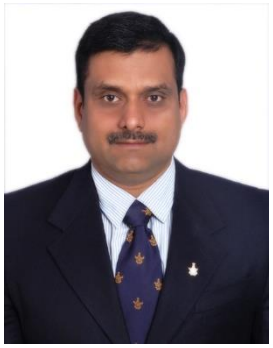
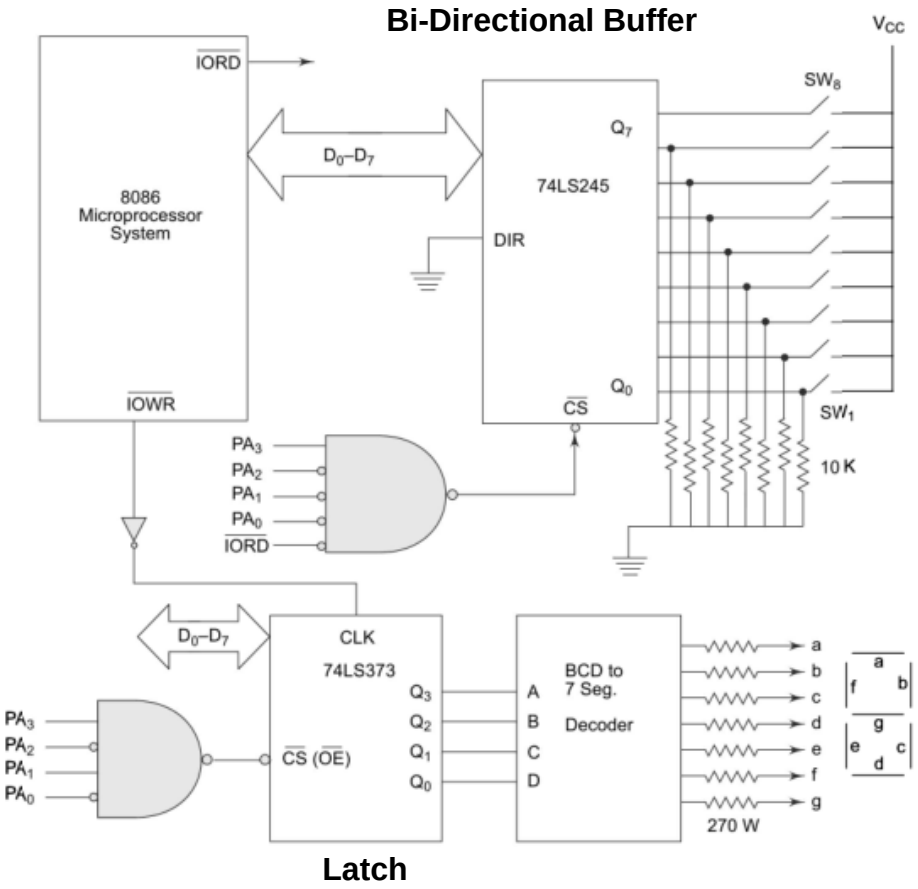
Microprocessors and Interfaces: 2021-22
Lecture 31 :
Programable Interrupt Controller 8259A

By Dr. Sanjay Vidhyadharan

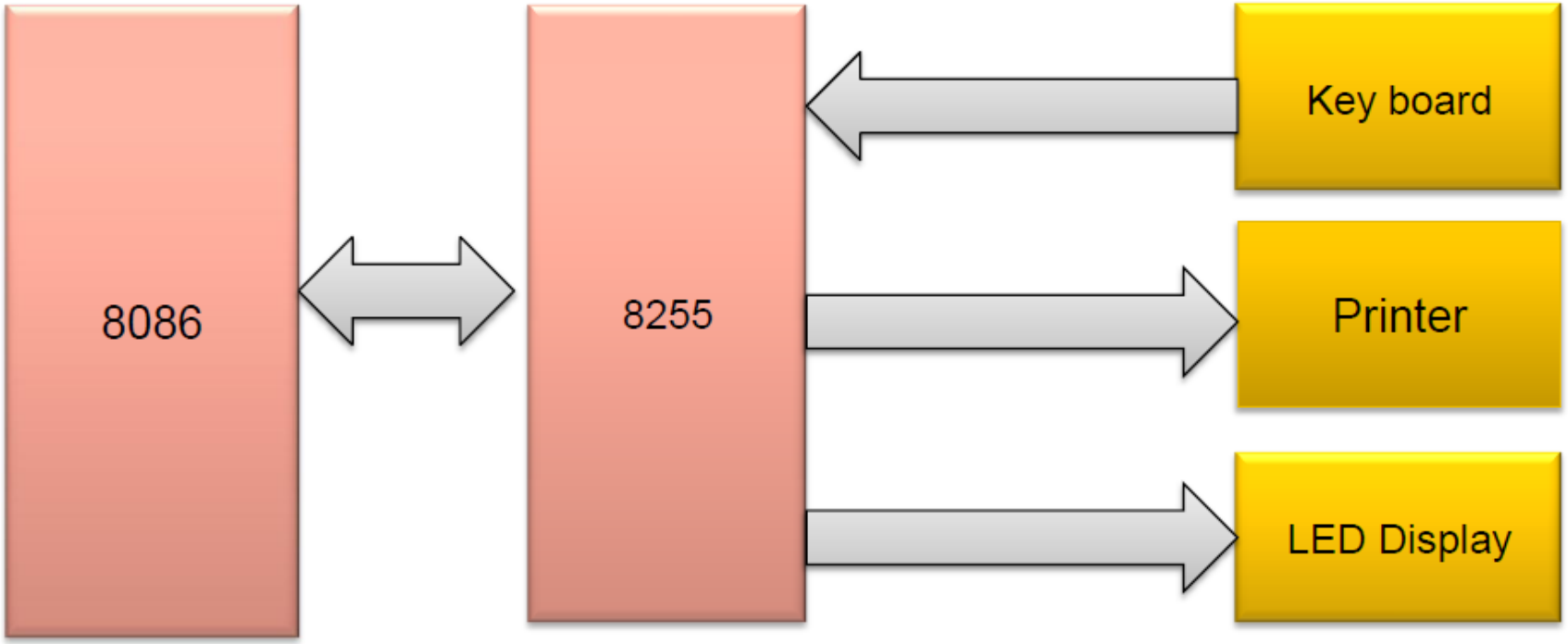


Input & Output Interface

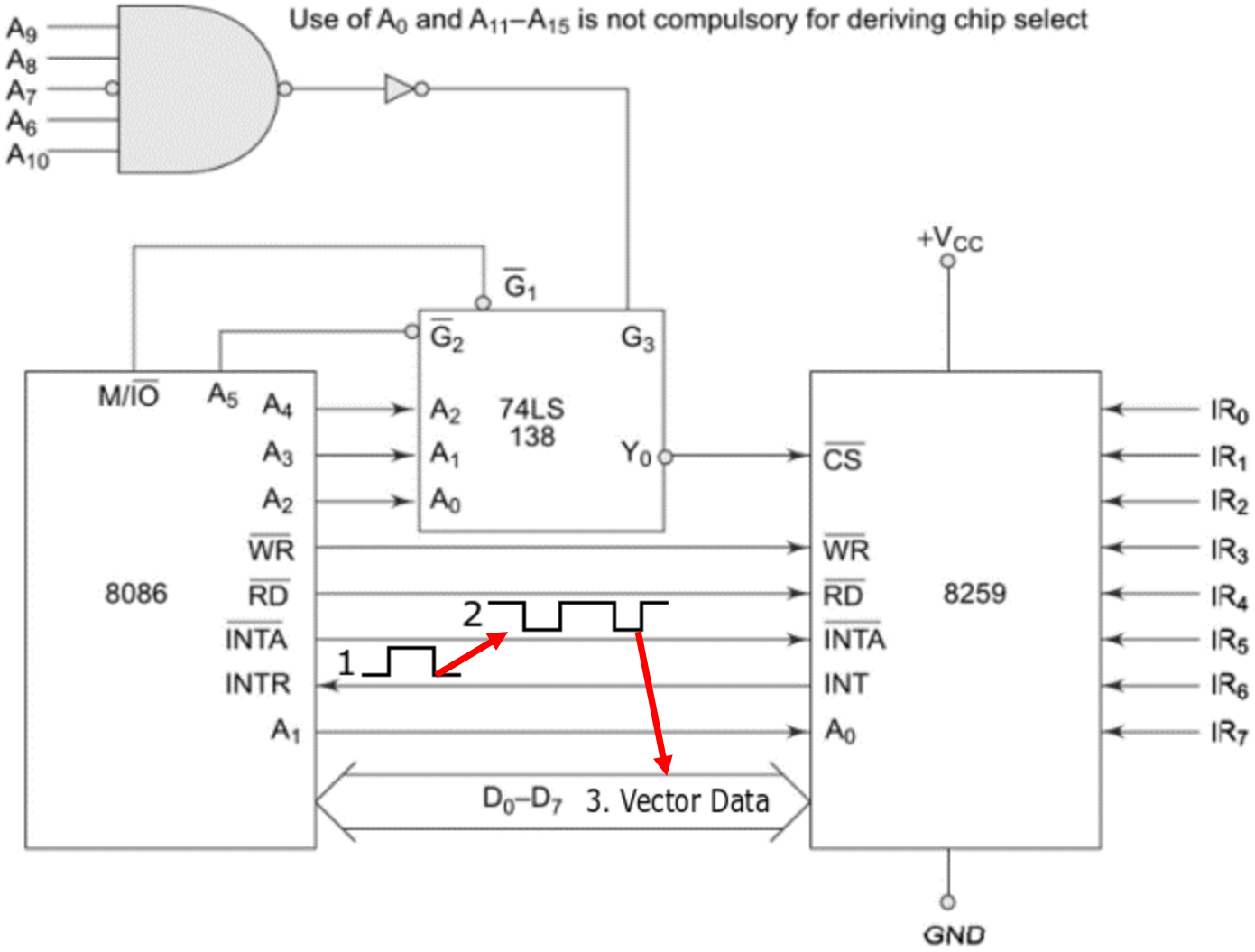


64K I/P & 64K O/P

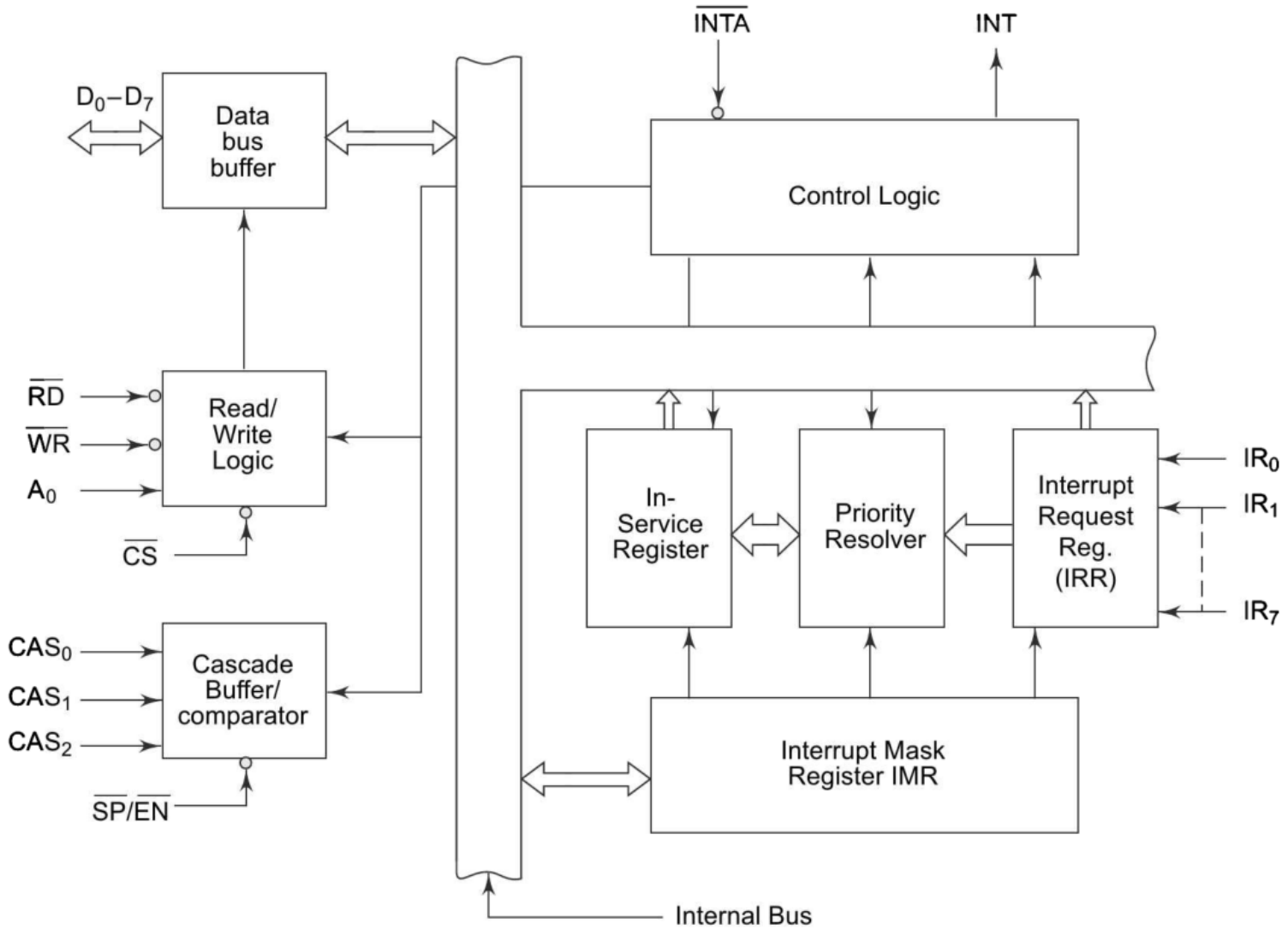
Input & Output Interface



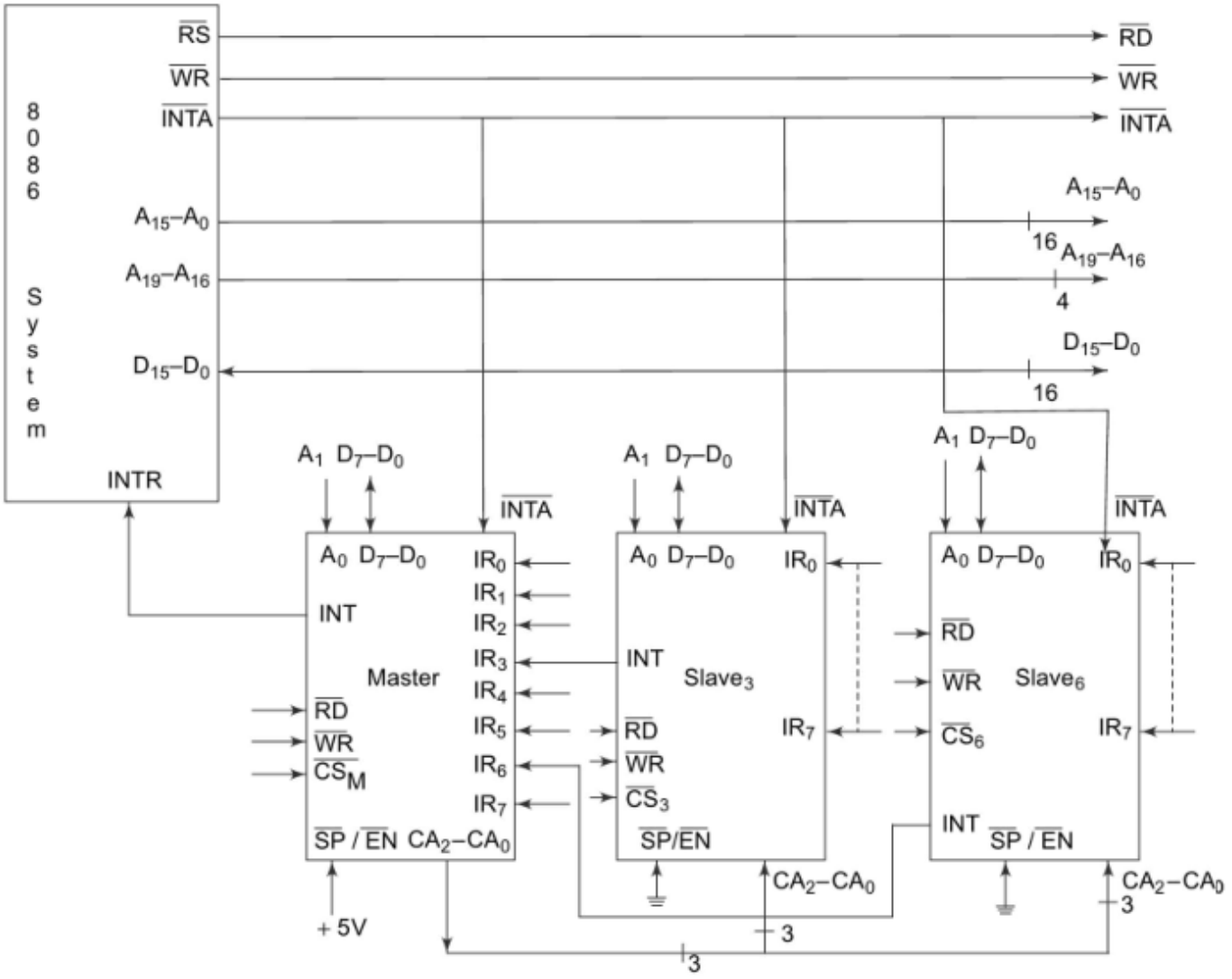
Interface with 8259A



8259A Block Diagram



Cascaded 8259A



Max 64

Addressing 8259A

- **Only Two Addresses per 8259A.**

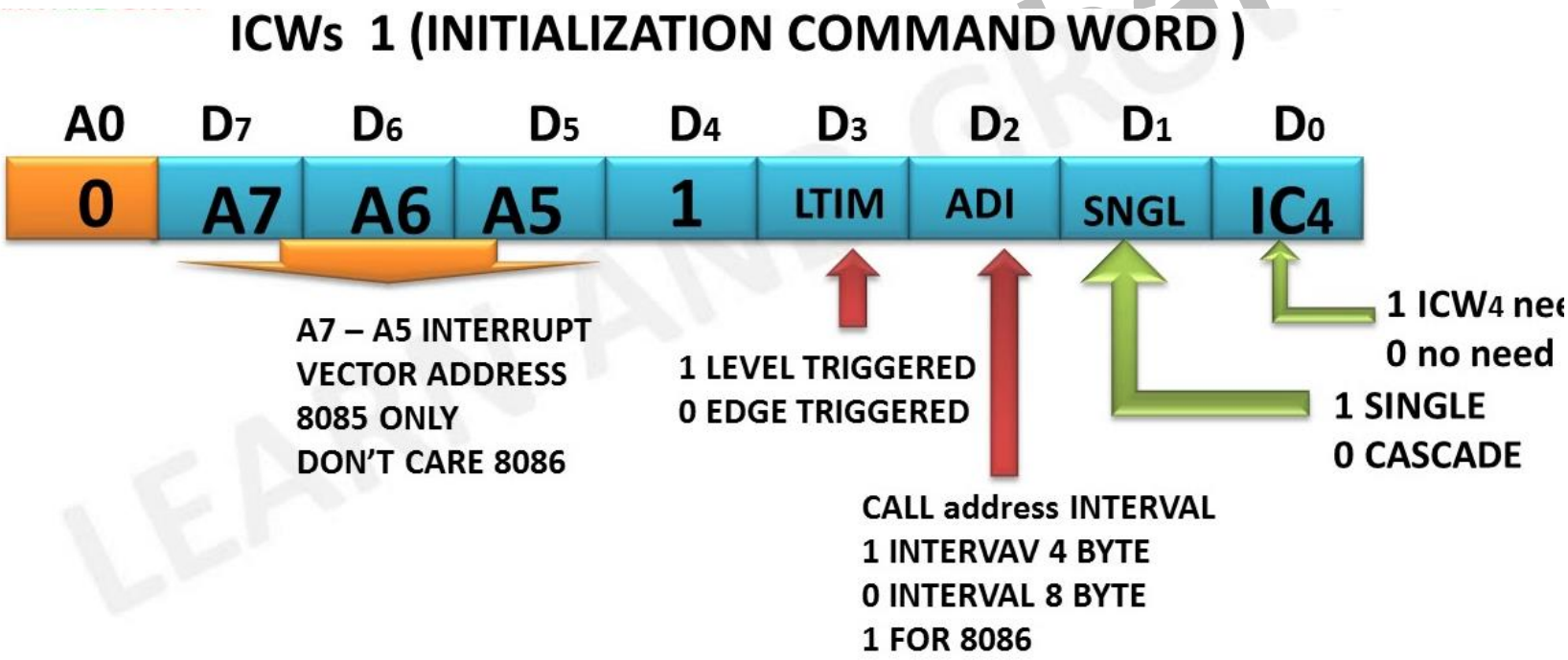
  - **INITIALIZATION COMMAND WORDS (ICWS)**

    ICW 1, ICW 2, ICW 3, & IC4

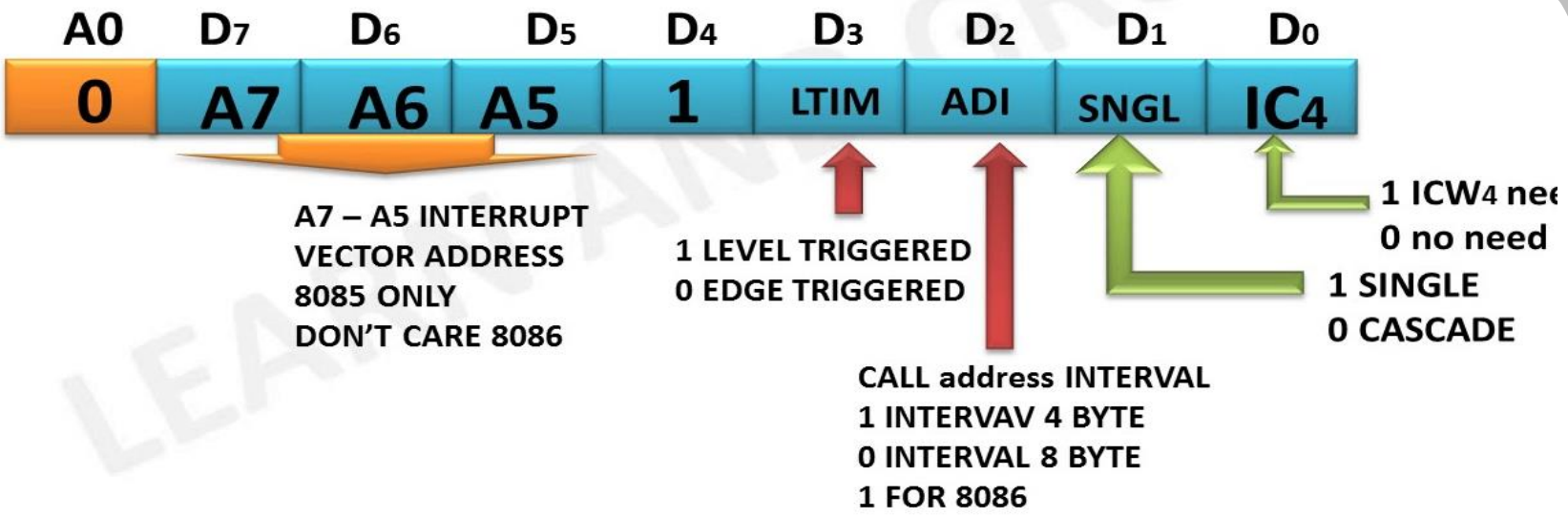
  - **Operation Command Words (OCWs):**
    OCW 1, OCW 2 & ICW 3

8259A ICWs

ICW1 : Mandatory



8259A ICWs

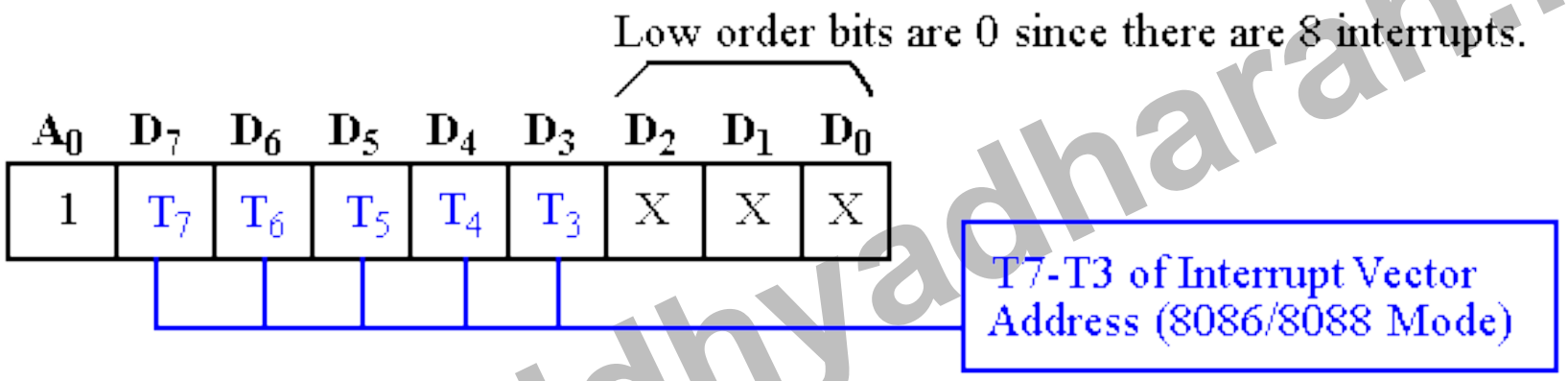


WAP to initialize Single 8259 as follows
Edge triggered,
Single,
Auto EOI Mode,
Buffered Mode,
Mask IR3, IR4, IR5, IR6,
Vector number of IR0 is 40H.
Assume 8259 is at Port Address 80H.

```
Start: MOV AL, 17H
       OUT  80H, AL
```

8259A ICWs

ICW2 : Mandatory



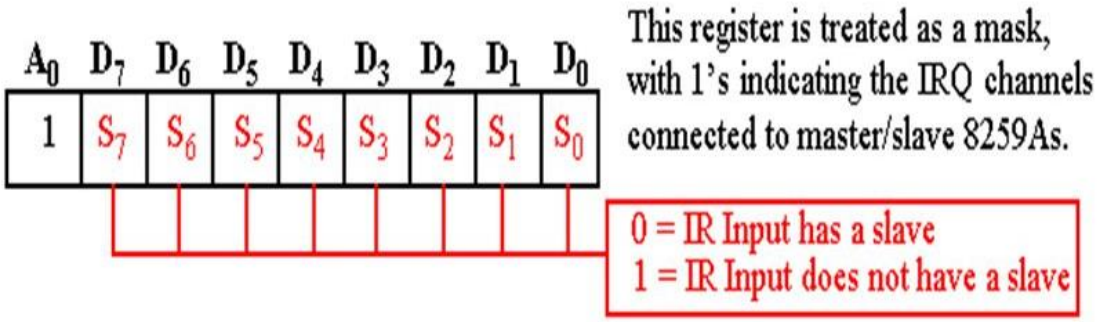
WAP to initialize Single 8259 as follows
Edge triggered,
Single,
Auto EOI Mode,
Buffered Mode,
Mask IR3, IR4, IR5, IR6,
Vector number of IR0 is 40H.
Assume 8259 is at Port Address 80H.

```
Start: MOV AL, 17H
       OUT  80H, AL

       MOV  AL, 40H
       OUT  82H, AL
```

8259A ICWs

ICW3 : Dependant on ICW 1 (Mandatory if Cascade selected in ICW1)




```
WAP to initialize Single 8259 as follows
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Buffered Mode,
Mask IR3, IR4, IR5, IR6,
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Assume 8259 is at Port Address 80H.
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8259A ICWs

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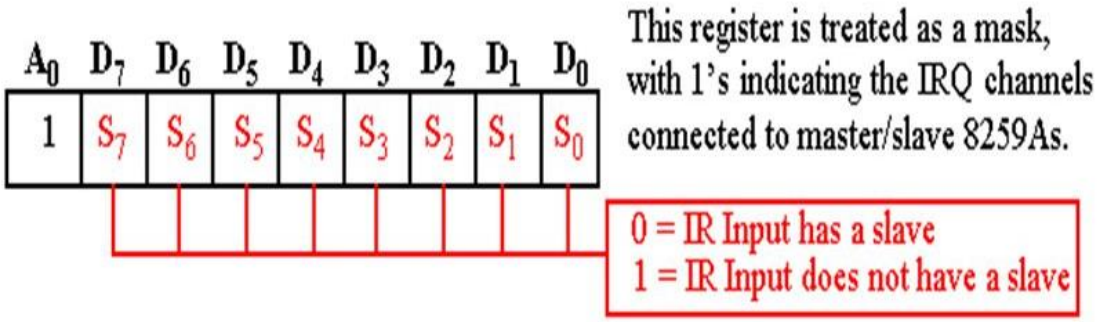

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Edge triggered,
Single,
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Buffered Mode,
Mask IR3, IR4, IR5, IR6,
Vector number of IR0 is 40H.
Assume 8259 is at Port Address 80H.

```
Start: MOV AL, 17H
       OUT  80H, AL

       MOV  AL, 40H
       OUT  82H, AL
```

8259 ICWs

ICW3 : Dependant on ICW 1 (Mandatory if Cascade selected in ICW1)

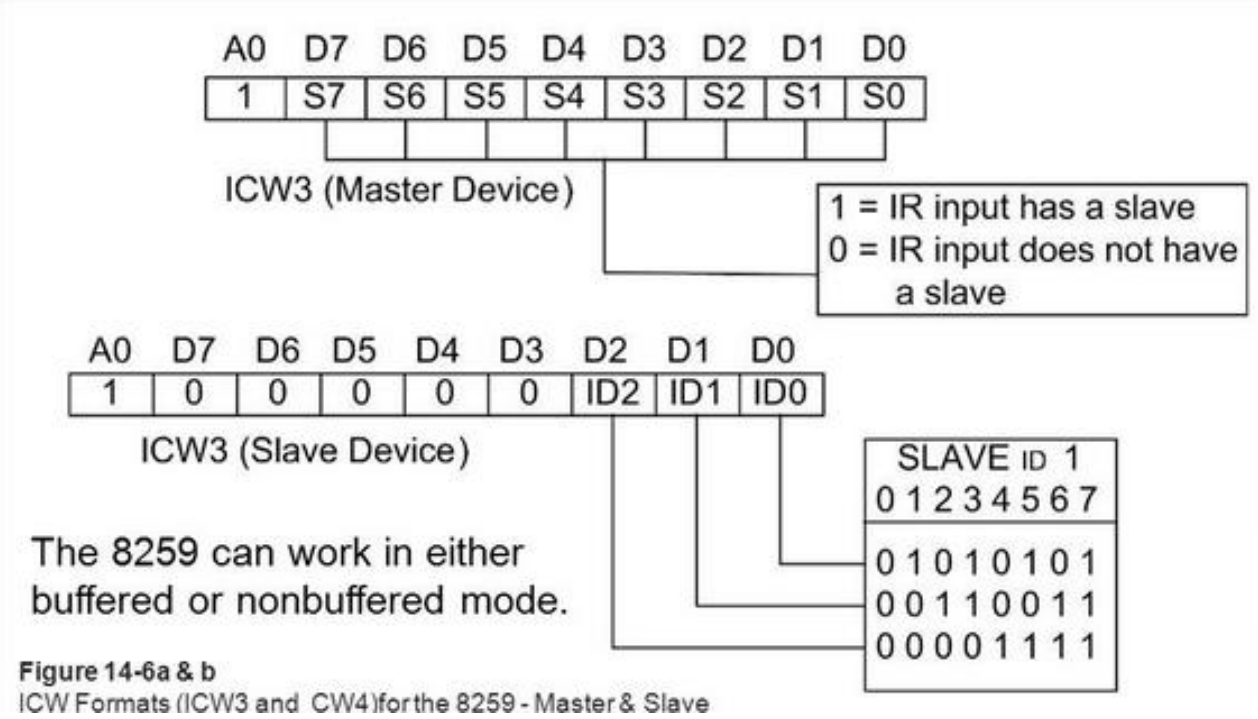
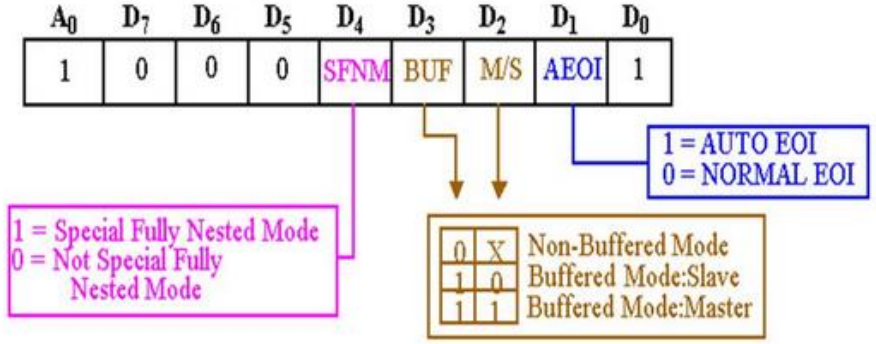


Figure 14-6a & b
ICW Formats (ICW3 and CW4) for the 8259 - Master & Slave

8259 ICWs

ICW4 : Dependant on ICW 1 (Mandatory if 8086 used)



SFNM :1 for Fully nested
Cascade: 0/1
SFNM :0 for Single

D_0-0 for 8085
D_0-1 for 8086

Normal EOI- D_1-0
ISR has EOI
Auto EOI : D_1-1

After sending vector ISR register set 0

WAP to initialize Single 8259 as follows
Edge triggered,
Single,
Auto EOI Mode,
Buffered Mode,
Mask IR3, IR4, IR5, IR6,
Vector number of IR0 is 40H.
Assume 8259 is at Port Address 80H.

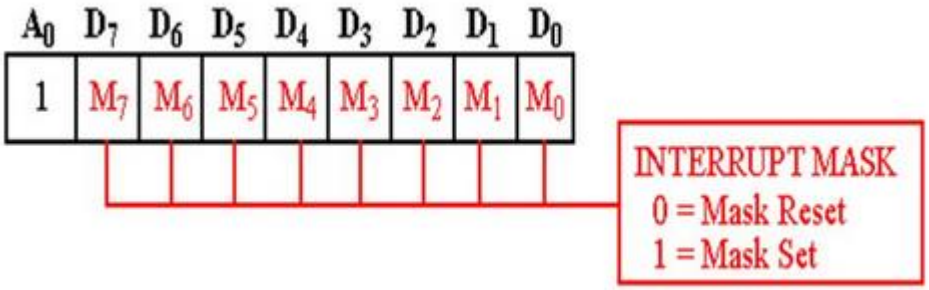
```
Start: MOV AL, 17H
       OUT  80H, AL

       MOV  AL, 40H
       OUT  82H, AL

       MOV  AL, 0FH
       OUT  82H, AL
```

8259 OCWs

OCW1 : Non-Mandatory




```
Start: MOV AL, 17H
       OUT  80H, AL

       MOV  AL, 40H
       OUT  82H, AL

       MOV  AL, 0FH
       OUT  82H, AL

       MOV  AL, 78H
       OUT  82H, AL

       INT  03H

Code ENDS

     END Start
```

WAP to initialize Single 8259 as follows
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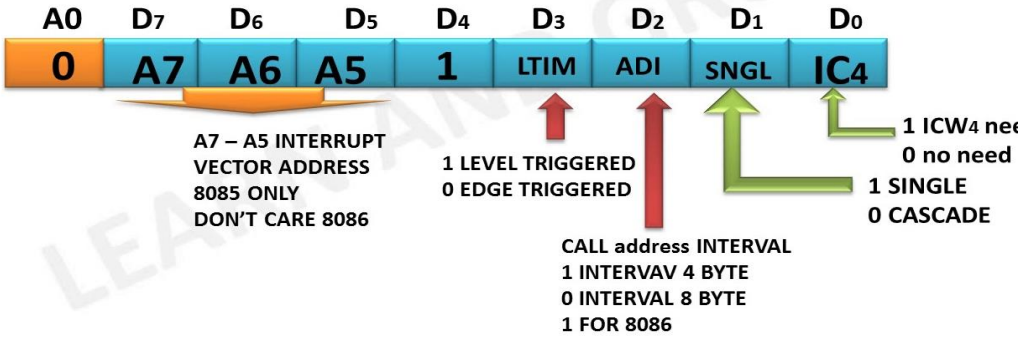
Buffered Mode,
Mask IR3, IR4, IR5, IR6,
Vector number of IR0 is 40H.
Assume 8259 is at Port Address 80H.

Problem

Q 2) **WAP to initialize Cascaded 8259.**
One Master, two slaves connected on IR2 and IR3 of master.
Master: Port address 80H. Vector Number of IR6 is 46H. Edge triggered. AEOI Mode.
SFNM. Keyboard Interrupt connected on IR4.
Slave2: Port address 84H. Vector Number of IR0 is 50H. Level triggered.
Normal EOI Mode. Printer Interrupt on IR0. Card Reader Interrupt on IR1.
Slave3: Port address 90H. Vector Number of IR6 is 76H. Edge triggered. AEOI Mode.
External Interrupts connected on IR0, IR1, IR2 and IR7.
For all the above 8259's, mask the unwanted interrupts.

```
Start: MOV  AL, 15H      // MASTER 8259
       OUT  80H, AL           // ICW1 = 0001 0101 = 15H
       MOV  AL, 40H
       OUT  82H, AL           // ICW2 = 0100 0000 = 40H
       MOV  AL, 0CH
       OUT  82H, AL           // ICW3 = 0000 1100 = 0CH
       MOV  AL, 1FH
       OUT  82H, AL           // ICW4 = 0001 1111 = 1FH
       MOV  AL, E3H
       OUT  82H, AL           // OCW1 = 1110 0011 = E3H
```



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For all the above 8259's, mask the unwanted interrupts.

```
Start: MOV   AL, 11H      // MASTER 8259
       OUT   80H, AL            // ICW1 = 0001 0001 = 11H
       MOV   AL, 40H
       OUT   82H, AL            // ICW2 = 0100 0000 = 40H
       MOV   AL, 0CH
       OUT   82H, AL            // ICW3 = 0000 1100 = 0CH
       MOV   AL, 1FH
       OUT   82H, AL            // ICW4 = 0001 1111 = 1FH
       MOV   AL, E3H
       OUT   82H, AL            // OCW1 = 1110 0011 = E3H
```

Low order bits are 0 since there are 8 interrupts.

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	T_7	T_6	T_5	T_4	T_3	X	X	X

T7-T3 of Interrupt Vector Address (8086/8088 Mode)

Problem

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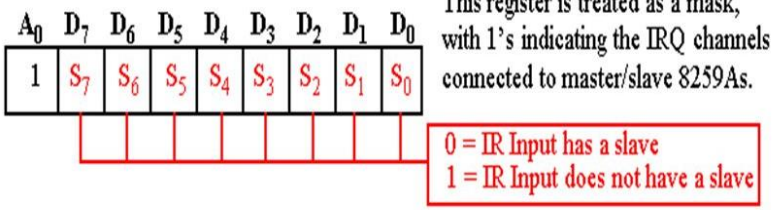

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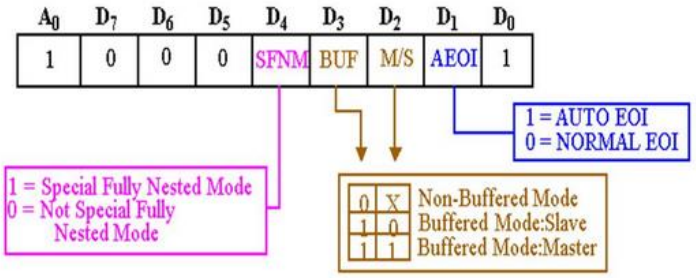

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       MOV  AL, 0CH
       OUT  82H, AL          // ICW3 = 0000 1100 = 0CH
       MOV  AL, 1FH
       OUT  82H, AL          // ICW4 = 0001 1111 = 1FH
       MOV  AL, E3H
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```

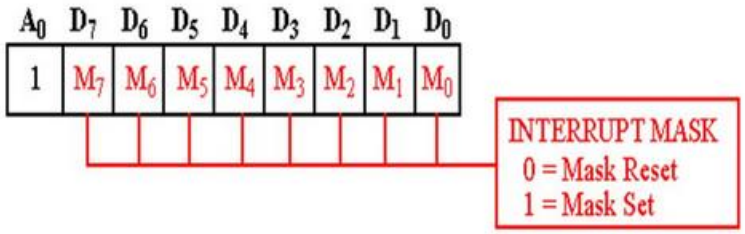

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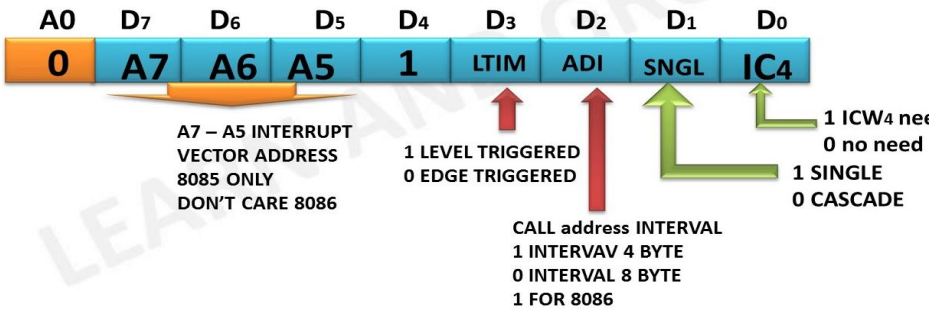
```
MOV   AL, 1DH      // SLAVE at IR2
OUT   84H, AL          // ICW1 = 0001 1101 = 1DH
MOV   AL, 50H
OUT   86H, AL          // ICW2 = 0101 0000 = 50H
MOV   AL, 02H
OUT   86H, AL          // ICW3 = 0000 0010 = 02H
MOV   AL, 09H
OUT   86H, AL          // ICW4 = 0000 1001 = 09H
MOV   AL, FCH
OUT   86H, AL          // OCW1 = 1111 1100 = FCH
```



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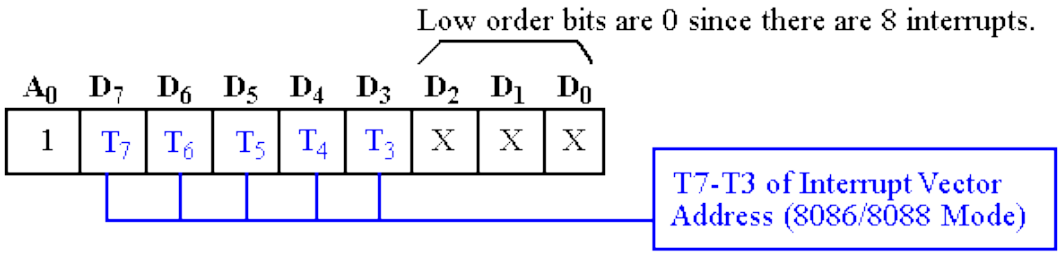

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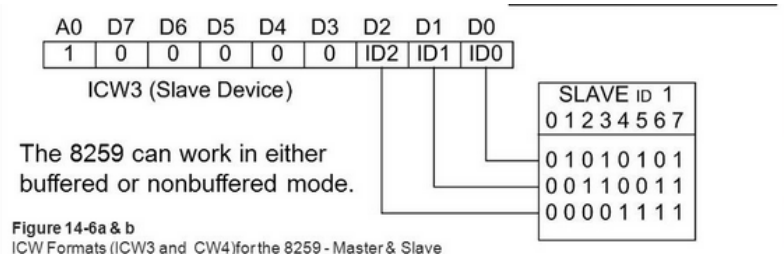

Figure 14-6a & b
ICW Formats (ICW3 and CW4) for the 8259 - Master & Slave

Problem

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MOV   AL, 09H
OUT   86H, AL           // ICW4 = 0000 1001 = 09H
MOV   AL, FCH
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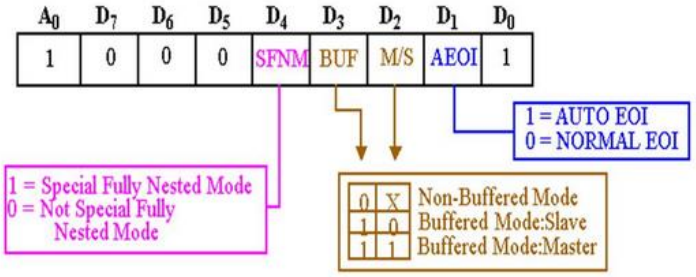
```



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MOV   AL, FCH
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```

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One Master, two slaves connected on IR2 and IR3 of master.
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For all the above 8259's, mask the unwanted interrupts.

```
        MOV   AL, 15H      // SLAVE at IR3
        OUT   90H, AL            // ICW1 = 0001 0101 = 15H
        MOV   AL, 70H
        OUT   92H, AL            // ICW2 = 0111 0000 = 70H
        MOV   AL, 03H
        OUT   92H, AL            // ICW3 = 0000 0011 = 03H
        MOV   AL, 0BH
        OUT   92H, AL            // ICW4 = 0000 1011 = 0BH
        MOV   AL, 78H
        OUT   92H, AL            // OCW1 = 0111 1000 = 78H

        INT 03H
Code    ENDS
END     Start
```

Thank You