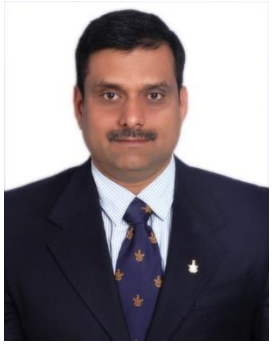
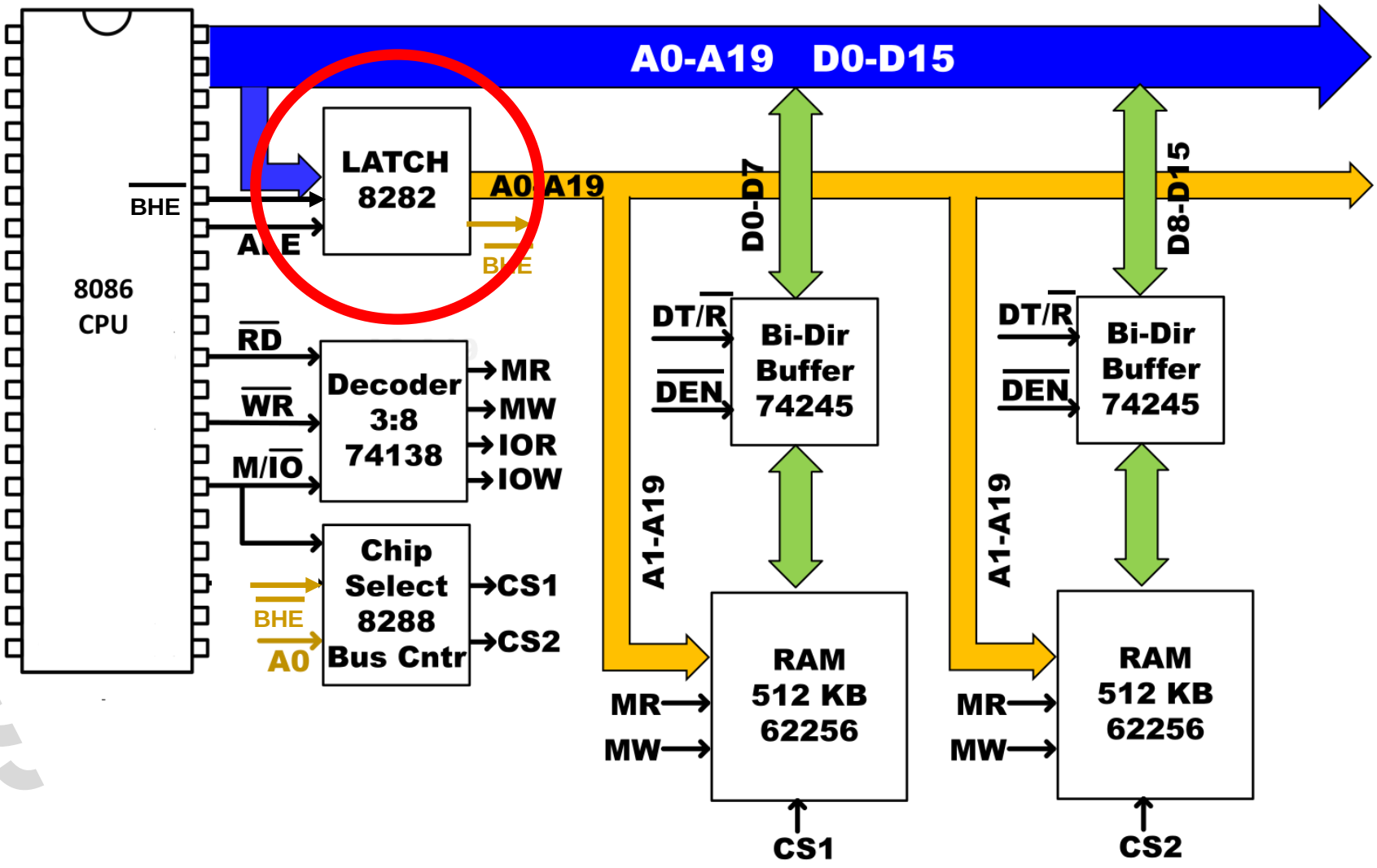
Microprocessors and Interfaces: 2021-22
Lecture 20
Bus De-Multiplexing, Chip Select Logic, Bus-Buffering, Clock Generator and Timing Diagram

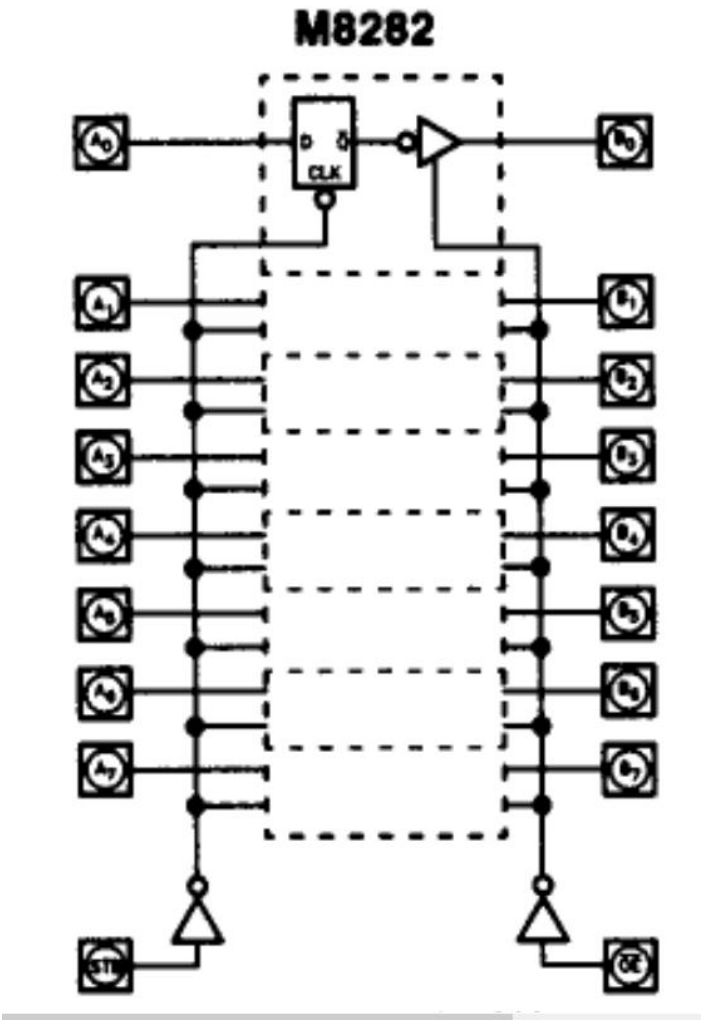
By Dr. Sanjay Vidhyadharan



Bus De-Multiplexing

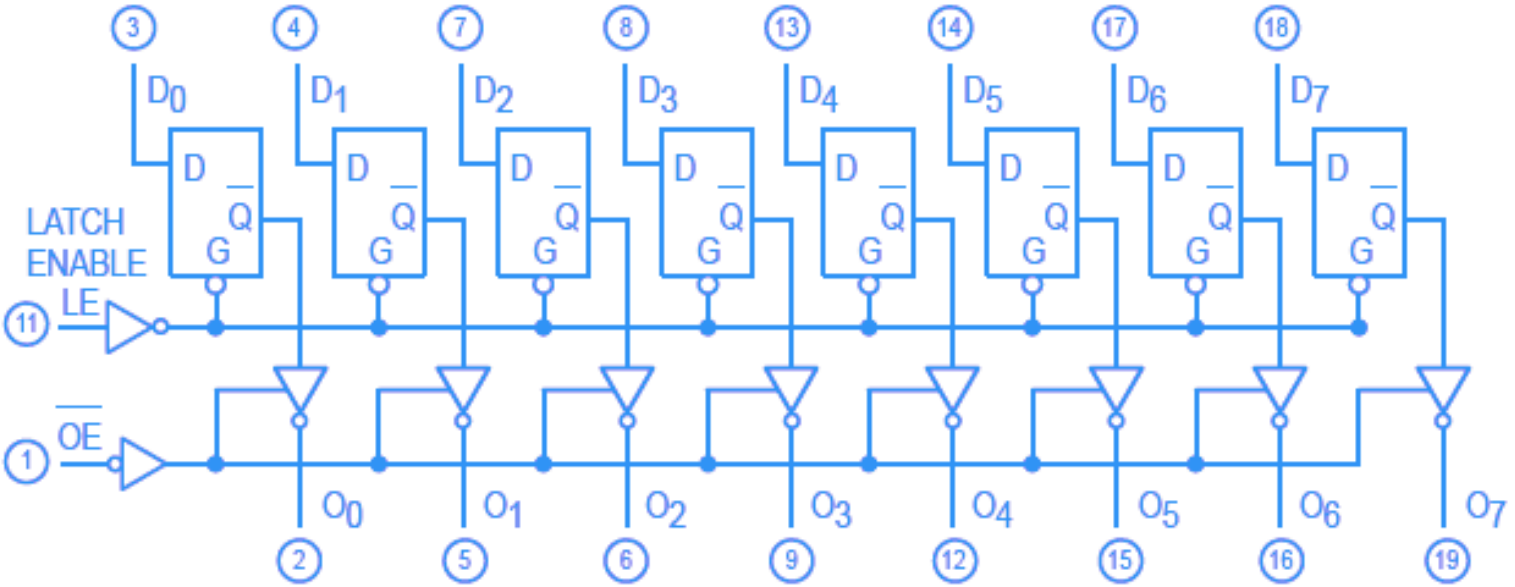


Bus De-Multiplexing

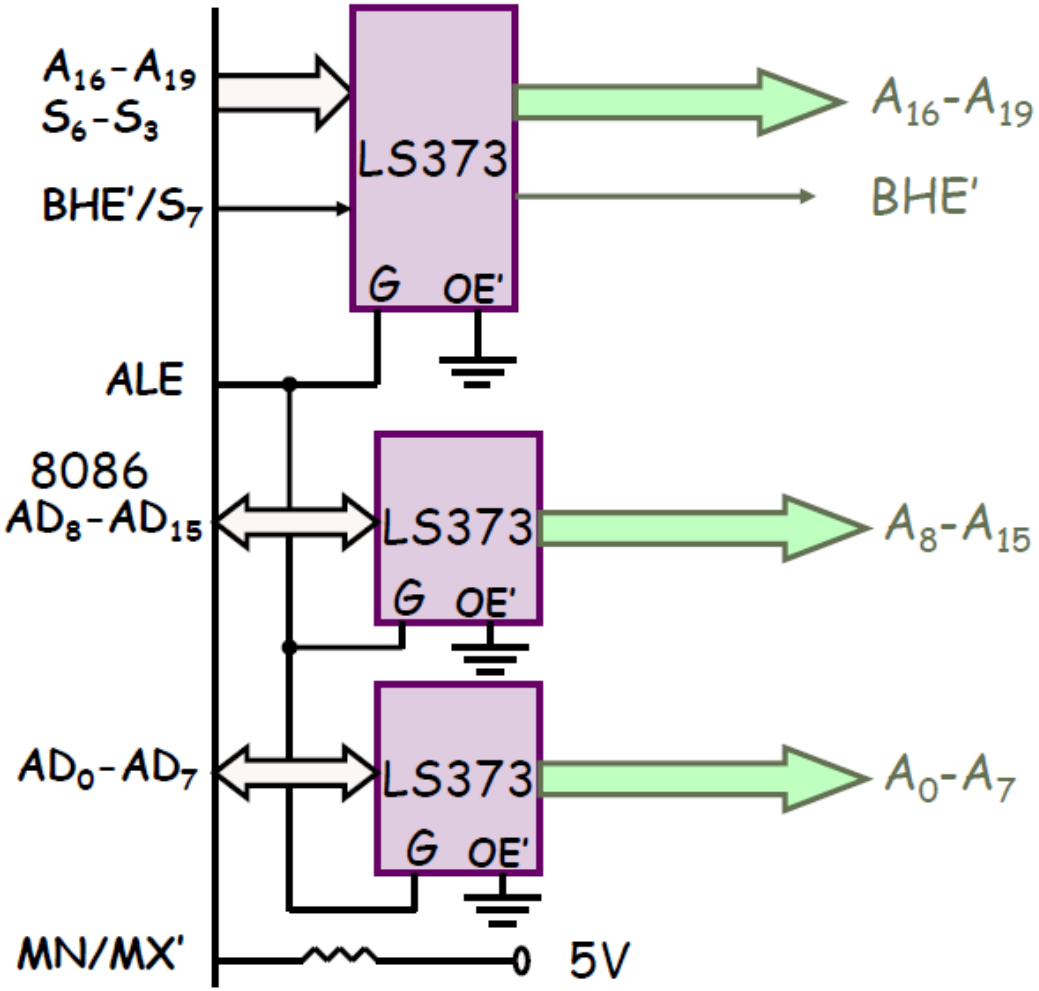


Bus De-Multiplexing

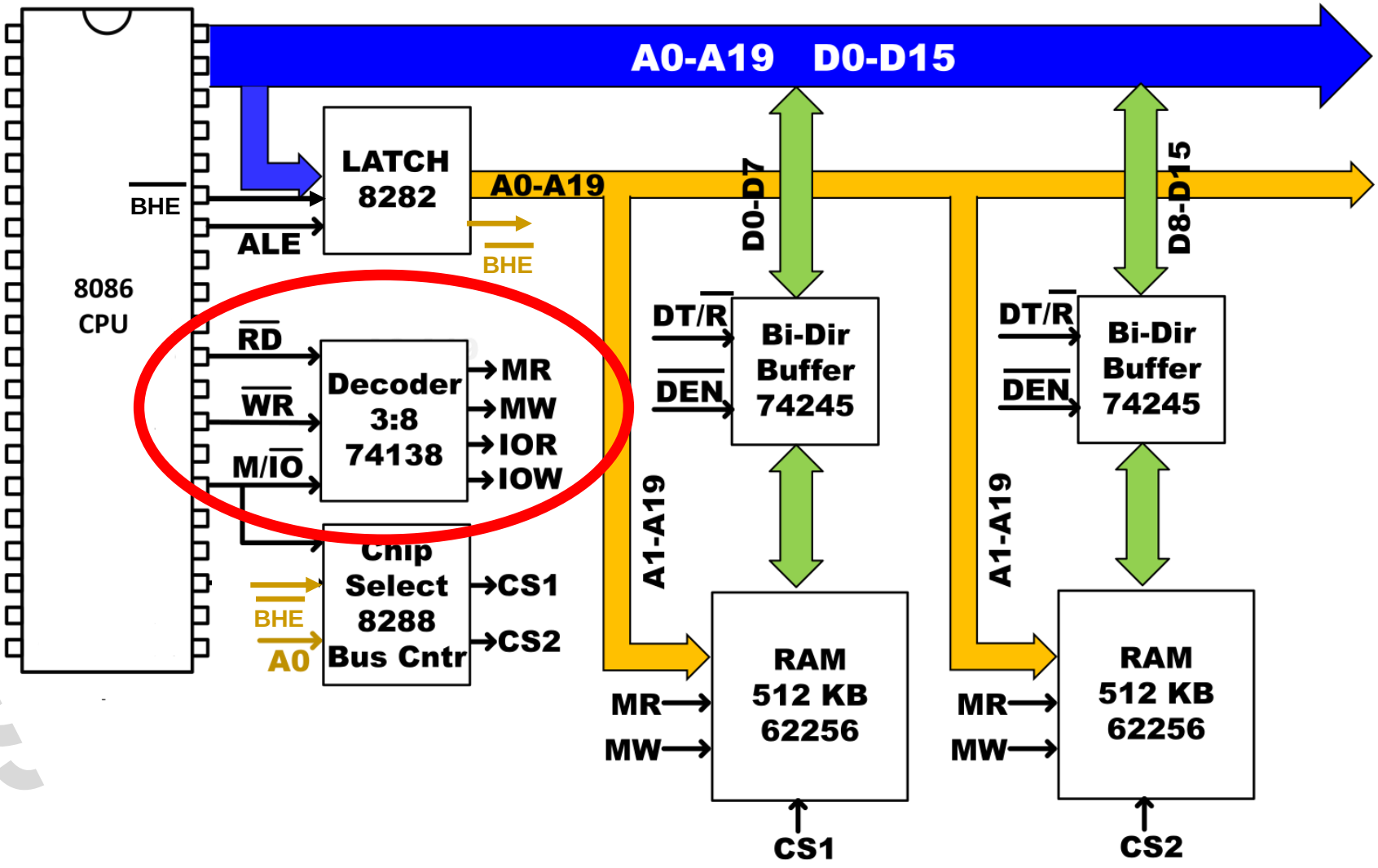
Latch IC 74LS373



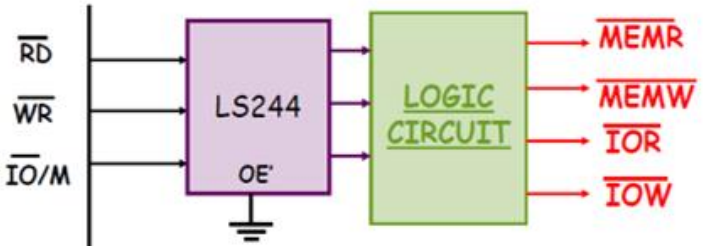
Bus De-Multiplexing



Memory / IO Chip Select Logic



Memory / IO Chip Select Logic



M/IO'	RD'	WR'	FUNCTION
1	0	1	MEMR
1	1	0	MEMW
0	0	1	IOR
0	1	0	IOW

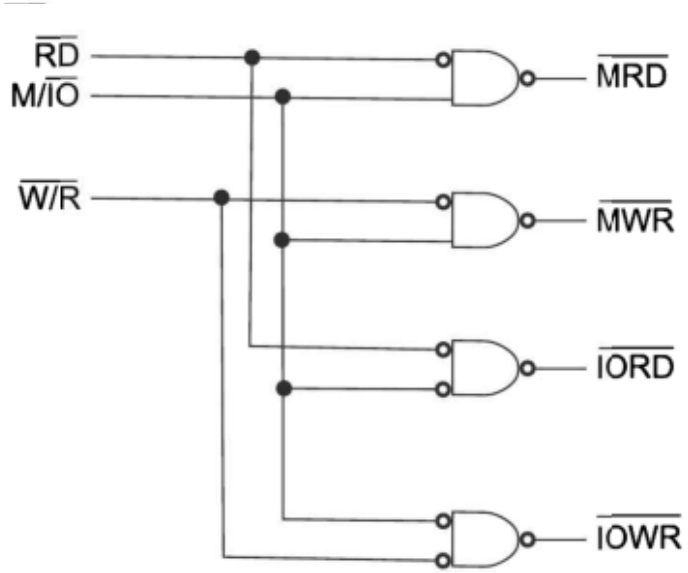


Fig. 1.12 (a) *Deriving 8086 Control Signals*

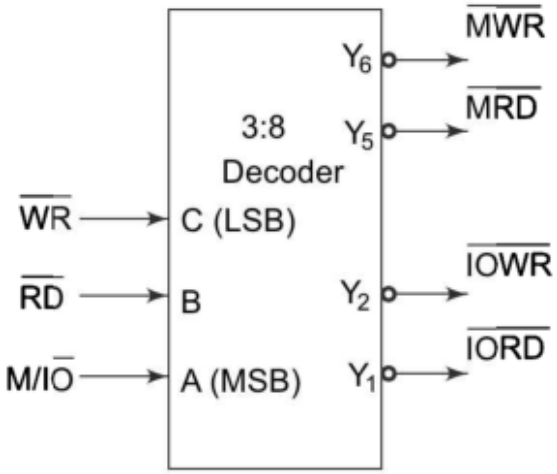
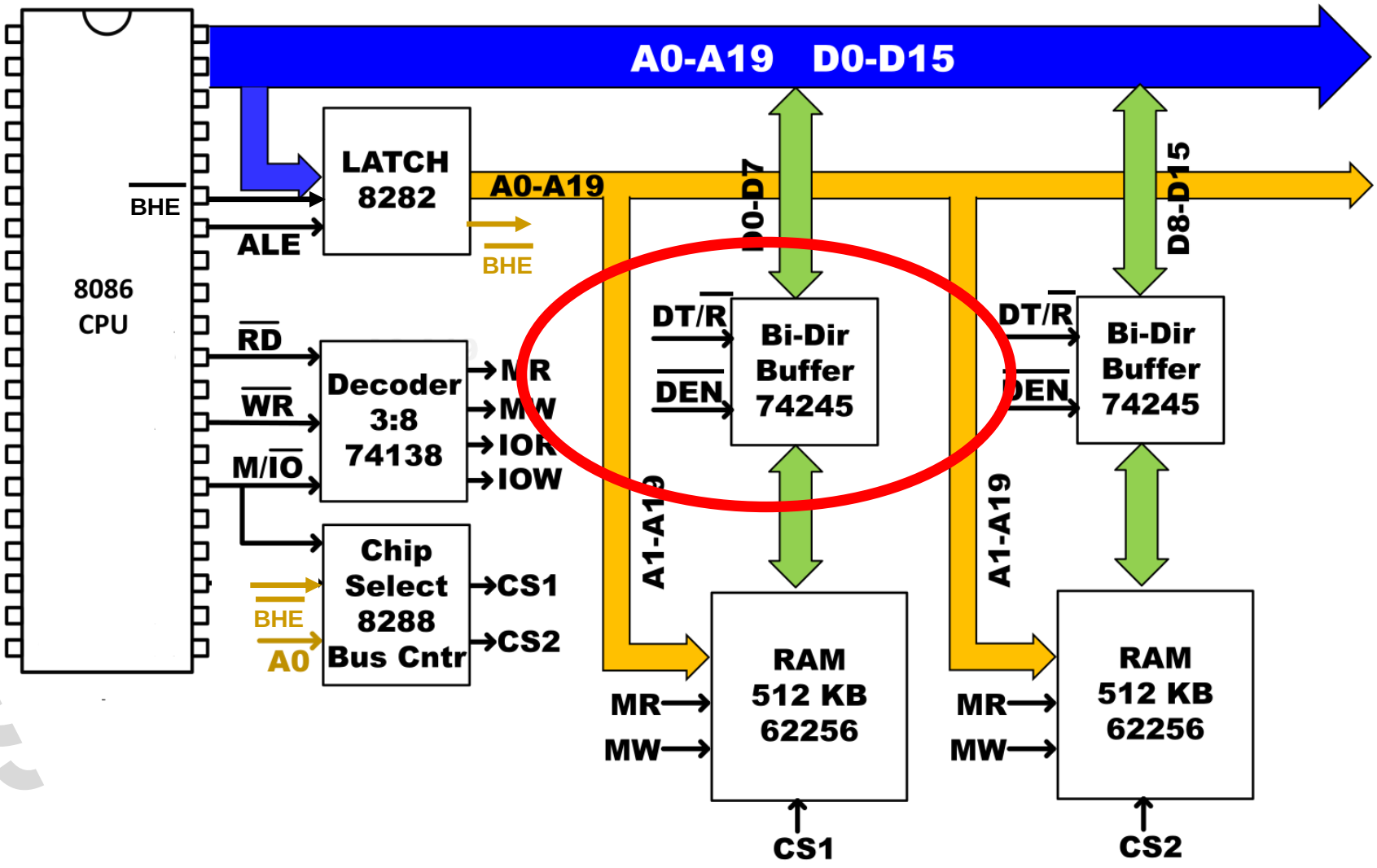


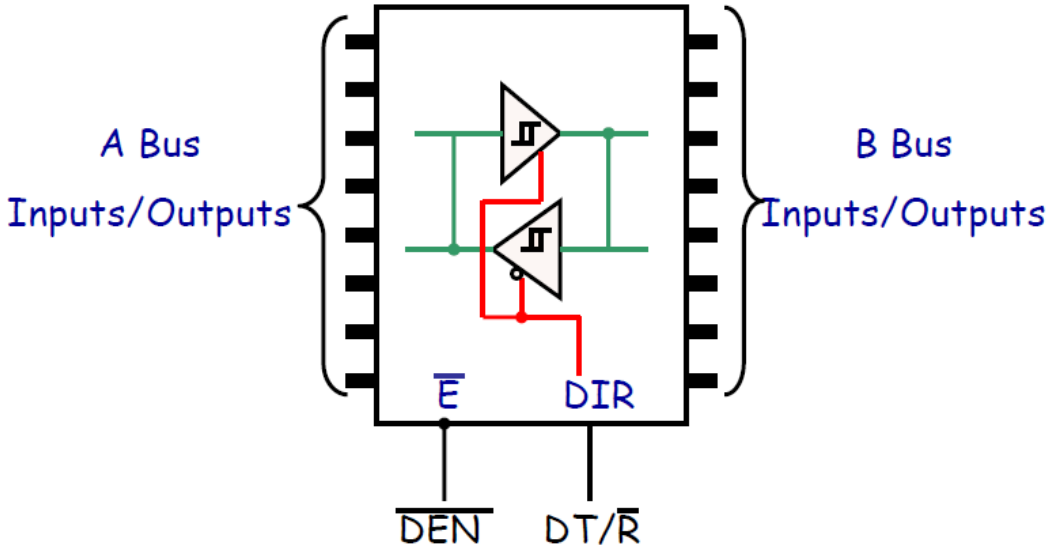
Fig. 1.12 (b) *Deriving 8086 Control Signals*

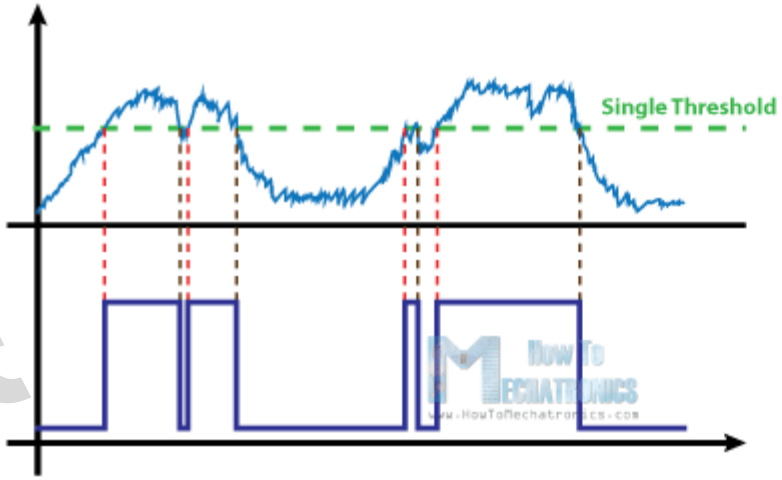
Bus Buffering

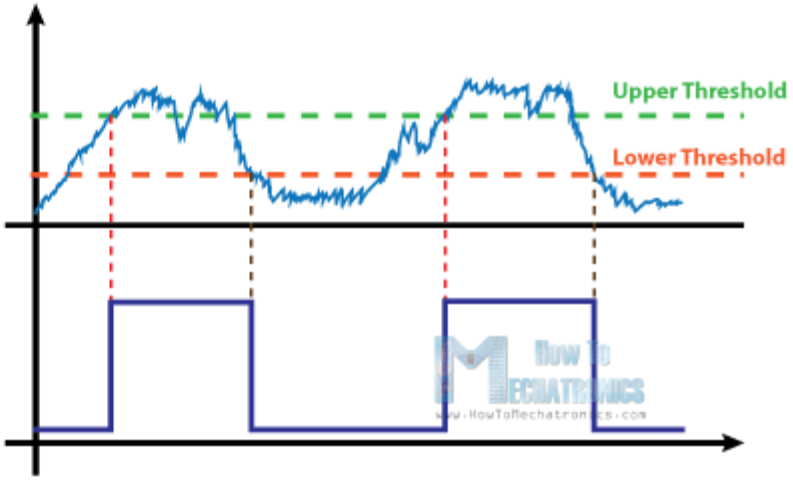


Bus Buffering

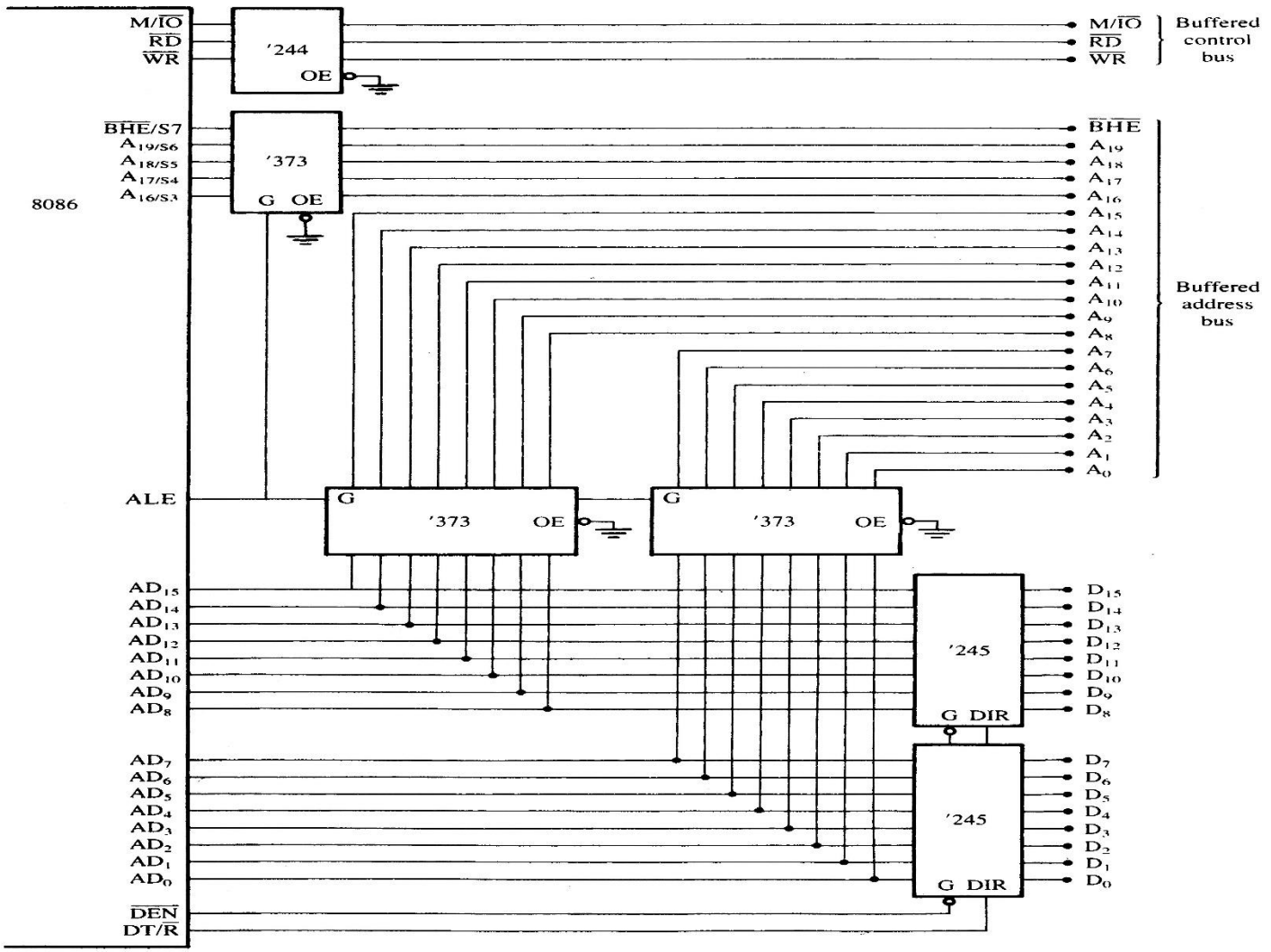
74LS245 Bi-Directional Buffer



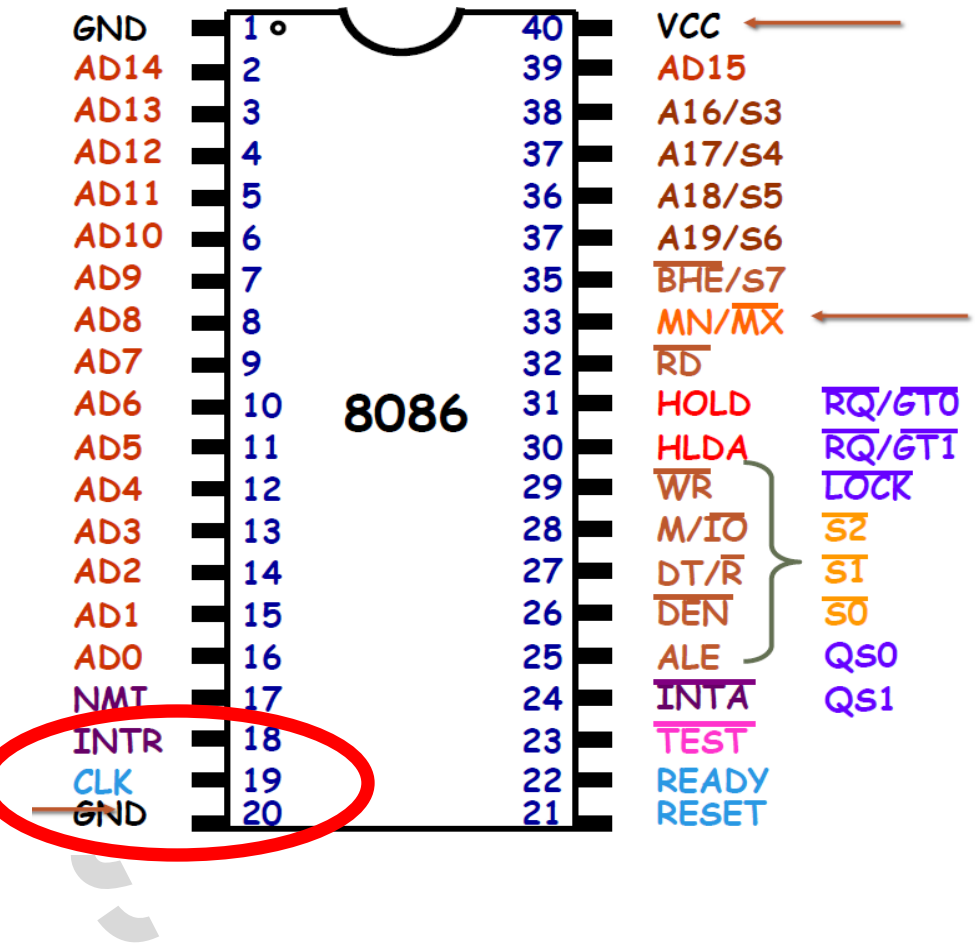




Demultiplexing the Buses

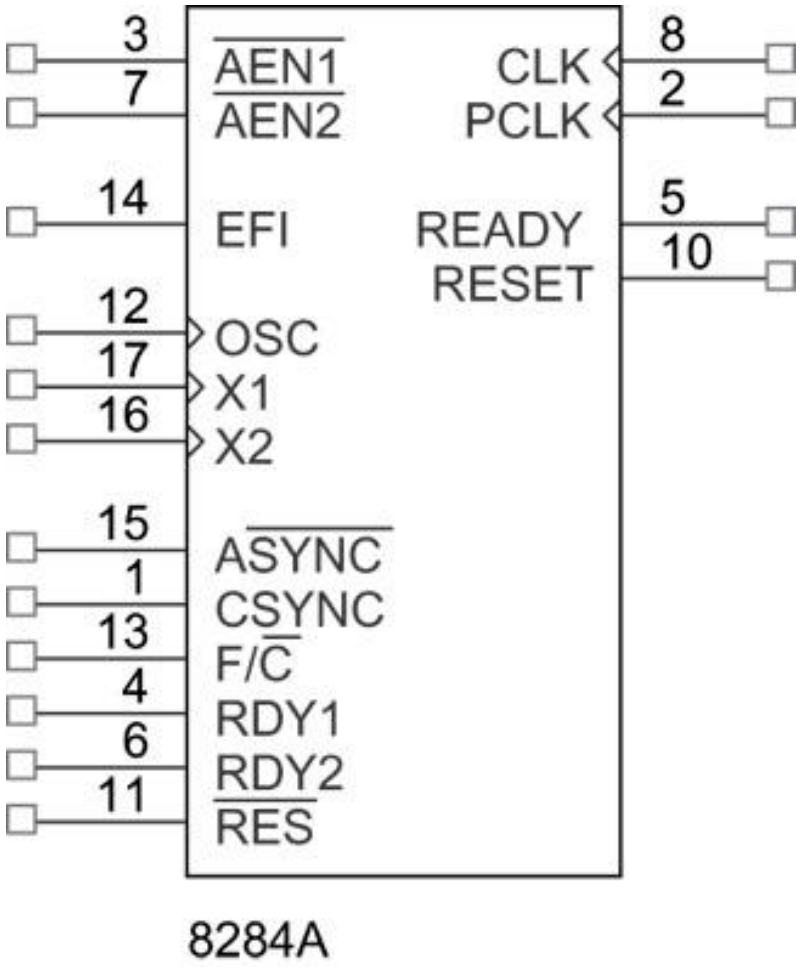


CLOCK GENERATOR (8284A)

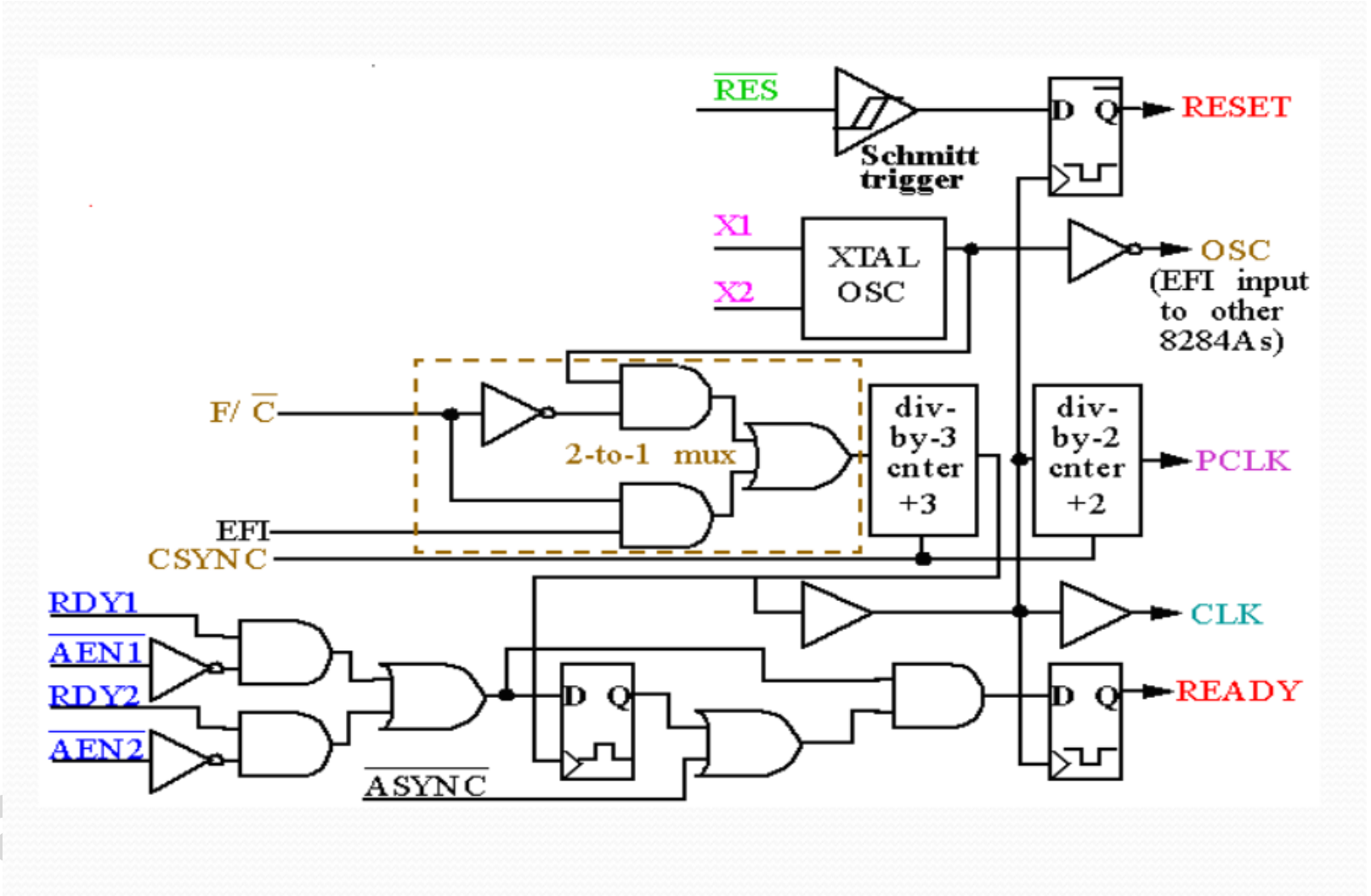


Model number	Frequency	Technology
8086	5 MHz[13]	HMOS
8086-1	10 MHz	HMOS II
8086-2	8 MHz[13]	HMOS II
8086-4	4 MHz[13]	HMOS
I8086	5 MHz	HMOS
M8086	5 MHz	HMOS

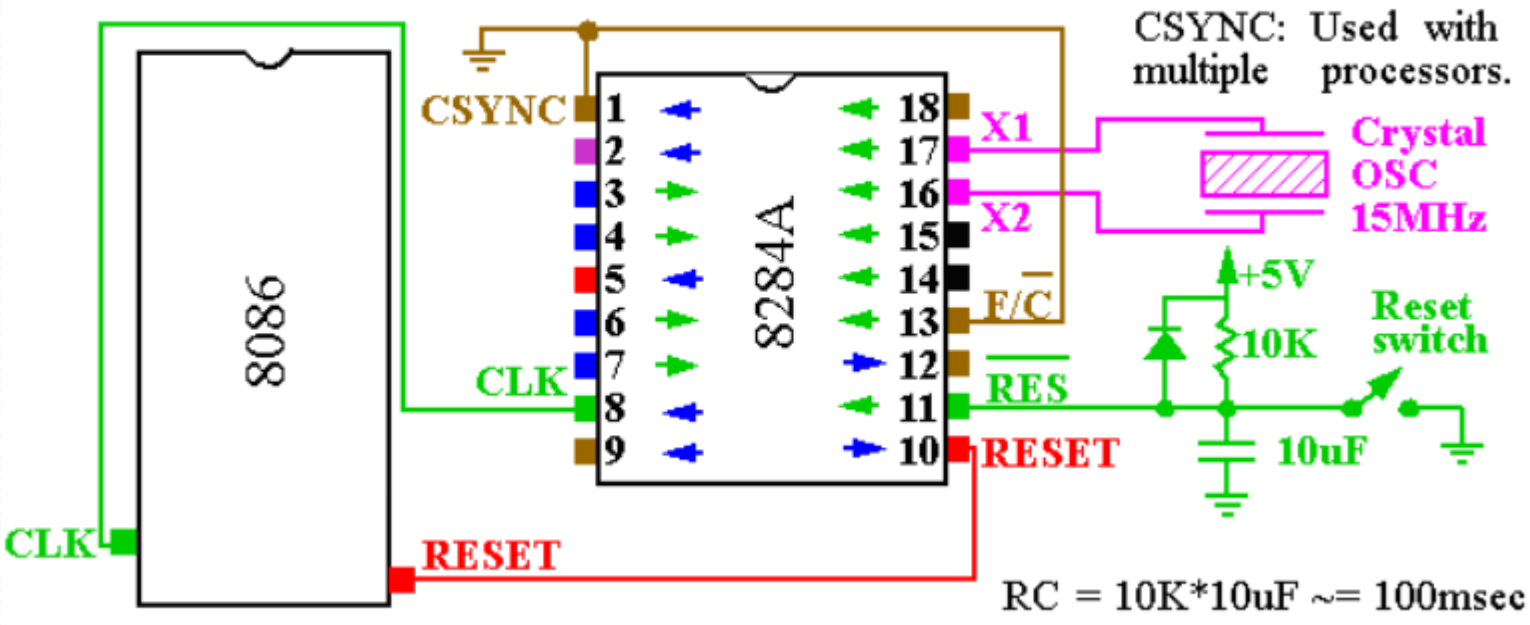
CLOCK GENERATOR (8284A)



CLOCK GENERATOR (8284A)

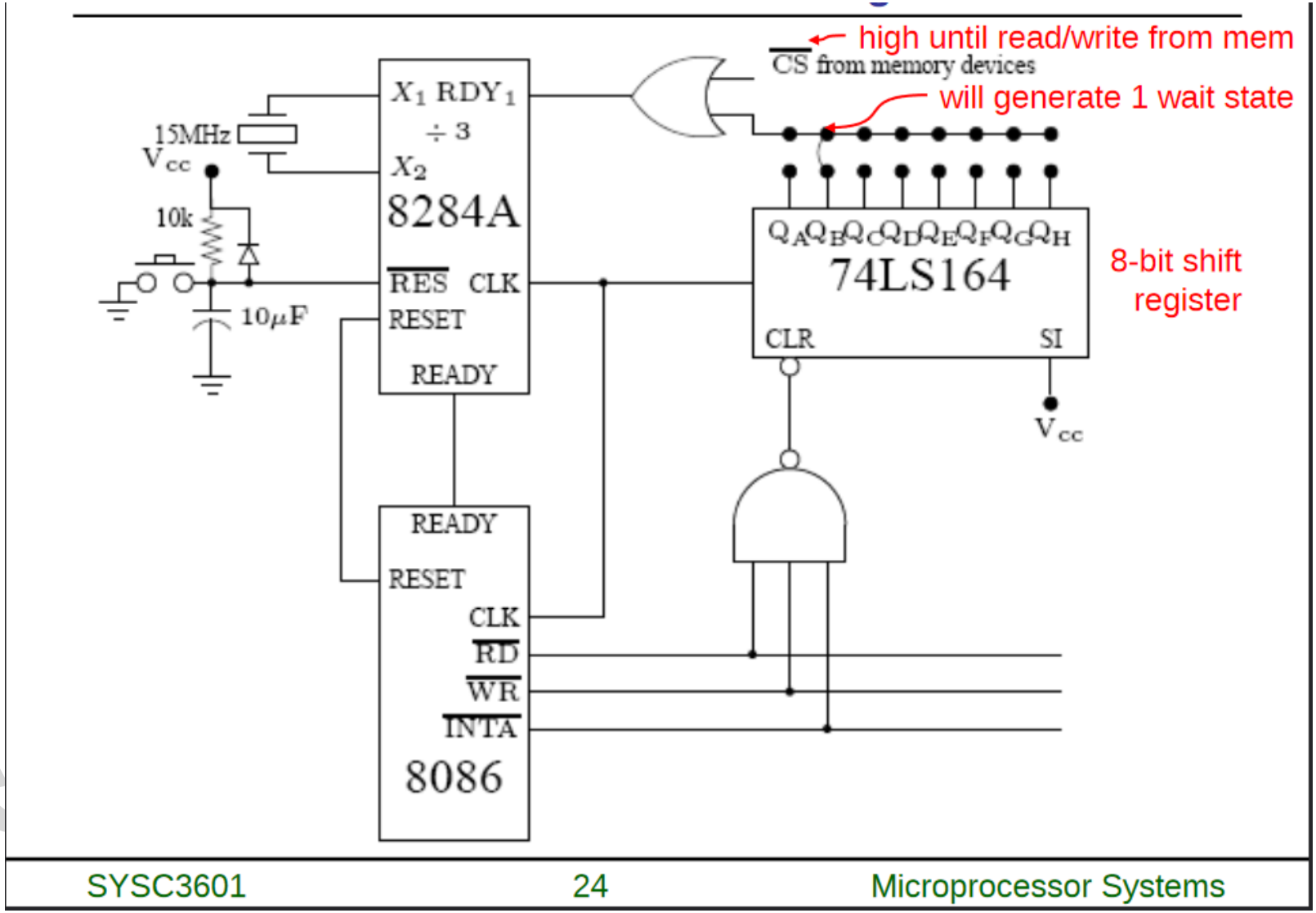


CLOCK GENERATOR (8284A)

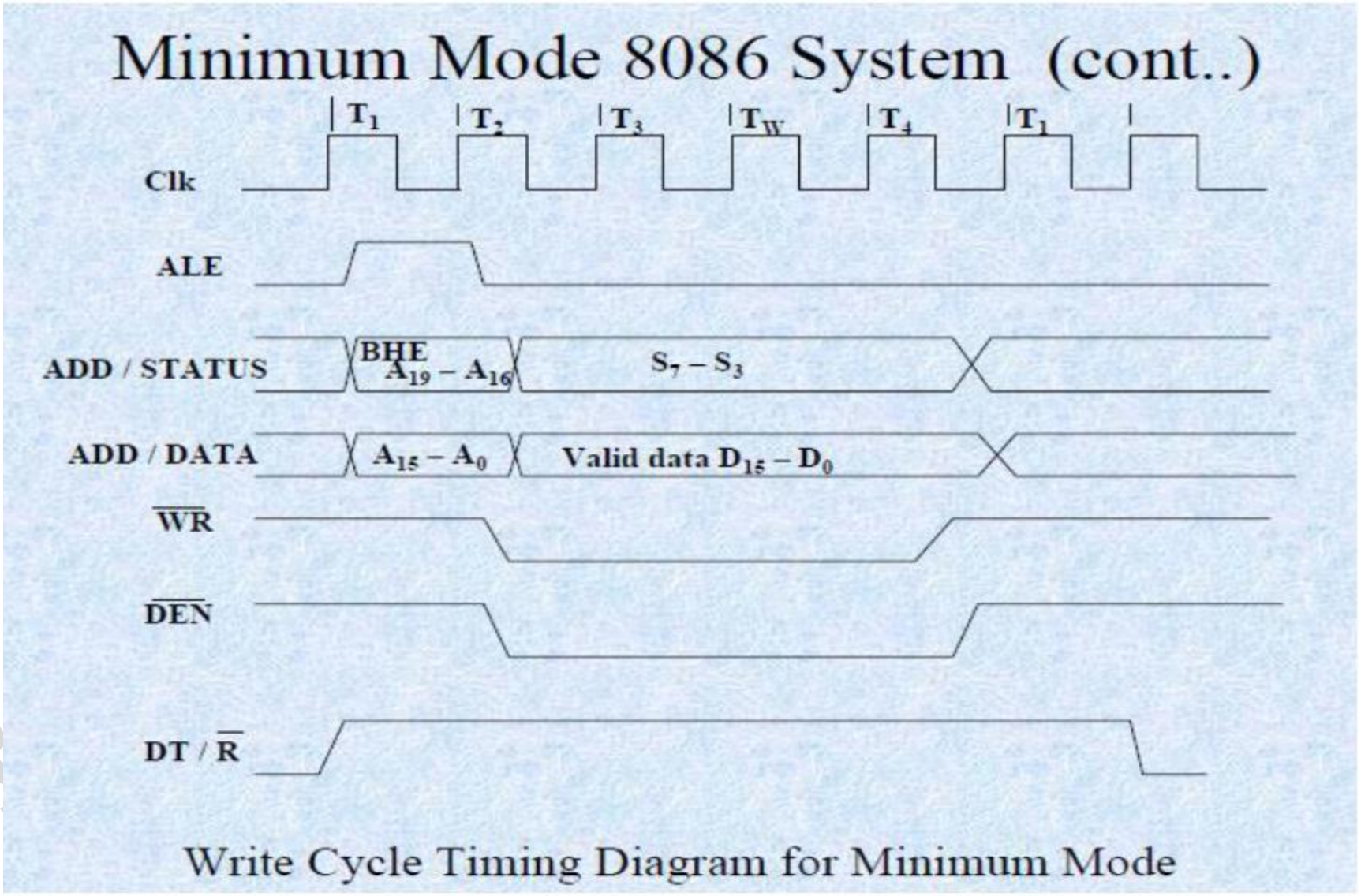


Microprocessor resets if this pin is held high for 4 clock periods. Instruction execution begins at FFFF0H and IF flag is cleared.

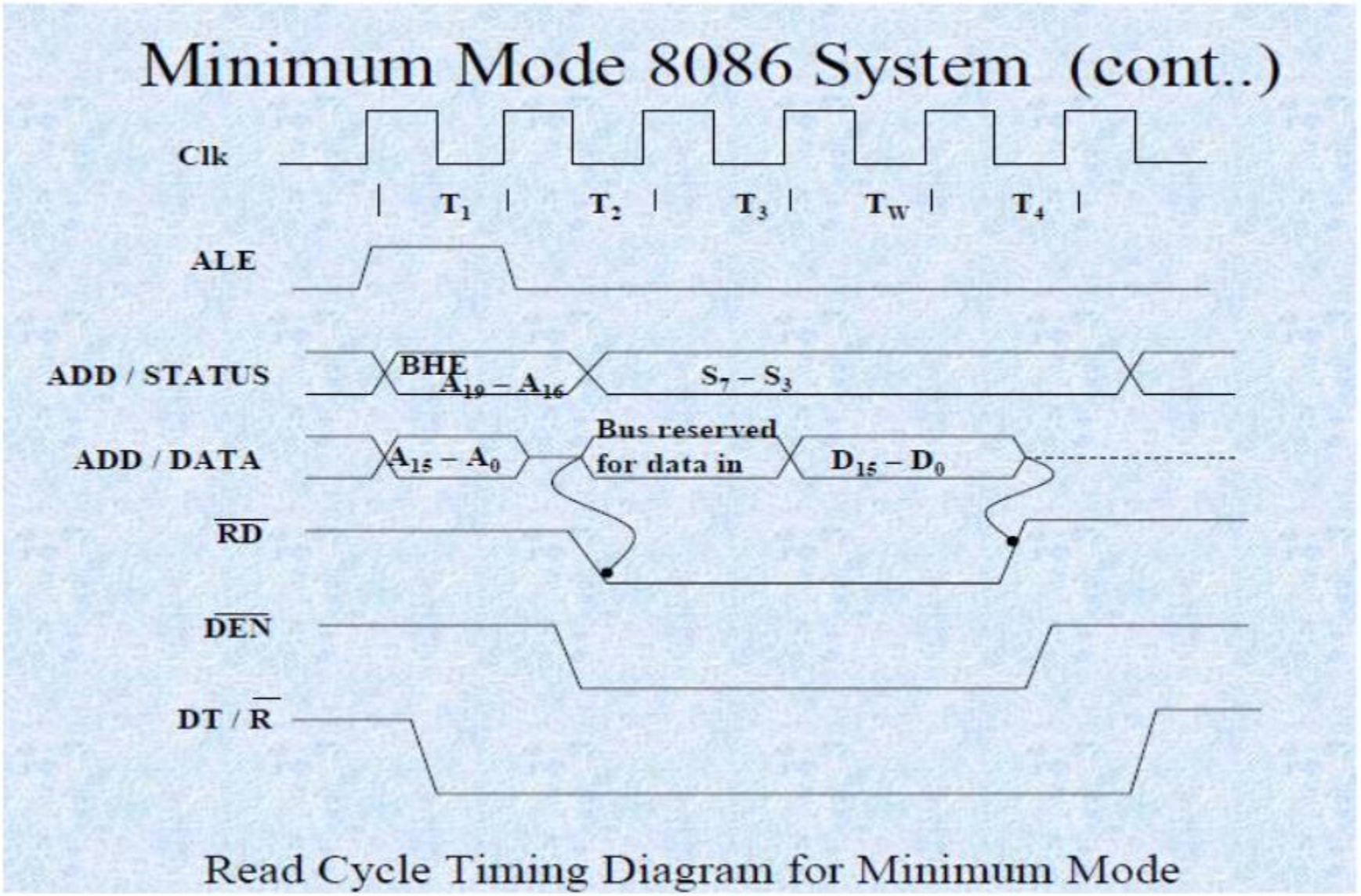
CLOCK GENERATOR (8284A)



Memory Write Operation

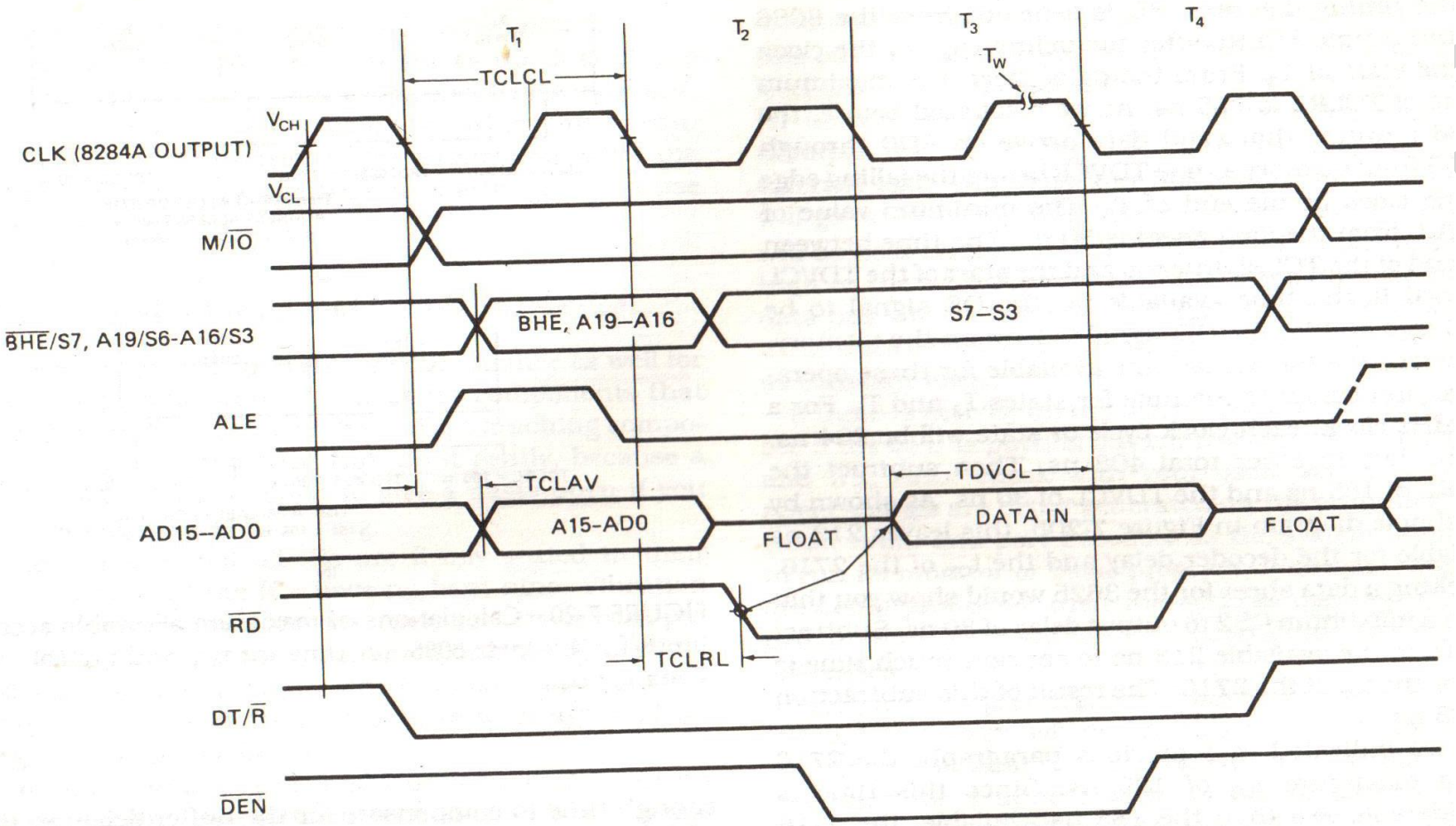


Memory Read Operation



Read Cycle Timing Diagram for Minimum Mode

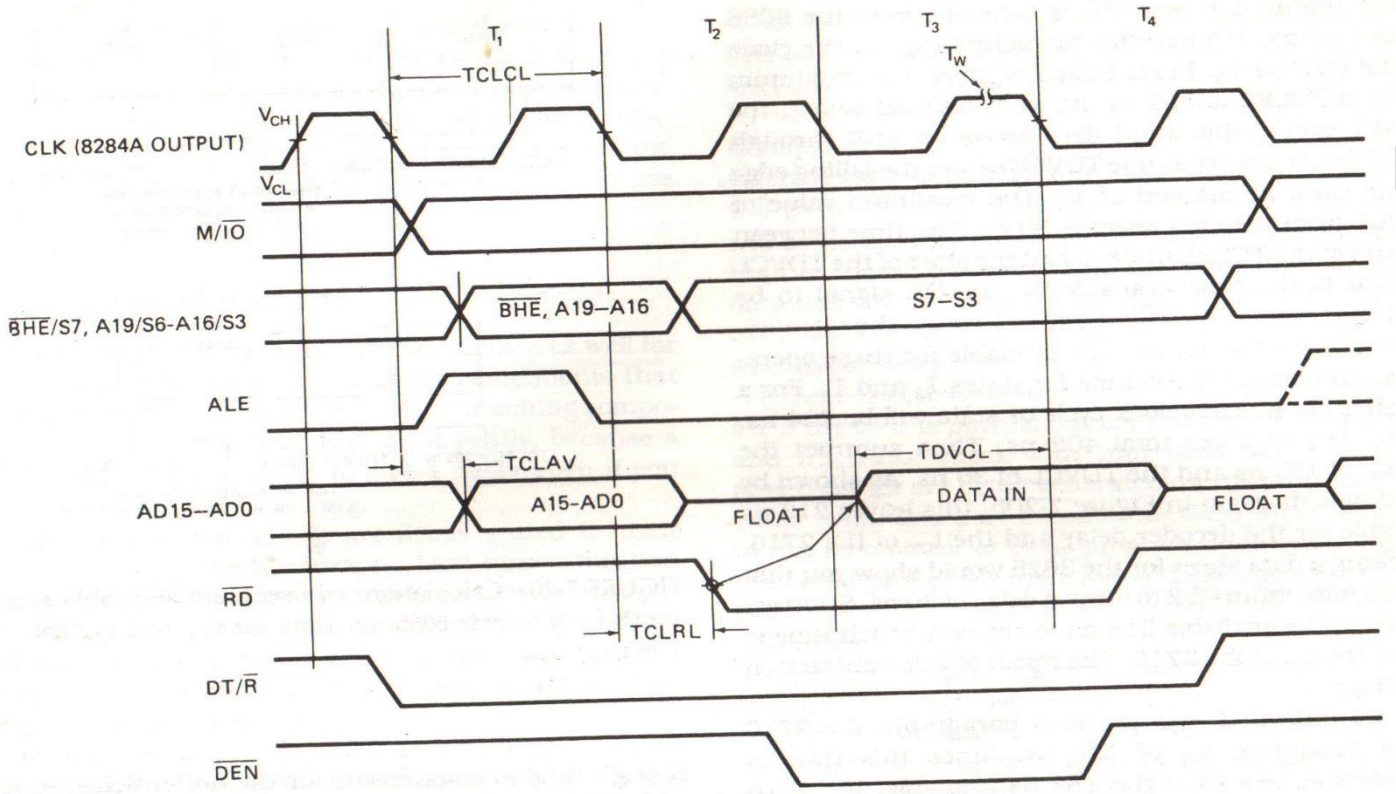
MEMORY ACCESS TIME



TCLAV- Time from Clock to Address Valid ; 110 ns for MHz Clock

Memory Access Time : TCLAV time must be subtracted from the three clocking states (600 ns) separating the appearance of the address (T_1) and the sampling of the data (T_3).

MEMORY ACCESS TIME



- TCLRL- Time from Clock to Read Line
- TDVCL – Time Data Valid to Clock 30ns
- Memory Access Time : 600 ns-110ns-30ns = 460 ns
- A wait state (T_W) is an extra clocking period between T_2 and T_3 to lengthen bus cycle
- On one wait state, memory access time of 460 ns, is lengthened by one clocking period (200 ns) to 660 ns, based on a 5 MHz clock.

Thankyou