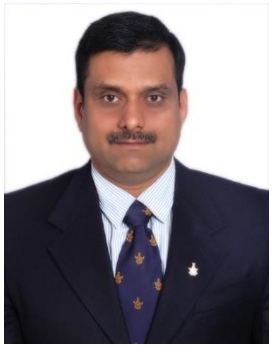
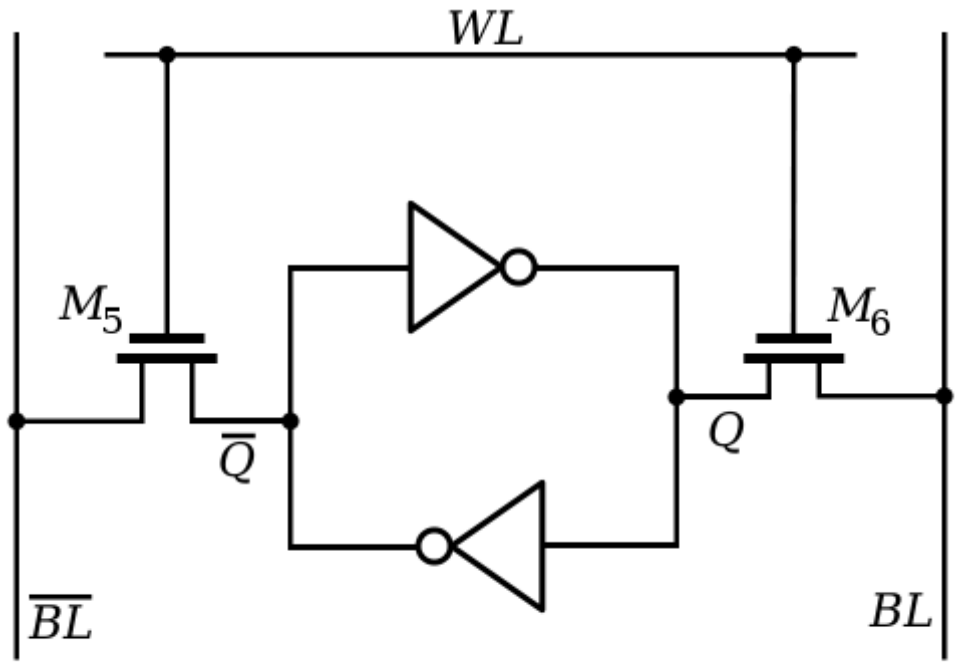
Microprocessors and Interfaces: 2021-22
Lecture 19
Memory Organisation

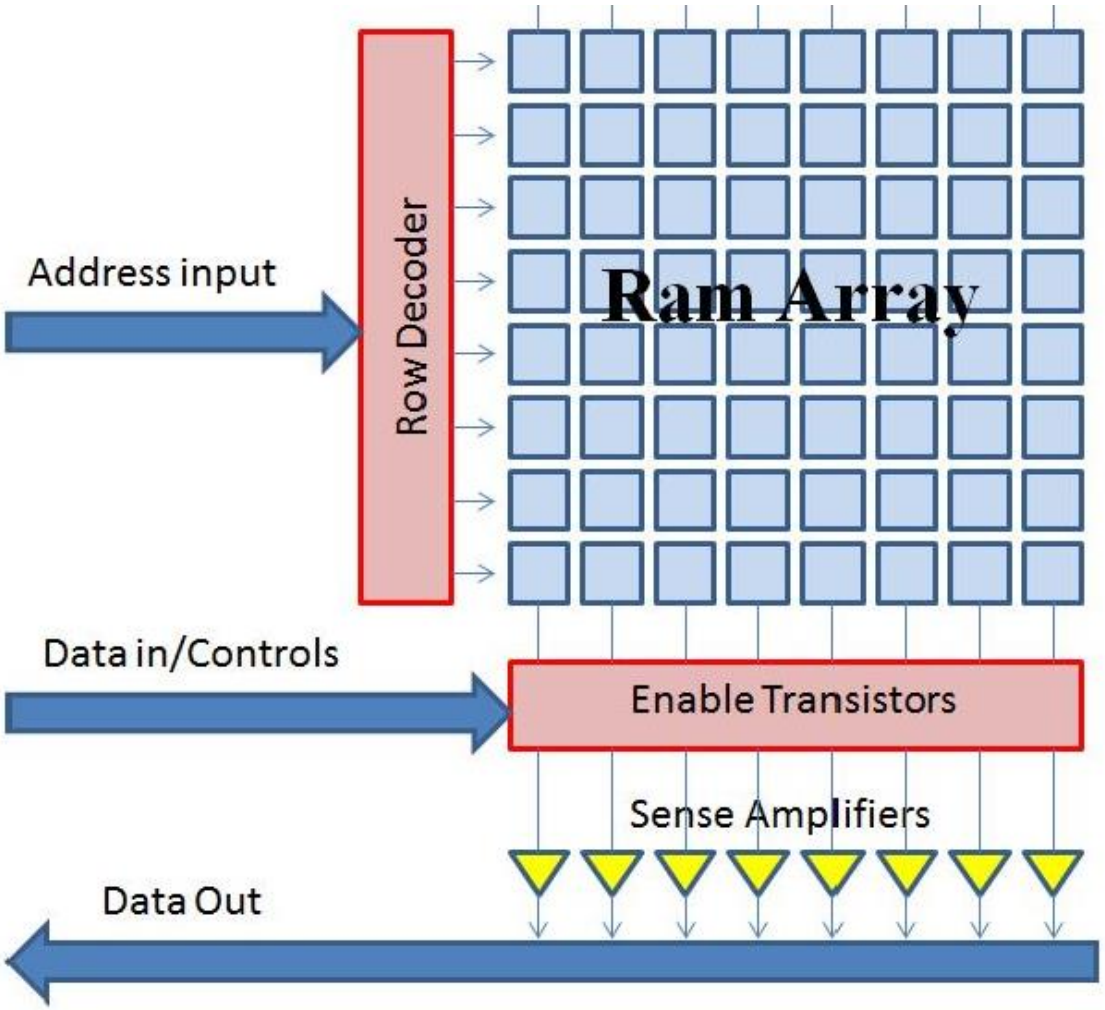
By Dr. Sanjay Vidhyadharan



RAM CELL

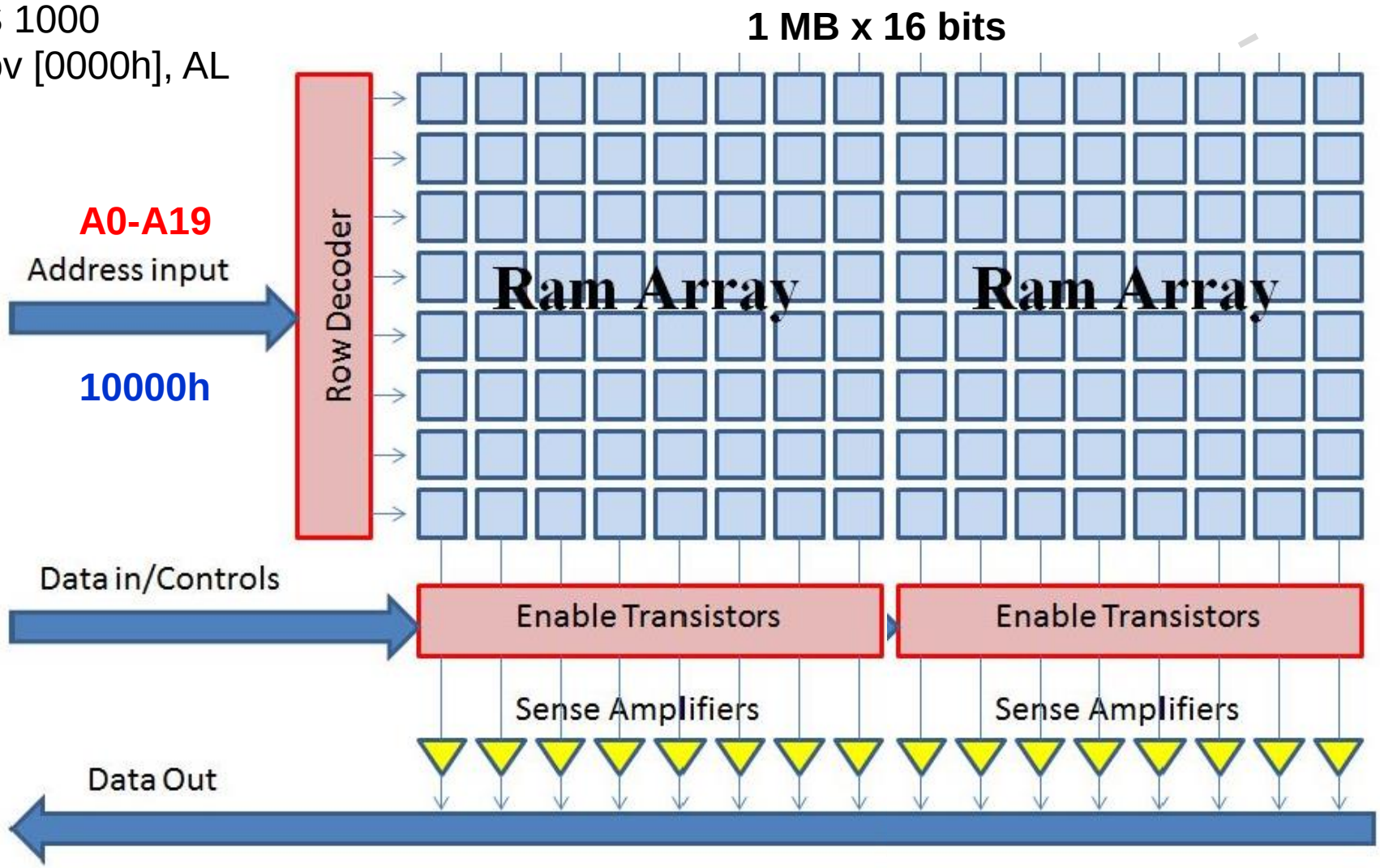


SRAM ARRAY


Address input
Row Decoder
Ram Array
Data in/Controls
Enable Transistors
Sense Amplifiers
Data Out

Memory Banking 8086

DS 1000
Mov [0000h], AL



Memory Banking 8086

1 MB x 16 Bits

00000h - 1000 0000 0000 0000 0000 (A0-A19)
00001h - 1000 0000 0000 0000 0001 (A0-A19)
00002h - 1000 0000 0000 0000 0010 (A0-A19)
00003h - 1000 0000 0000 0000 0011 (A0-A19)
00004h - 1000 0000 0000 0000 0100 (A0-A19)
00005h - 1000 0000 0000 0000 0101 (A0-A19)

A0 = 0

00000h - 0000 0000 0000 0000 000 (A1-A19)
00002h - 0000 0000 0000 0000 001 (A1-A19)
00004h - 0000 0000 0000 0000 010 (A1-A19)

500 KB X 8 bits

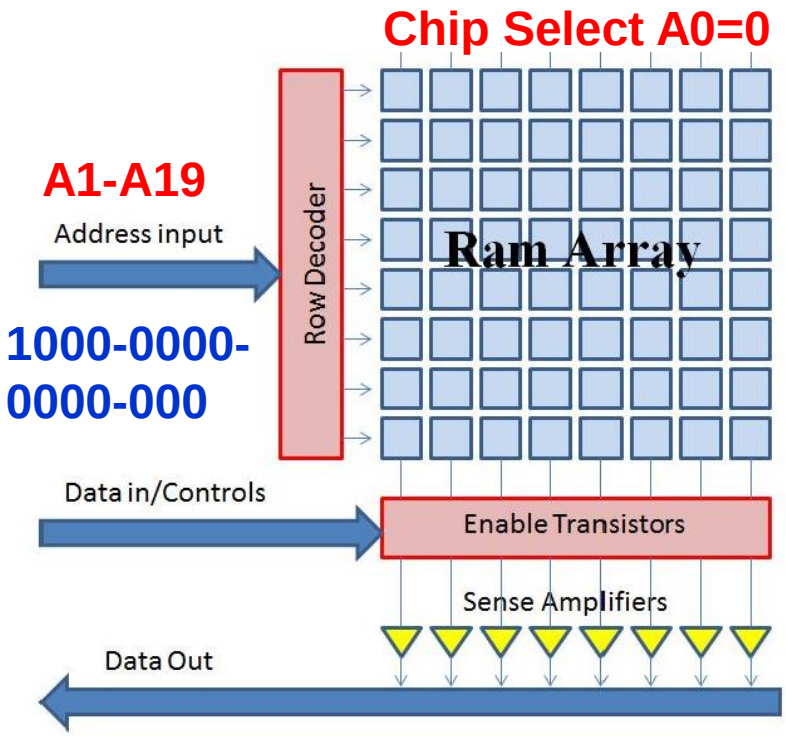
A0 = 1

00001h - 0000 0 000 0000 0000 000 (A1-19)
00003h - 0000 0000 0000 0000 001 (A1-19)
00005h - 0000 0000 0000 0000 010 (A1-19)

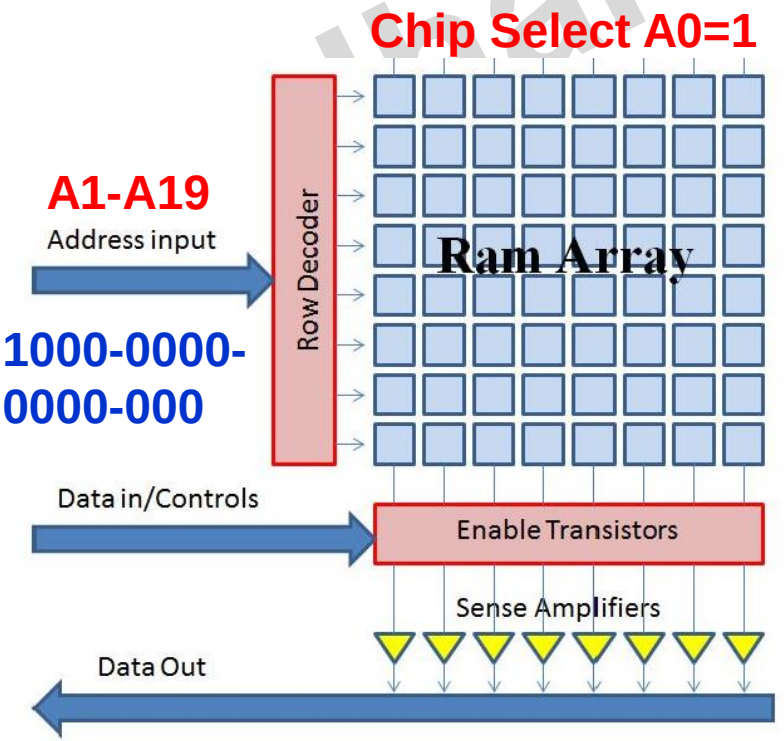
500 KB X 8 bits

Memory Banking 8086

DS 1000
Mov [0000h], AL



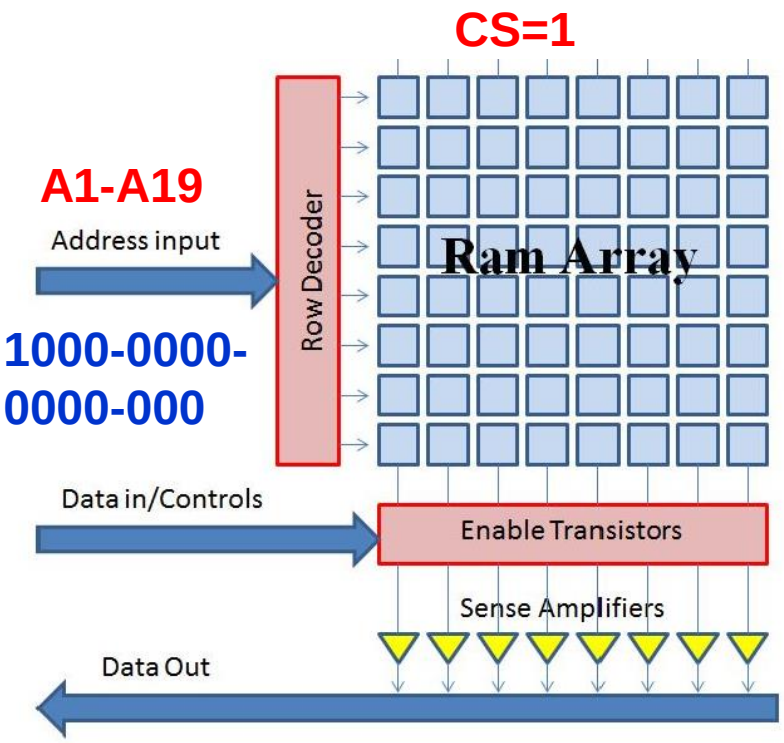
DS 1000
Mov [0001h], AL

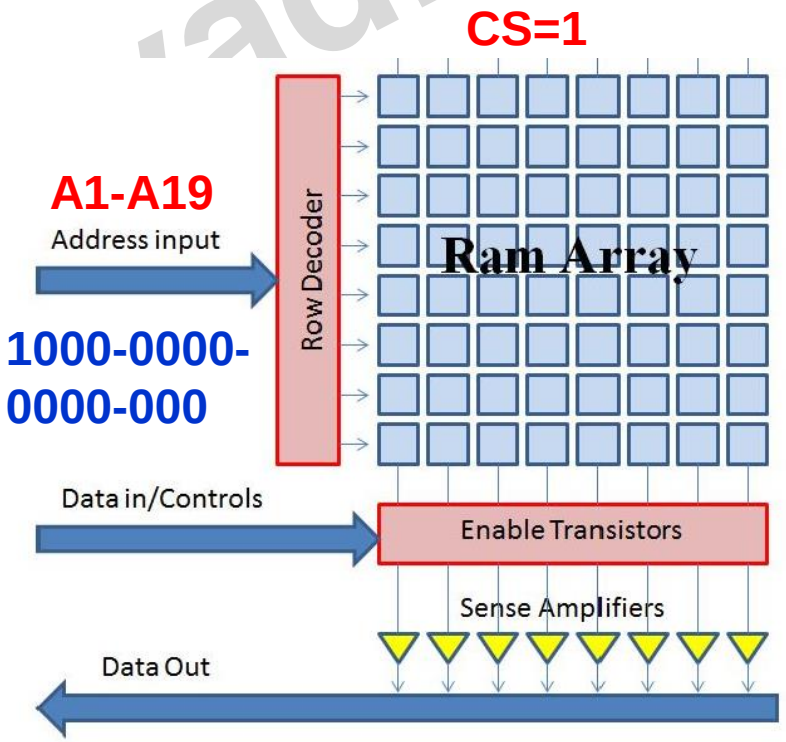


Memory Banking 8086

DS 1000
Mov [0000h], AX $\overline{BHE}$=0

$\overline{BHE}$	A_0	*Indication*
0	0	Whole word (2 bytes)
0	1	Upper byte from or to odd address.
1	0	Lower byte from or to even address
1	1	None

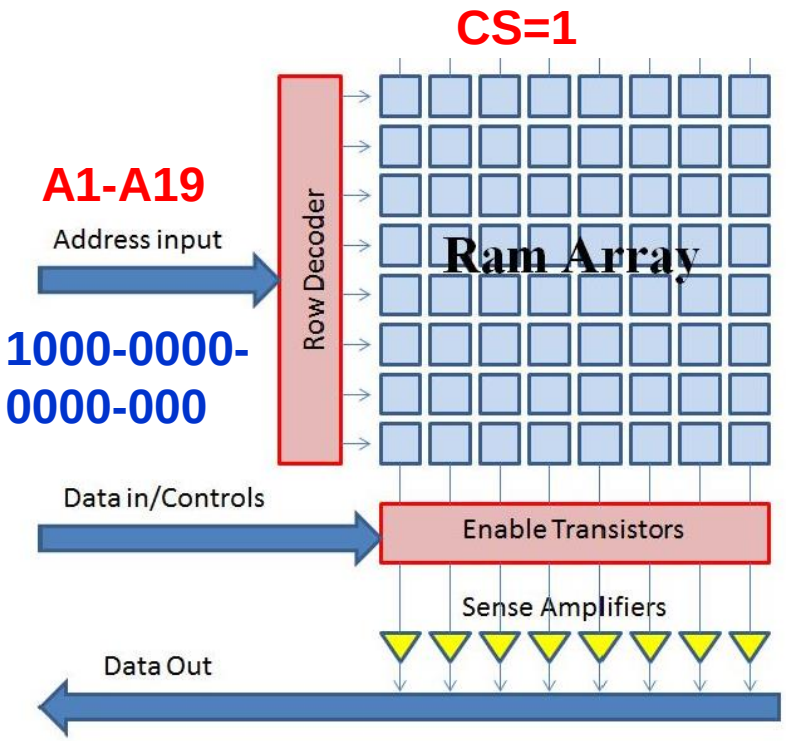


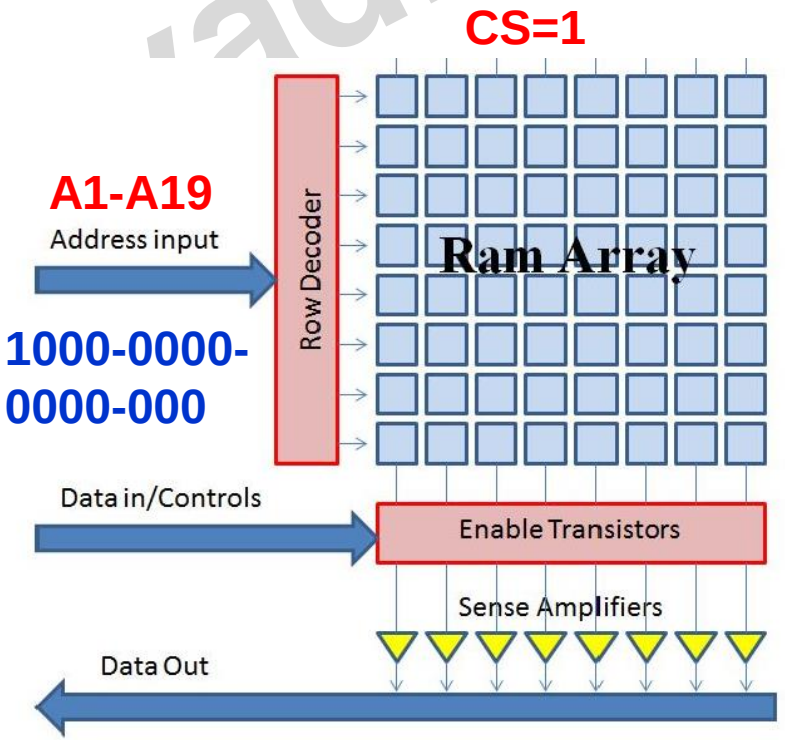


Memory Banking 8086

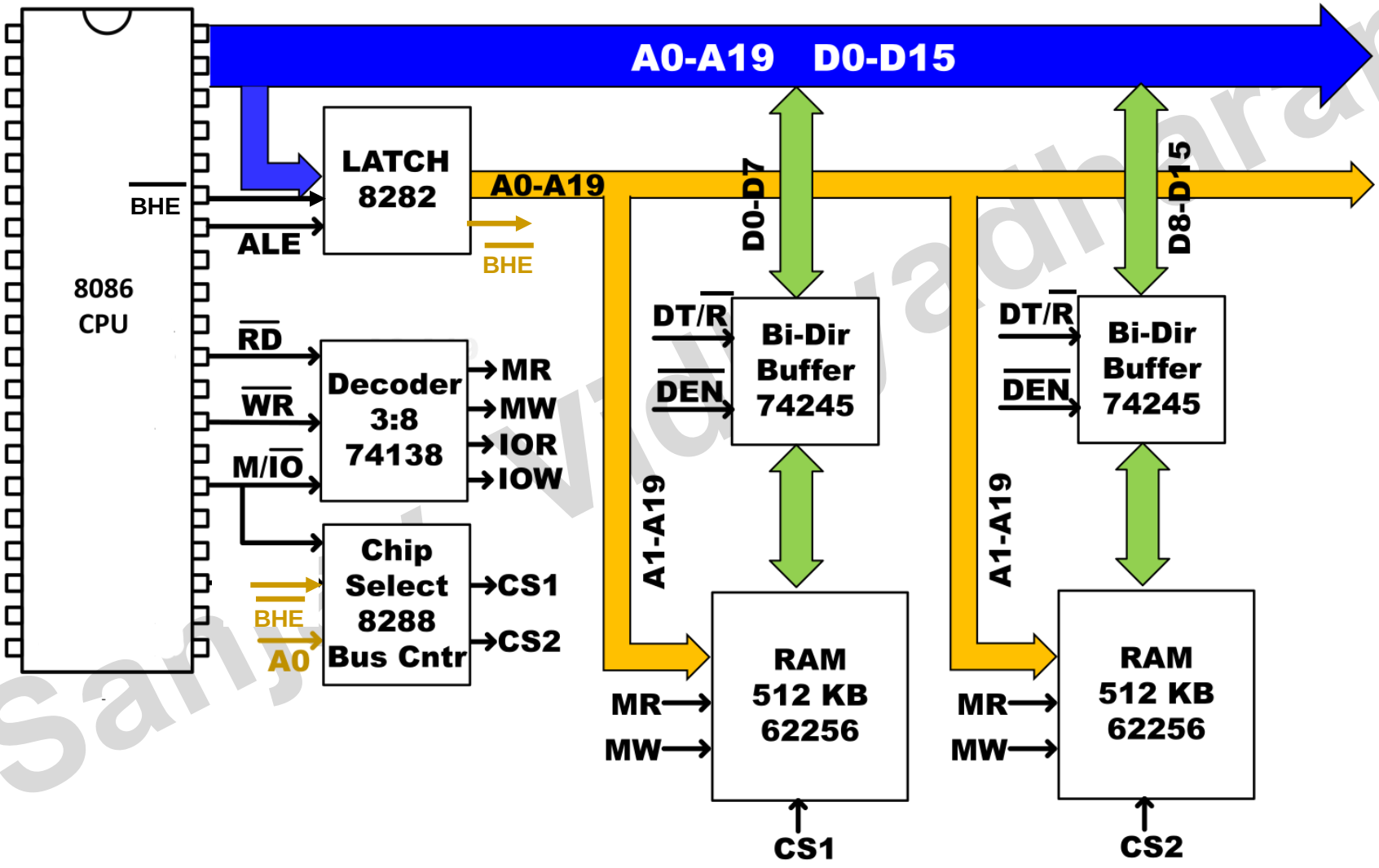
DS 1000
Mov [0000h], CL
Mov [0001h], AX

$\overline{BHE}$	A_0	*Indication*
0	0	Whole word (2 bytes)
0	1	Upper byte from or to odd address.
1	0	Lower byte from or to even address
1	1	None

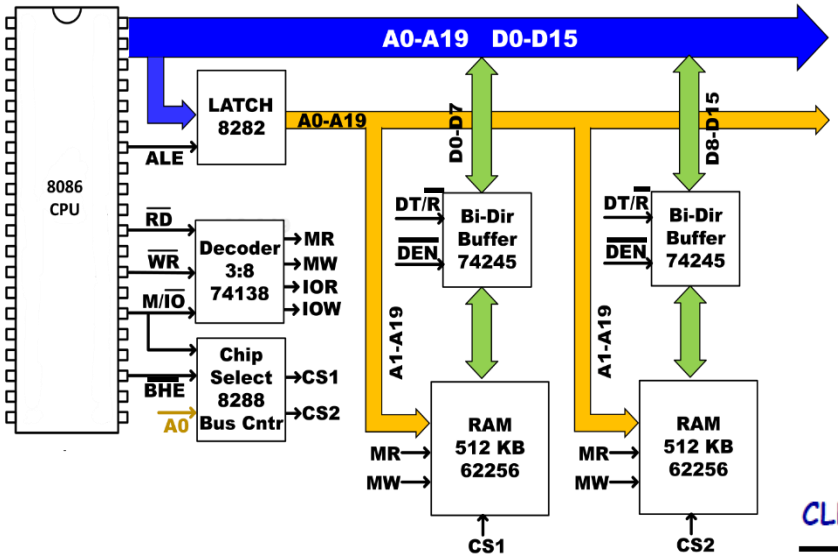


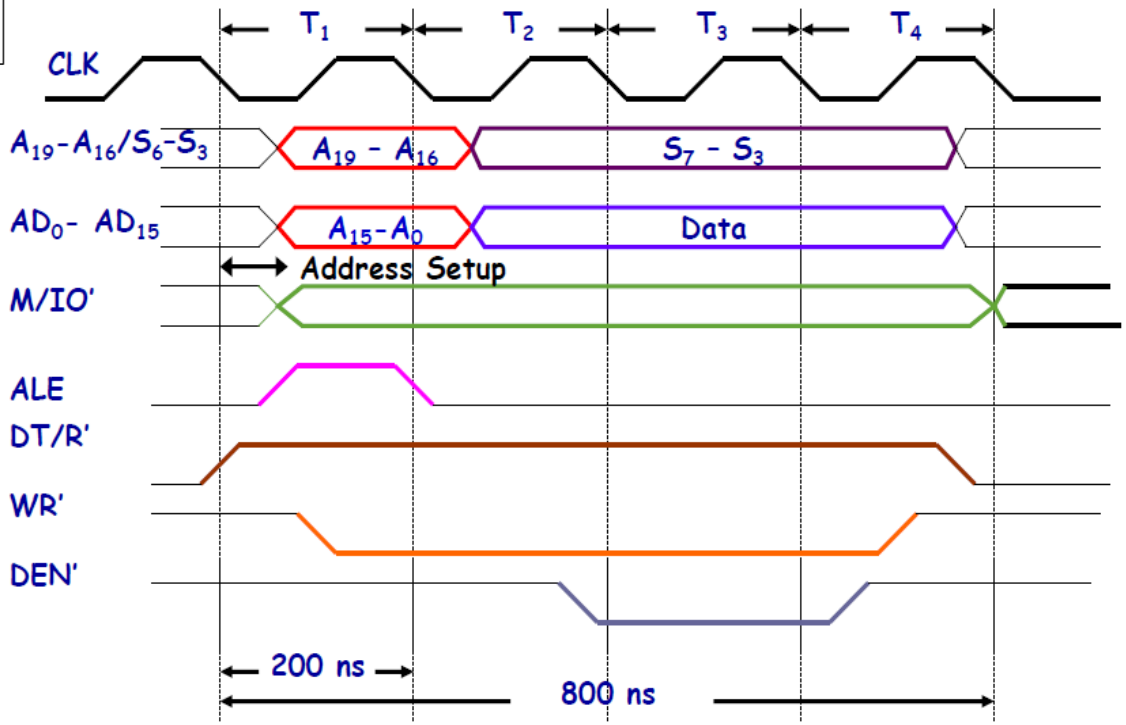


8086 Memory Organization



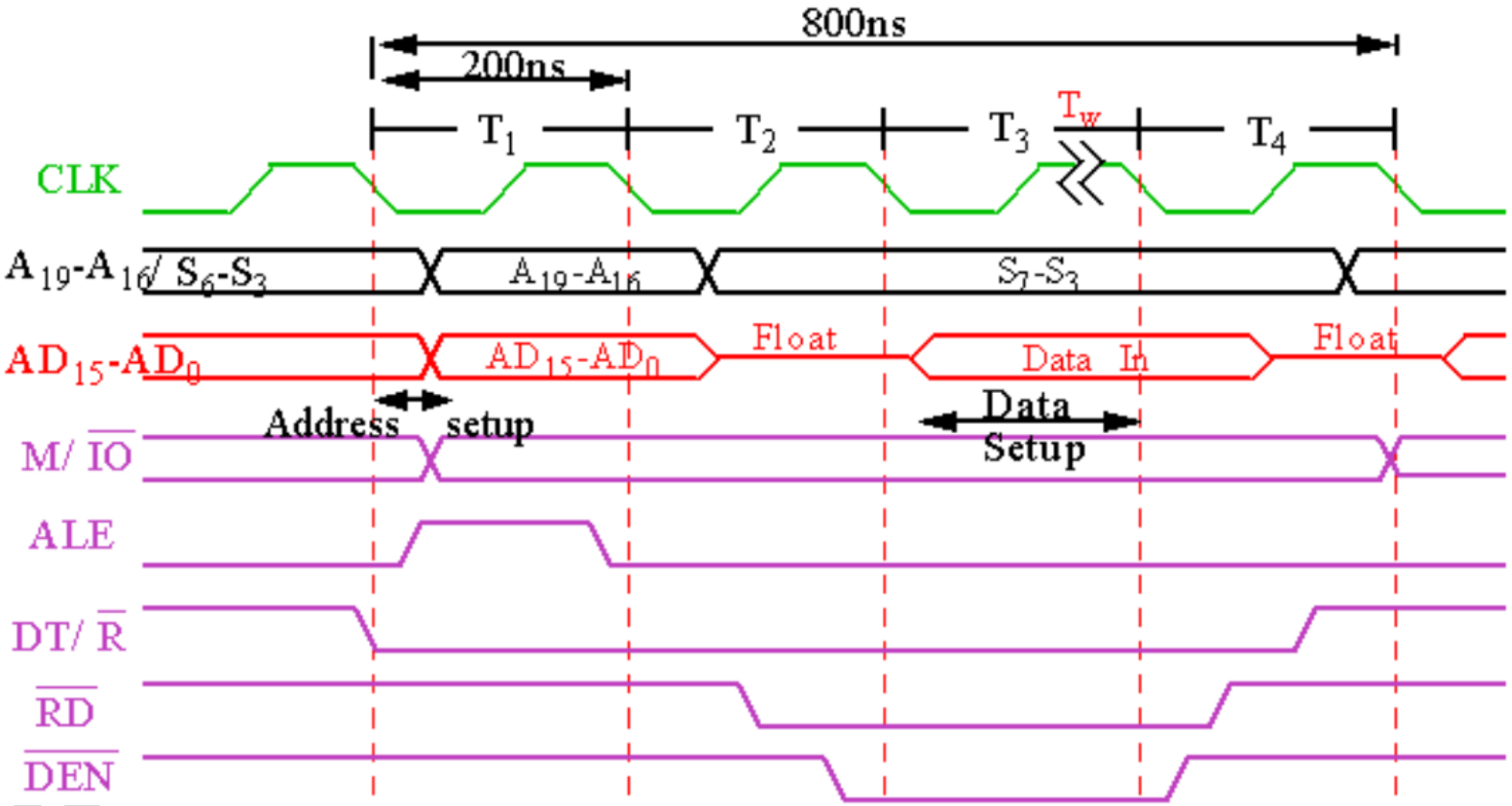
8086 Memory Write Operation





8086 Memory Read Operation

- *Bus Timing:*



Thankyou